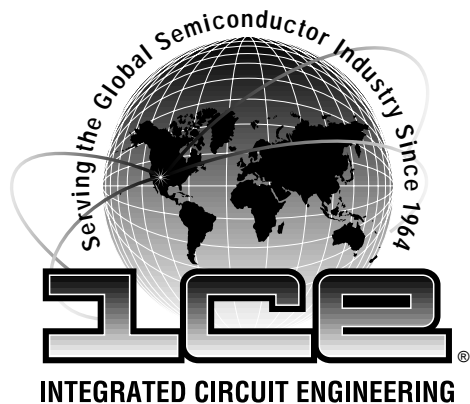


Construction Analysis

Sharp LH28F032SUTD-70 32 Mbit Flash EEPROM

Report Number: SCA 9708-548



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INTRODUCTION

This report describes a construction analysis of the Sharp LH28F032SUTD-70, 32 Mbit Flash EEPROM. Three devices packaged in 56-pin plastic TSOPs were received for the analysis. All devices were date coded 9652.

MAJOR FINDINGS

Questionable Items:¹

- Poly 2 “stringers” at dual poly transistors (Figure 22).

Special Features:

- Dual 16Mbit Flash chips (LH28F016SUT) mounted on both sides of package paddle.
- Dual poly (UPROM ?) gates in periphery.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were encapsulated using a unique 56-pin Thin Small Outline Package (TSOP) design. Package dimensions were 14 x 20 mm.
- One LH28F016SUT-70 16-Mbit EEPROM die was mounted on each side of the package paddle to implement a 32-Mbit Flash memory. Wirebonds were made to both sides (top and bottom) of the leadframe.
- Iron-Nickel leadframe internally plated with silver. External pins (gull wing) were tinned with solder.
- Lead-locking provisions (anchors) at all pins.
- Thermosonic ball bond method employing 0.9 mil O.D. gold wire. Pins 29 and 30 were not connected.
- Sawn dicing (full depth) on both dice.
- Two layers of silver-epoxy die attach.

Die Process

- Fabrication process: Selective oxidation CMOS process. Apparent twin-well process (could not delineate P-wells) in a P-epi on a P substrate.
- Final passivation: A thick multilayered glass over a nitride. No die coat was used on this device.
- Metallization: Two levels of metal defined by dry-etch techniques. Metal 2 consisted of aluminum with a titanium-nitride cap and a titanium barrier/adhesion layer. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier on a thin titanium adhesion layer. Standard vias were used with metal 2 and tungsten plugs (fully lined) were employed for metal 1 contacts.

TECHNOLOGY DESCRIPTION (continued)

- Interlevel dielectric: Interlevel dielectric (between M2 and M1) consisted of a thin layer of glass followed by a thick layer of glass. Remnants of a sacrificial oxide was evident between the two layers. Glass 1 appeared to have been subjected to a back sputter etch, however, planarization was minimal and CMP was not used.
- Pre-metal glass: A single layer of CVD reflow glass (probably BPSG) over various grown/densified oxides.
- Polysilicon: Two layers of polysilicon were employed. Poly 2 (poly 2 and tungsten silicide) was used to form word lines in the cell array and all standard gates on the die. Poly 1 was used to form the floating gates in the array and together with poly 2 to form unusual devices (UPROM?) in the periphery. The interpoly dielectric appeared to consist of oxide-nitride-oxide (ONO).
- No buried contacts were used.
- Thin oxides: Besides the interpoly ONO, apparently three different gate oxides were employed.

Gate oxide 1 under poly 1 in the array.

Gate oxide 2 under poly 1 at the UPROM (?) gates.

Gate oxide 3 under poly 2 in the periphery.

- Diffusions: Implanted N⁺ and P⁺ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing and were left in place.
- Wells: Apparent twin-wells in a P-epi on a P substrate.
- Flash memory: The memory cells consisted of a standard "stacked dual gate" EEPROM based design. Polycide formed the word lines, poly 1 formed the floating gates, metal 2 formed "piggyback" word lines and metal 1 formed the bit lines.

TECHNOLOGY DESCRIPTION (continued)

- SRAM memory: Small SRAM arrays were present at one end of the die. The memory cell was a IOT CMOS SRAM design. Metal 2 distributed GND and formed the bit lines (via metal 1). Metal 1 distributed Vcc and GND and provided cell interconnect. Poly 2 formed the word lines and all gates.
- No redundancy elements were present.
- The process appears to be very similar to that used by Intel for its 32Mbit Flash.

ANALYSIS RESULTS I

Assembly:

Figures 1 - 5

Questionable Items:¹ None.

Special Features:

- Unique “dual die” package with a 16-Mbit die mounted to both sides of the paddle.

General Items:

- Devices were encapsulated using a unique 56-pin Thin Small Outline Package (TSOP). A two-step molding process was probably used, whereby one half of the package was molded separately from the other half. This may have been necessary to facilitate bonding on both sides of the leadframe.
- Overall package quality: Normal. No defects were found on the external portions of the packages. External pins were well formed and tinning was complete.
- Wirebonding: Thermosonic ball bond method using 0.9 mil O.D. gold wire on both die. Wirebonding was made to both sides of the leadframe. No bond lifts occurred and bond pull strengths were good (see page 12). Wire spacing and placement was good. Height of bonding wire arcs resulted in good clearance between the die edge and bonding wires on both sides.
- Die attach: Silver-epoxy of normal quality with no significant voiding noted.
- Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process and Design:

Figures 6 - 39

Questionable Items:¹

- Poly 2 “stringers” at dual poly transistors (Figure 22).

Special Features:

- Dual poly (UPROM?) gates.

General Items:

- Fabrication process: Selective oxidation CMOS process. Apparent twin-well process (could not delineate P-wells) in a P-epi on a P substrate. No significant problems were found in the basic process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: A thick multilayered glass over a layer of nitride. The nitride cusped at vias, creating voids; however, passivation integrity tests indicated defect-free passivation. Edge seal was also good, as the passivation extended into the scribe lane to seal the metallization. A cutout was present in the passivation around the scribe lane to prevent cracks from radiating over the active circuitry.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

ANALYSIS RESULTS II (continued)

- Metallization: Two levels of metallization were used. Metal 2 consisted of aluminum with a titanium-nitride cap and a titanium barrier (adhesion layer). Metal 1 consisted of aluminum with a titanium-nitride cap and barrier on a thin titanium adhesion layer.
- Metal defects: None. No notching or voiding was noted in either metal layer. No silicon nodules were found following removal of the metal layers.
- Metal step coverage: Metal 2 aluminum thinned up to 85 percent at via edges. The cap and barrier metal thinned as well at via edges. Metal 1 aluminum thinned only 25 percent at contact edges due to the use of tungsten plugs. MIL-STD-883D allows up to 70 percent metal thinning at contacts of this size.
- Metal patterning: Both metal layers were defined by a dry etch of good quality. Metal lines were widened around some vias and contacts. Metal completely surrounded all vias and contacts.
- Vertical interconnect: Standard via contacts between metal 2 and metal 1. Tungsten plugs were used under the metal 1 at contacts. Tungsten plugs were fully lined with titanium-nitride including the tops of the plugs.
- Vias and contacts: Via cuts were slope-etched and contacts were etched straight. No significant over-etching was found at contacts. The via etch did remove the metal 1 cap and a small portion of the aluminum layer in these areas. No problem appears to exist.
- Interlevel dielectric: Interlevel dielectric consisted of a thin layer of glass followed by a thick layer of glass (plus a sacrificial oxide between). Glass 1 had been subjected to back sputtering as the only attempt at planarization in this area. No spin-on-glass or CMP techniques were used. No problems were found in these layers.
- Pre-metal glass: A layer of reflow glass (probably BPSG) over various grown oxides. This layer was well reflowed prior to contact cuts. No problems were found.

ANALYSIS RESULTS II (continued)

- Polysilicon: Two layers of polysilicon were employed. Poly 2 (poly 2 and tungsten silicide) was used to form all standard gates on the die, the program lines in the array and on top of the dual (UPROM?) gates. Poly 1 was used to form the floating gates in the cell array and to form connected (UPROM?) gates under poly 2 in the periphery. Definition of the poly layers was by a dry etch. Some residual poly 2 “stringers” were found at the dual gate structures; but this does not appear to present a problem. No “stringers” were found in the array.
- Thin oxides: No problems were found. Apparently three different thickness gate oxides were used, plus a thin interpoly dielectric layer between poly 1 and poly 2. The dielectric clearly appeared to be an ONO (oxide-nitride-oxide). All gate oxides were grown oxides (SiO₂). The gate oxides are listed here as:

Gate oxide "1" under poly 1 in the array.

Gate oxide "2" under poly 1 at the UPROM (?) gates.

Gate oxide "3" under poly 2 in periphery.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. There did not appear to be a step in the oxide at well boundaries. The tops of the LOCOS was etched back to be almost planar with the silicon surface, leaving very short birdsbeaks.
- Diffusions: An LDD process was used employing oxide sidewall spacers. The spacers were left in place. Implanted N⁺ and P⁺ diffusions were used for sources and drains. No problems were found in any of these areas.
- Wells: Apparent twin-wells (could not delineate P-wells) were used in a P-epi on a P substrate. Definition of the N-wells was normal.
- Buried contacts: Direct poly to diffusion contacts were not used..

ANALYSIS RESULTS II (continued)

- Flash memory: The memory cells consisted of a standard "stacked dual gate" EEPROM based design. Metal 2 "piggybacked" poly 2 word lines, poly 1 formed the floating gates, and metal 1 formed the bit lines. The dielectric between the gates appeared to consist of oxide-nitride-oxide (ONO). Cell size was 1.8 x 1.9 microns.
- SRAM memory: Small SRAM arrays were present at one end of the die. The memory cell design was an IOT CMOS SRAM design. Metal 2 distributed GND and formed the bit lines (via metal 1). Metal 1 distributed Vcc and GND and provided cell interconnect. Poly 2 formed the word lines and all gates. Cell size was 14.5 x 20 microns.
- No redundancy elements were present.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM inspection of assembly features

Wirepull test

Passivation integrity test

Delayer to metal 2 and inspect

Aluminum removal (metal 2)

Delayer to metal 1 and inspect

Aluminum removal (metal 1)

Delayer to tungsten plugs, polycide/substrate and inspect

Die sectioning (90° for SEM)

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	N
Package markings	G
Die placement	G
Wirebond placement	G
Wire spacing	G
Wirebond quality	N
Die attach quality	G
Dicing quality	N
Die attach method	Silver-epoxy
Dicing method:	Sawn (full depth)
Wirebond method:	Thermosonic ball/stitch bonds using 0.9 mil gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	G
Metal integrity	NP*
Metal registration	N
Contact coverage	G
Contact registration	G

*85 percent metal 2 aluminum thinning.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

SAMPLE #

1 - 3

TOP

LH28F032SUTD-70
SHARP
JAPAN
9652 30

WIREBOND STRENGTH

Wire material: 0.9 mil diameter gold

Die pad material: aluminum

of wires pulled: 25

Bond lifts: 0

Force to break - high: 8g

- low: 5g

- avg.: 5.6g

- std. dev.: 0.75

DIE MATERIAL ANALYSIS

Final passivation: Thick multilayered glass over a nitride.

Metallization 2: Aluminum with a titanium-nitride cap and titanium barrier layer.

Interlevel dielectric (M2 to M1): Two layers of silicon-dioxide.

Metallization 1: Aluminum with a titanium-nitride cap and barrier on a titanium adhesion layer.

Plugs: Tungsten

Pre-metal glass: Reflow glass (probably BPSG) over grown/densified oxides.

Polycide: Tungsten-silicide on polysilicon.

Interpoly dielectric: Oxide-nitride-oxide (ONO).

HORIZONTAL DIMENSIONS

Die size:	10.6 x 12.2 mm (419 x 482 mils)
Die area:	130 mm ² (201,958 mils ²)
Min pad size:	0.13 x 0.13 mm (5.0 x 5.0 mils)
Min pad window:	0.1 x 0.1 mm (4.0 x 4.0 mils)
Min pad space:	0.06 mm (2.6 mils)
Min metal 2 width:	1.0 micron
Min metal 2 space:	0.9 micron
Min metal 1 width:	1.0 micron
Min metal 1 space:	0.55 micron
Min via:	1.0 micron
Min contact:	0.65 micron
Min poly 2 width:	0.6 micron
Min poly 2 space:	0.85 micron
Min poly 1 width:	0.75 micron
Min gate length* - (N-channel):	0.75 micron
- (P-channel):	0.75 micron
Flash cell size:	1.8 x 1.9 micron
Flash cell area:	3.4 microns ²
SRAM cell size:	14.5 x 20 microns
SRAM cell area:	290 microns ²

*Physical gate length.

VERTICAL DIMENSIONS

Layers

Passivation 2:	2.1 microns
Passivation 1:	1.2 micron
Metal 2 - cap:	0.05 micron (approximate)
- aluminum:	1.0 micron
- barrier:	0.1 micron
Interlevel dielectric glass 2:	0.55 micron (average)
glass 1:	0.25 micron
Metal 1 - cap:	0.07 micron (approximate)
- aluminum:	0.4 micron
- barrier:	0.07 micron (approximate)
Pre-metal dielectric:	0.85 micron (average)
Poly 2 - silicide:	0.15 micron
- poly:	0.15 micron
Poly 1:	0.12 micron
Local oxide (under poly 2):	0.5 micron
N+ S/D diffusion:	0.25 micron
P+ S/D diffusion:	0.35 micron
N- well:	1.6 micron
P-epi:	5 microns

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SRAM MEMORY CELL	Figures 37 - 39

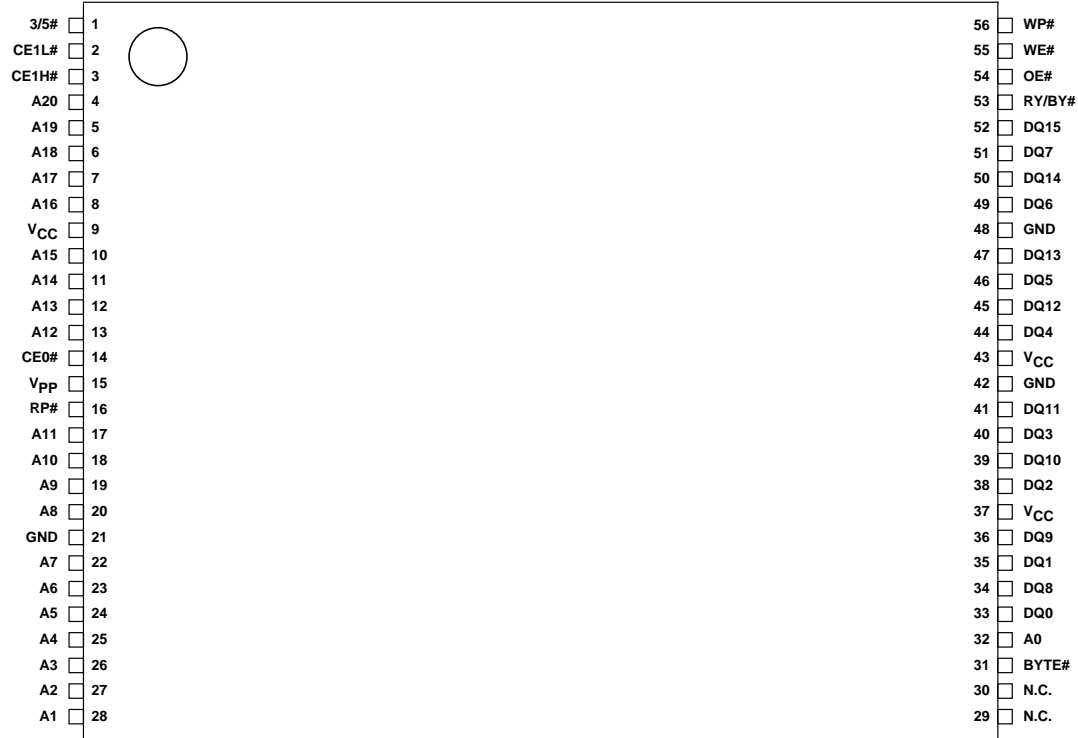


Figure 1. Package photograph and pinout diagram of the Sharp LH28FO32SUTD-70.
Mag. 4x.

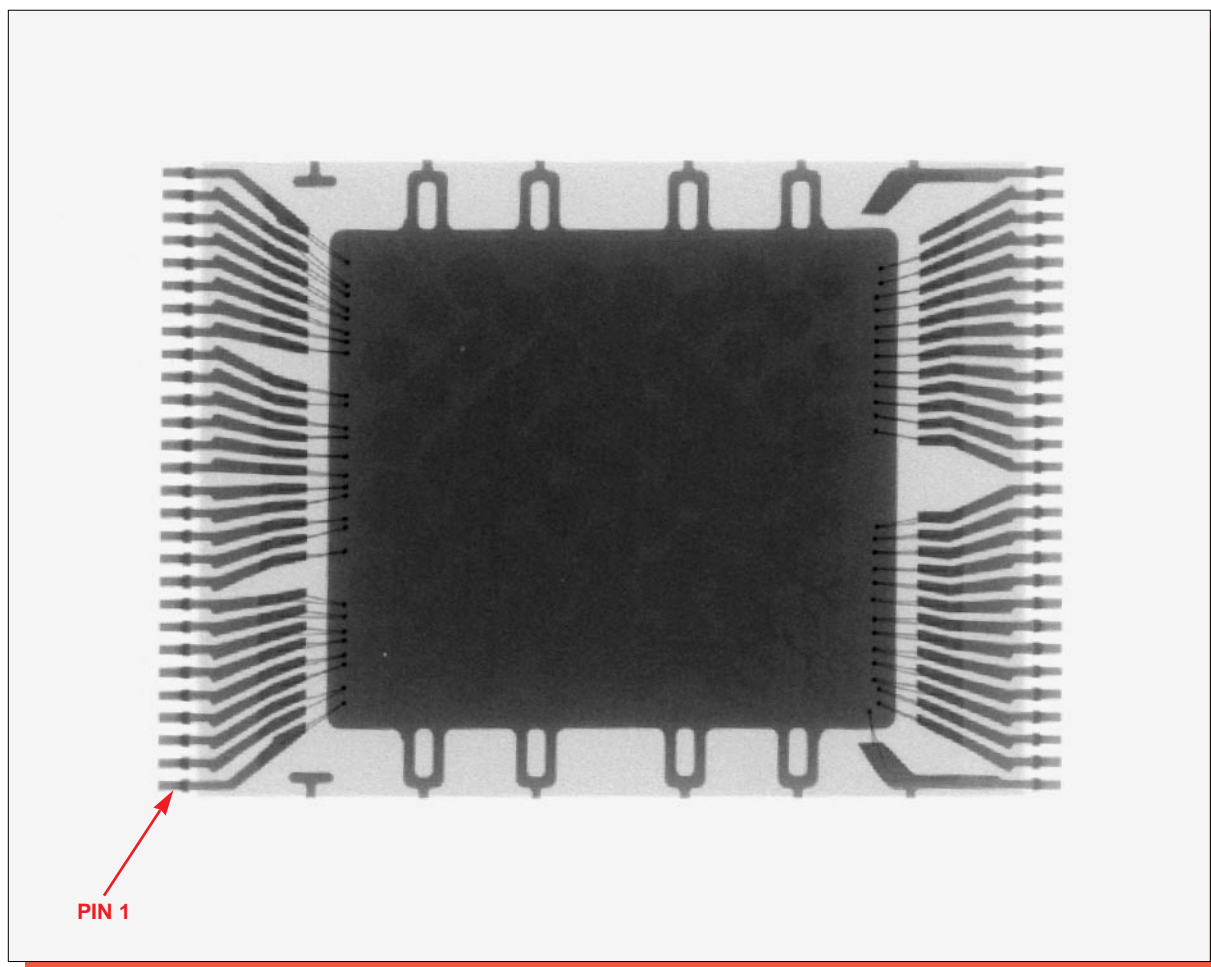
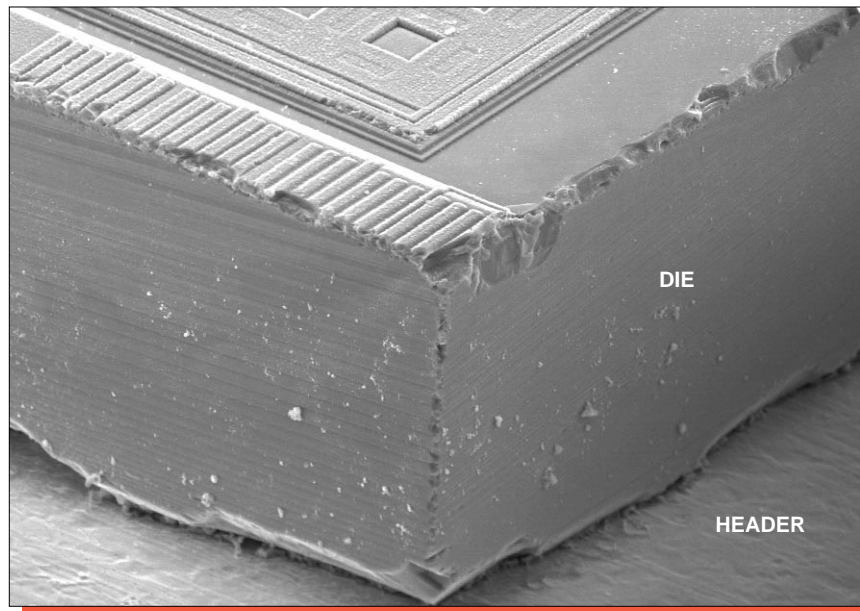
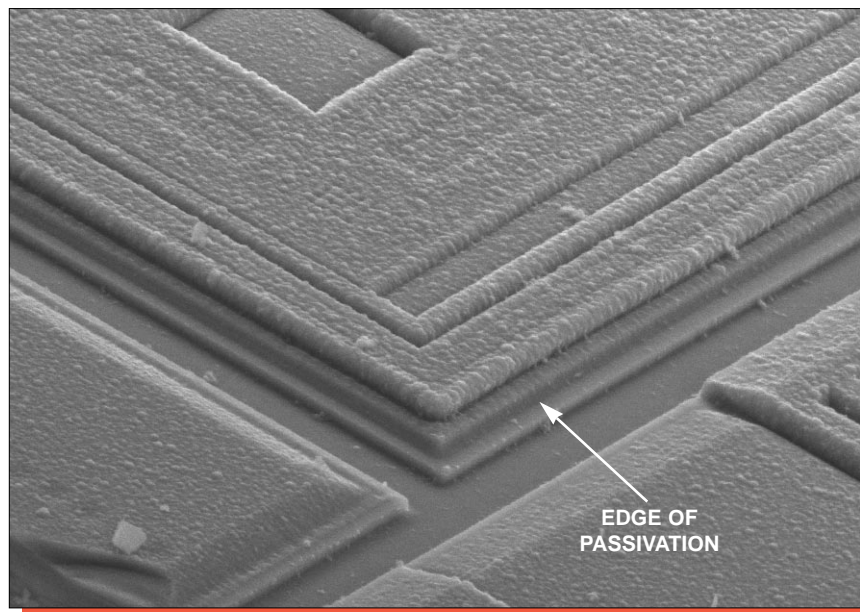


Figure 2. X-ray view of the package. Mag. 6x.



Mag. 300x



Mag. 1000x

Figure 3. SEM views of a die corner and edge seal. 60°.

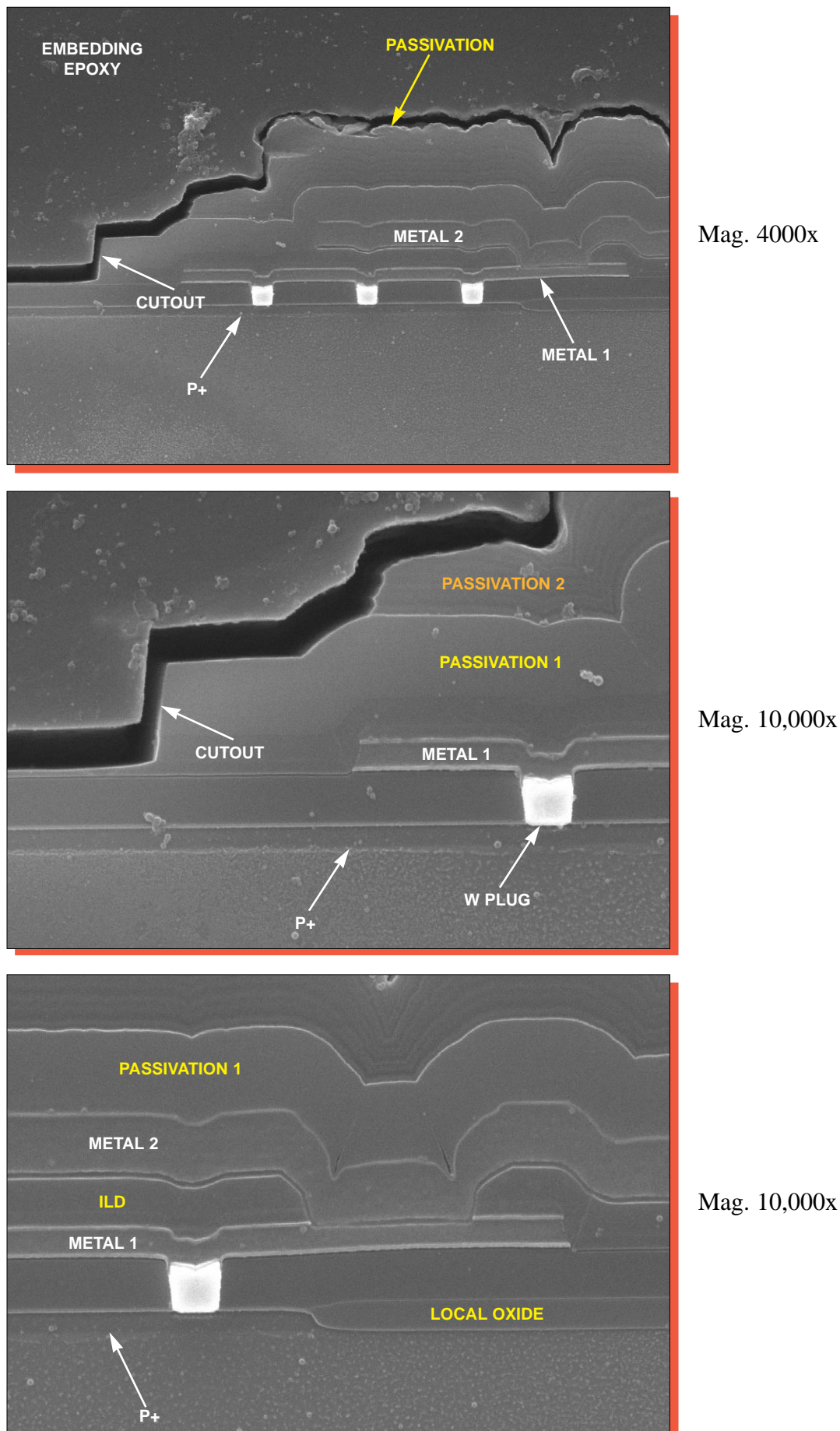
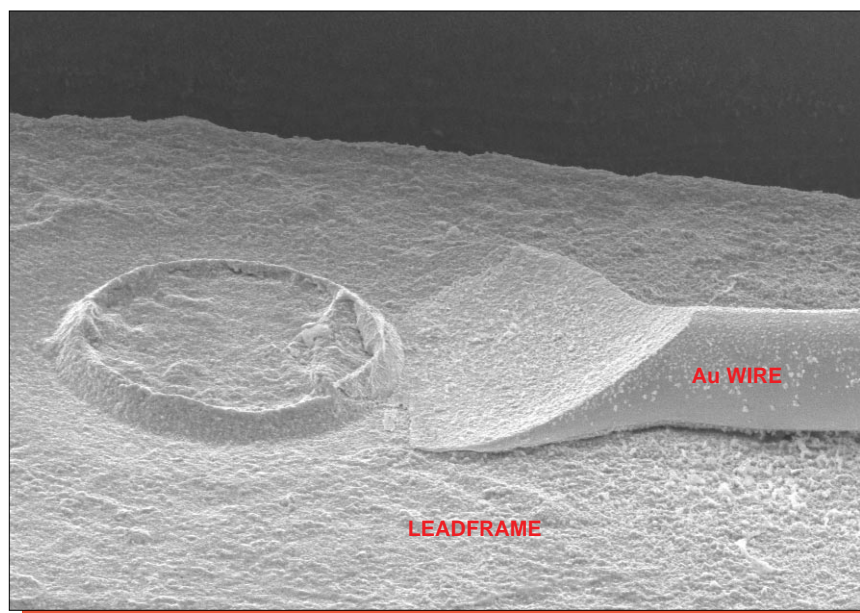
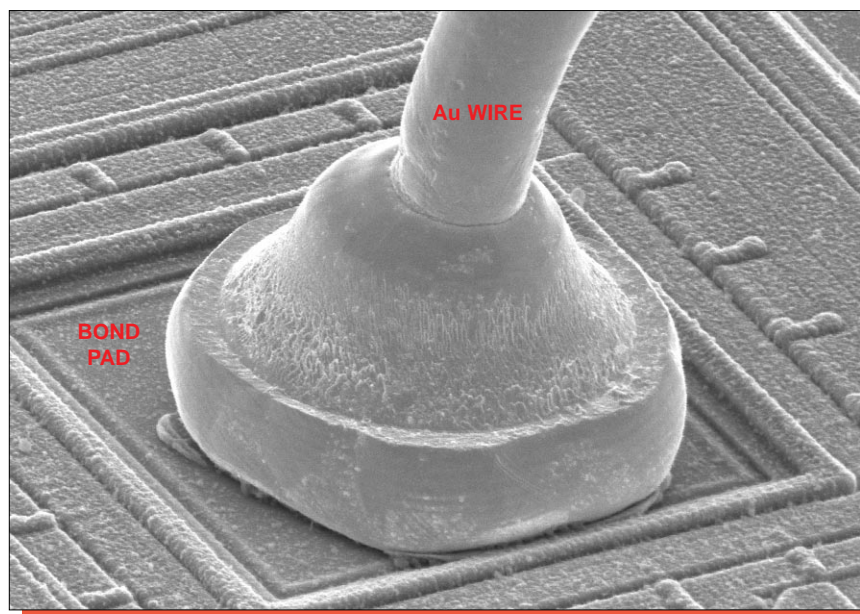


Figure 4. SEM section views of the edge seal structure.



Mag. 650x



Mag. 750x

Figure 5. SEM views of typical wirebonds. 60°.

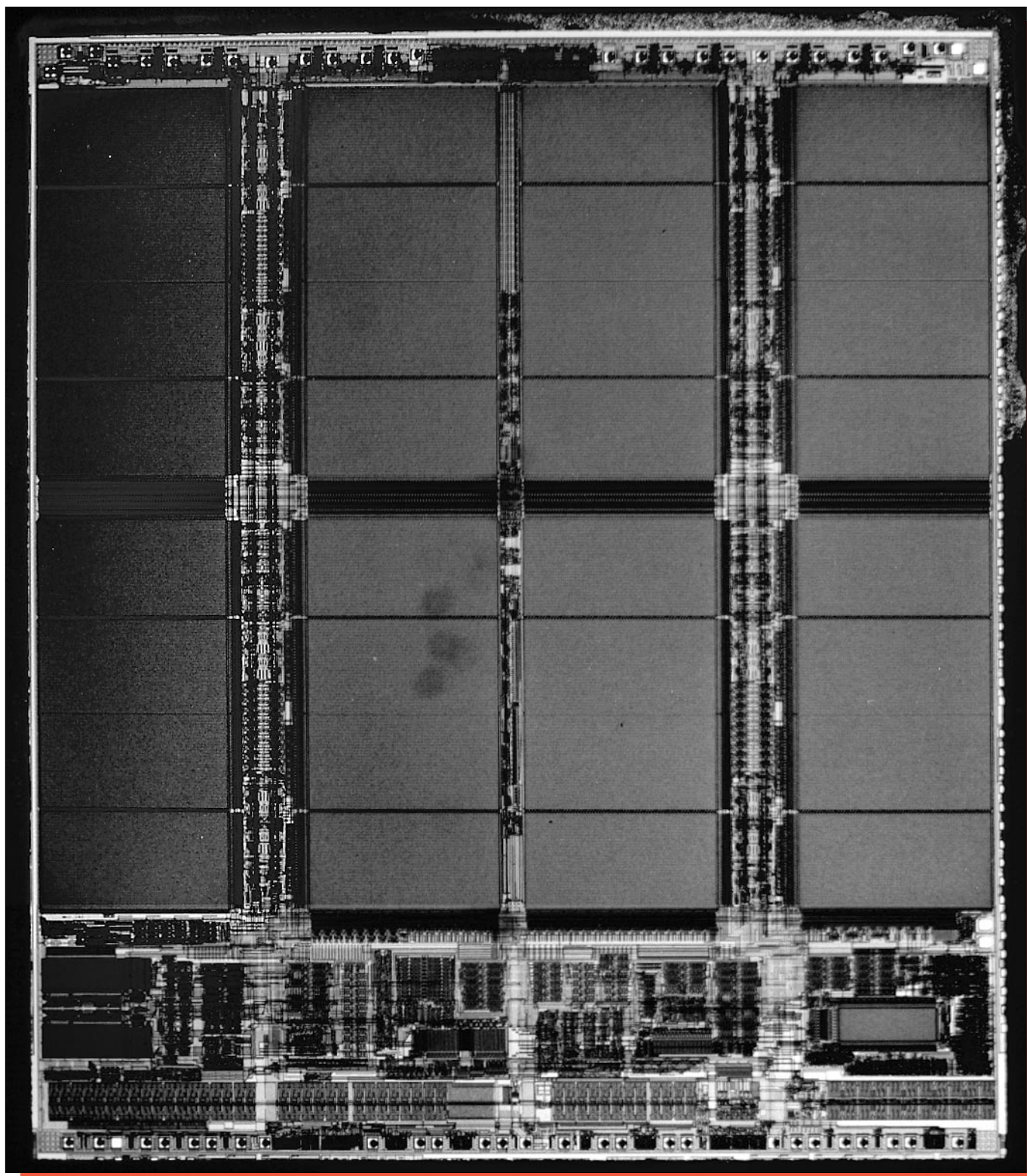
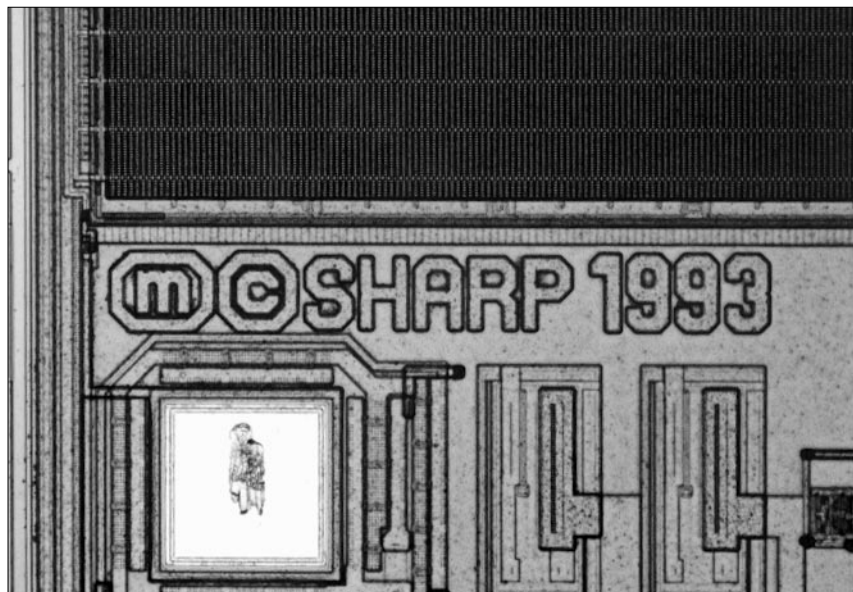
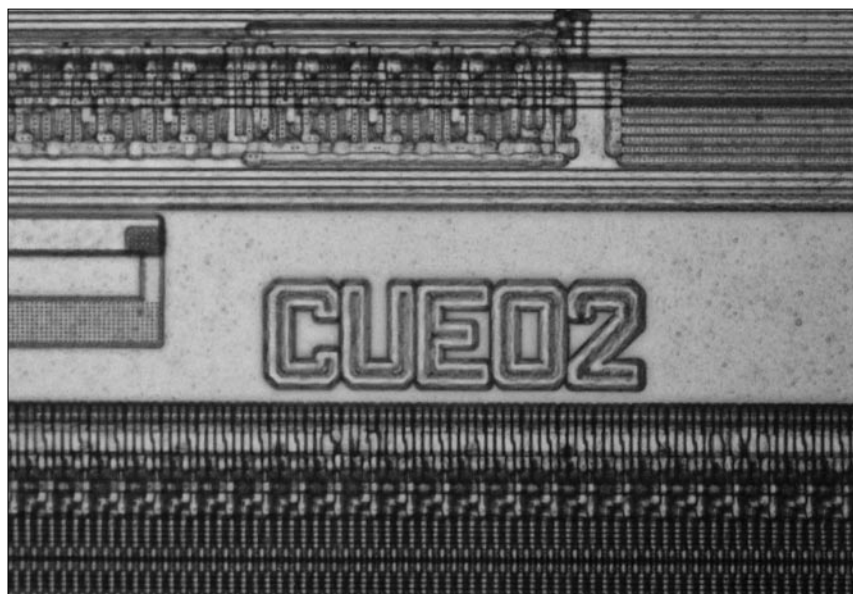


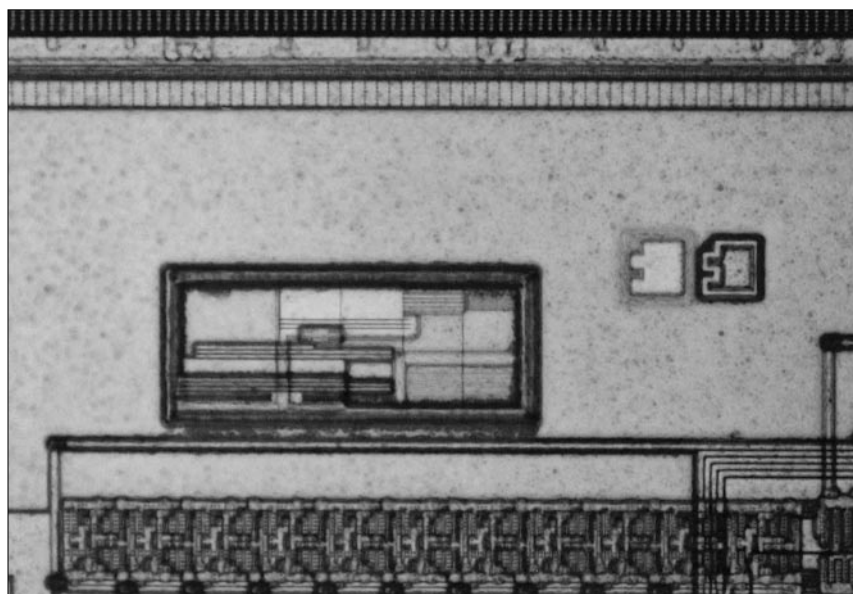
Figure 6. Whole die photograph of the Sharp LH28F032SUTD-70. Mag. 16x.



Mag. 200x



Mag. 400x



Mag. 320x

Figure 7. Optical views of markings on the die surface.

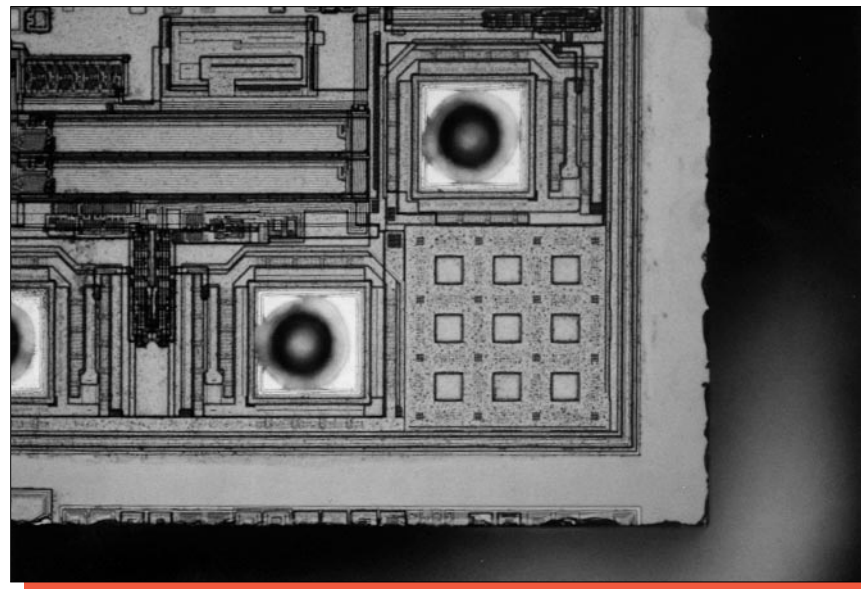
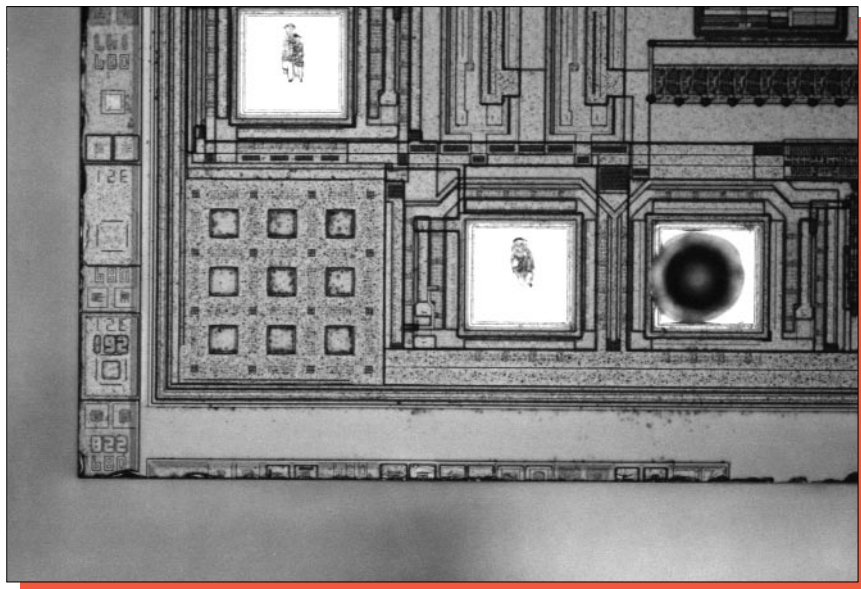
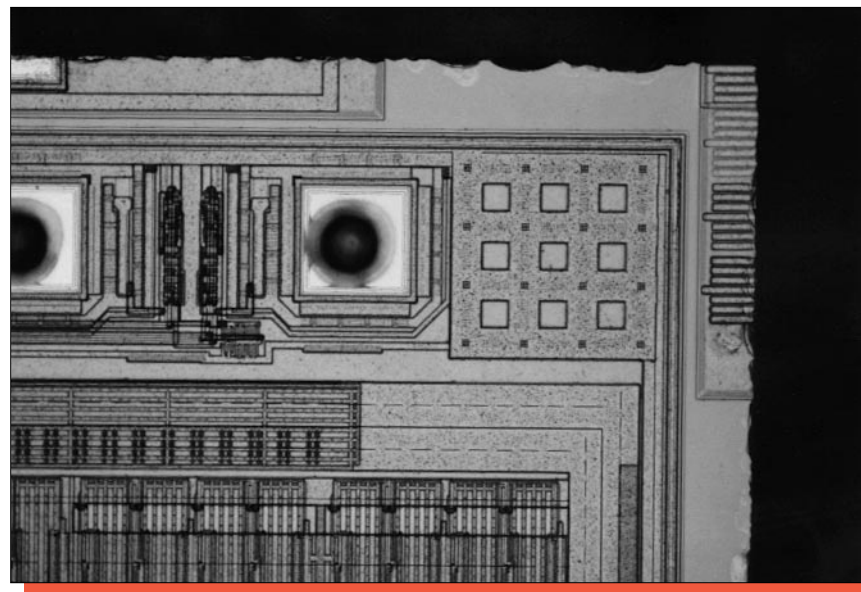
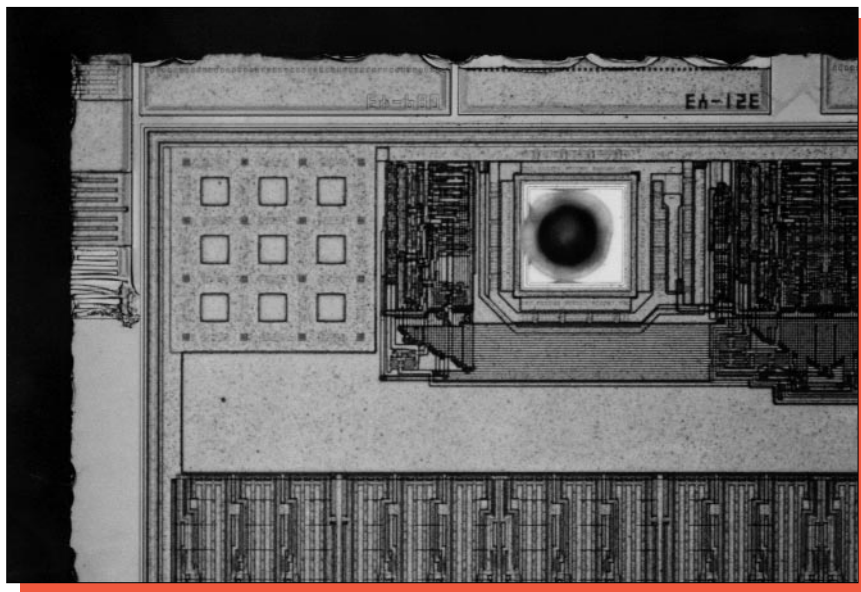
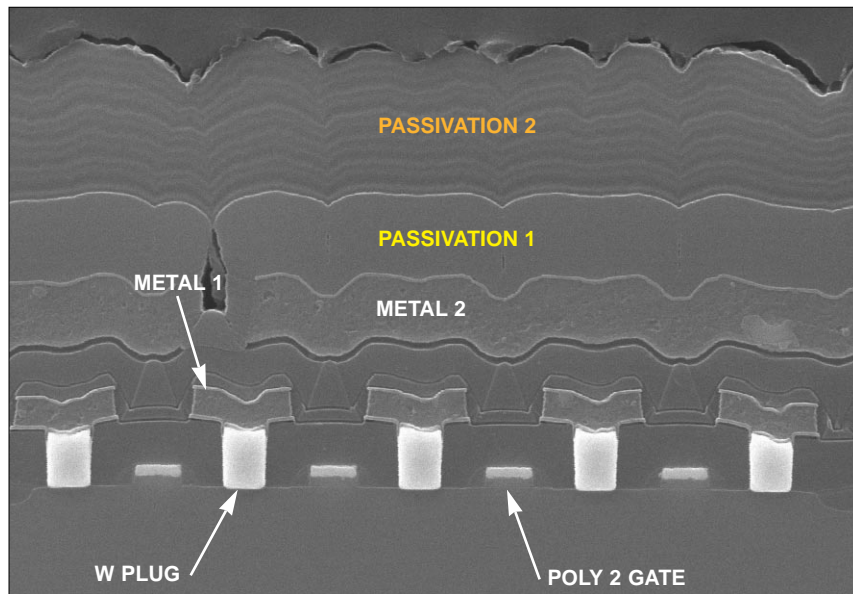
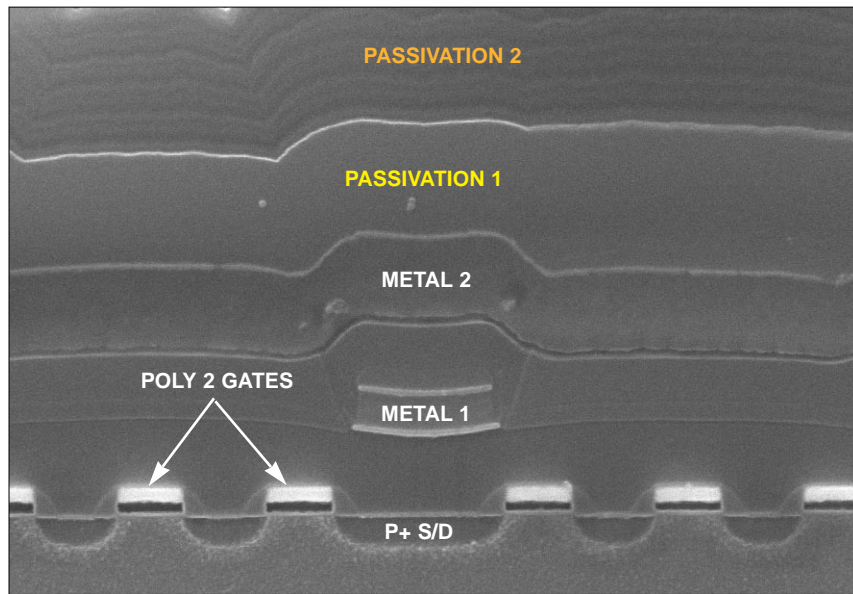


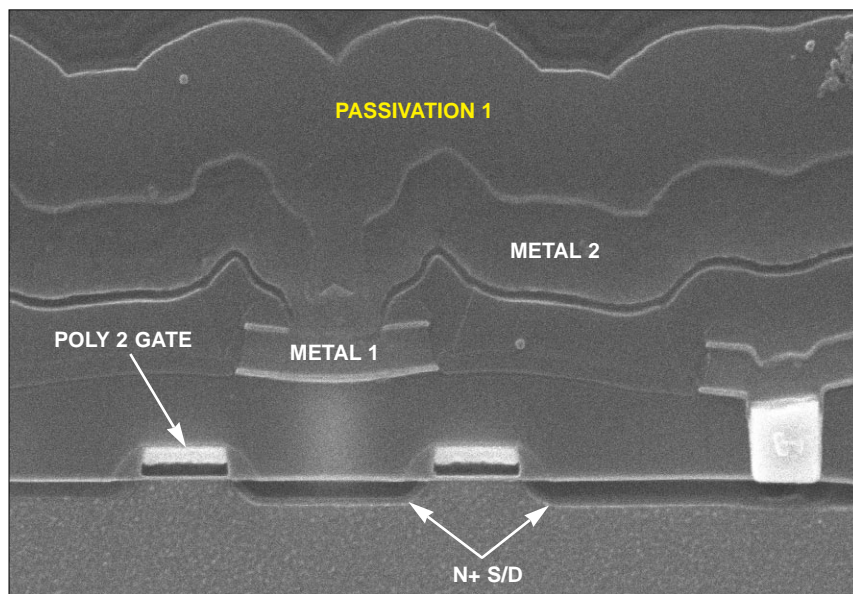
Figure 8. Optical views of the die corners. Mag. 130x.



glass etch,
Mag. 8400x

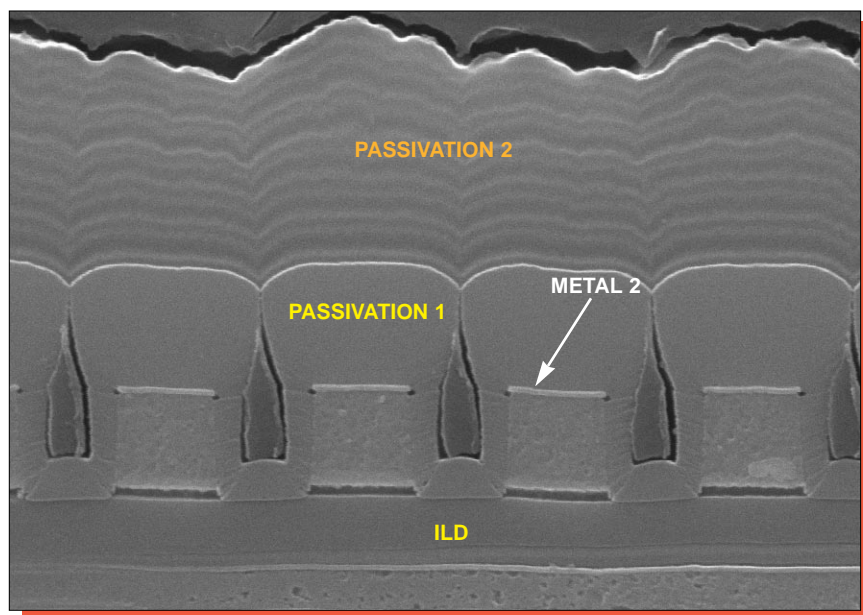


Mag. 11,000x

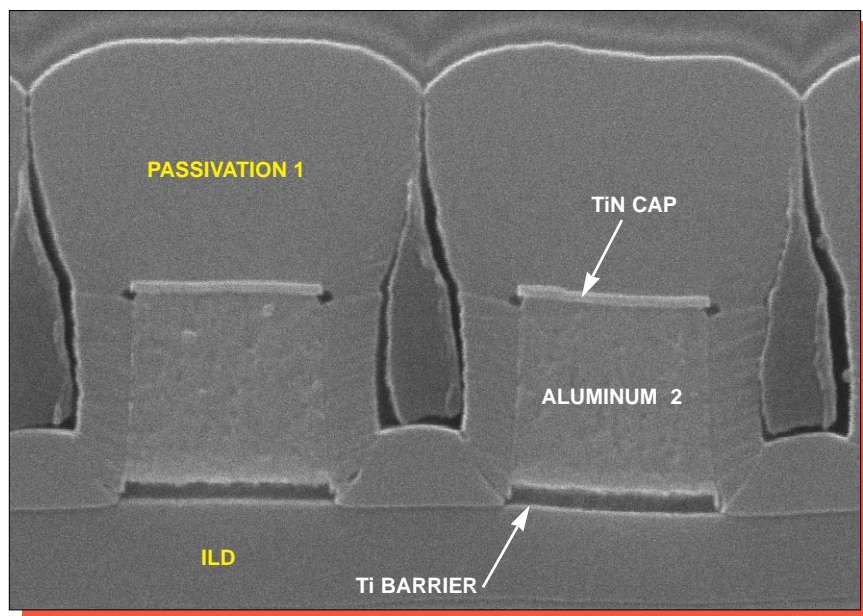


Mag. 13,000x

Figure 9. SEM section views illustrating general device structure.

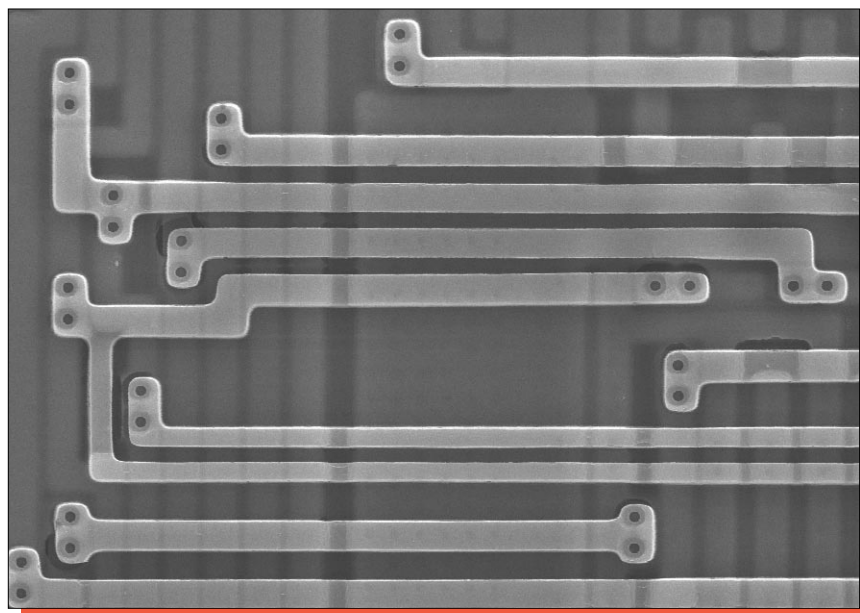


Mag. 13,000x

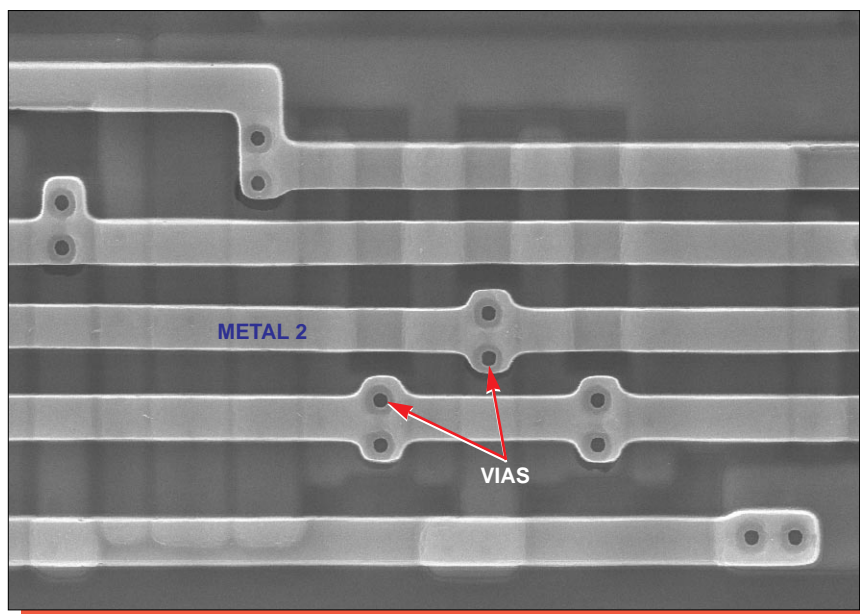


Mag. 26,000x

Figure 10. SEM section views of metal 2 line profiles.

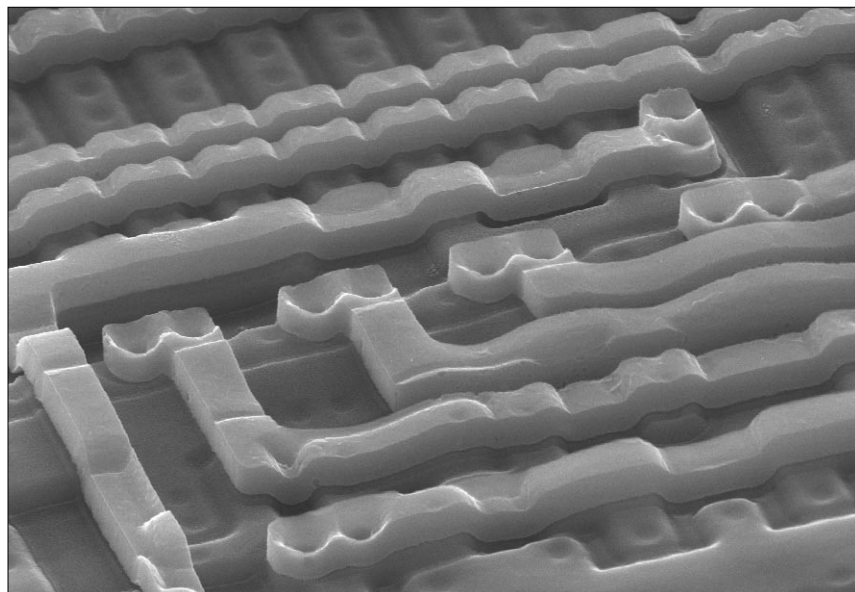


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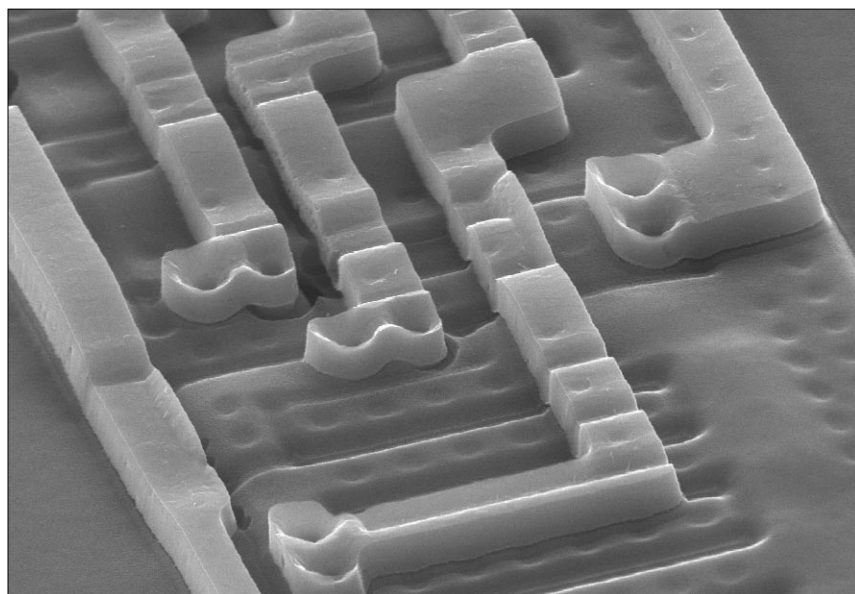


Mag. 3000x

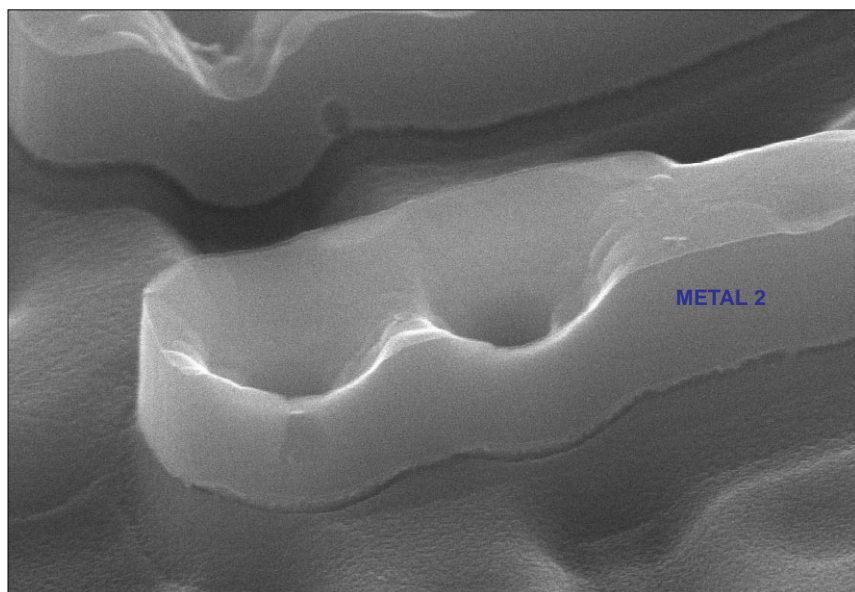
Figure 11. Topological SEM views illustrating metal 2 patterning. 0°.



Mag. 4200x



Mag. 5000x



Mag. 17,000x

Figure 12. SEM views of general metal 2 integrity. 55°.

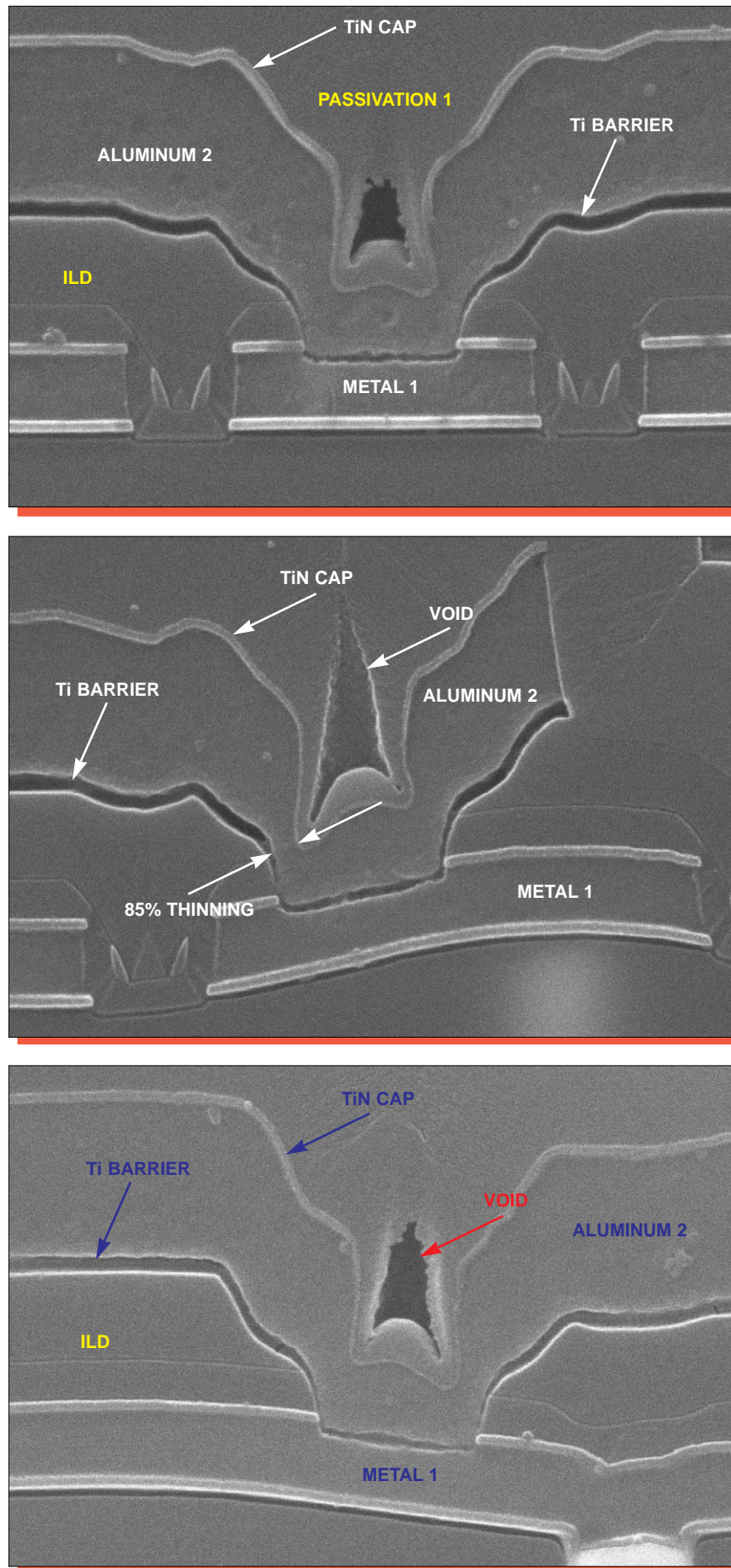
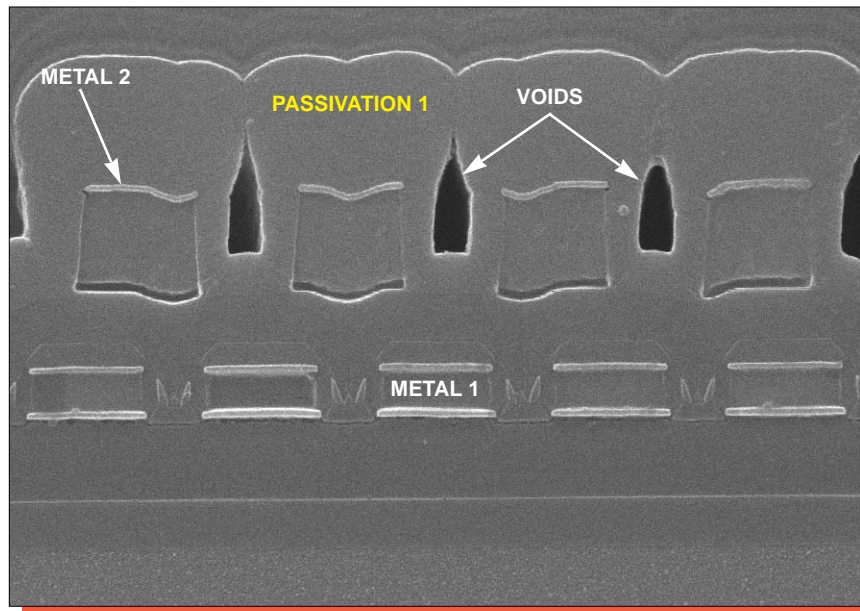
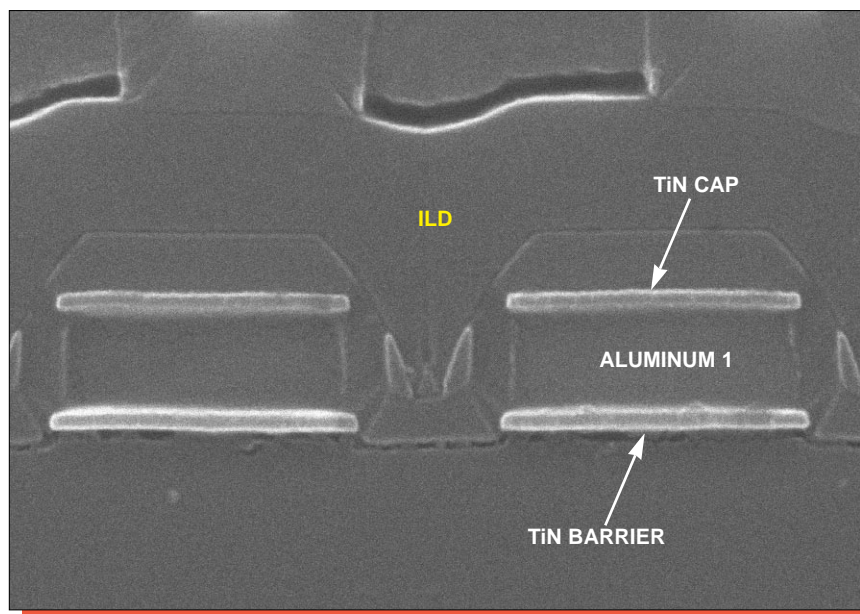


Figure 13. SEM section views of metal 2-to-metal 1 vias. Mag. 25,000x.

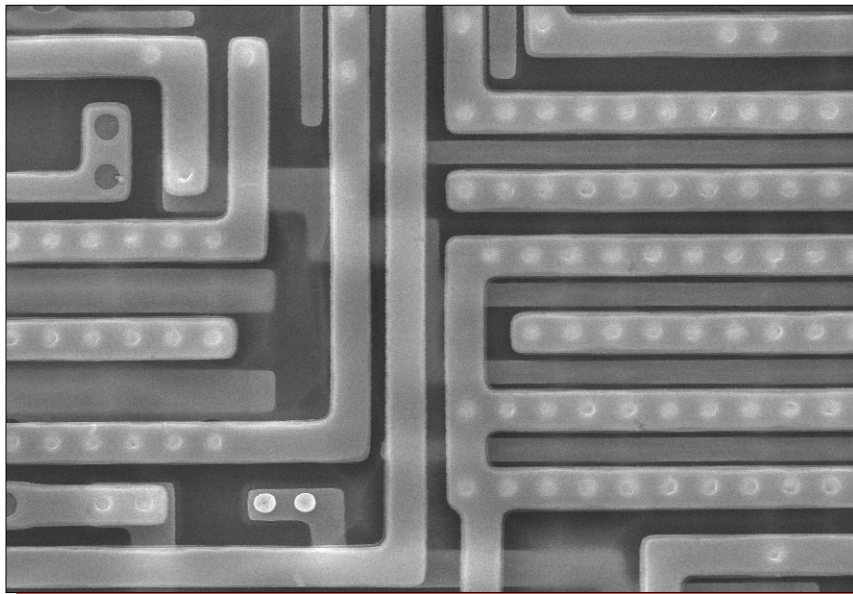


Mag. 13,000x

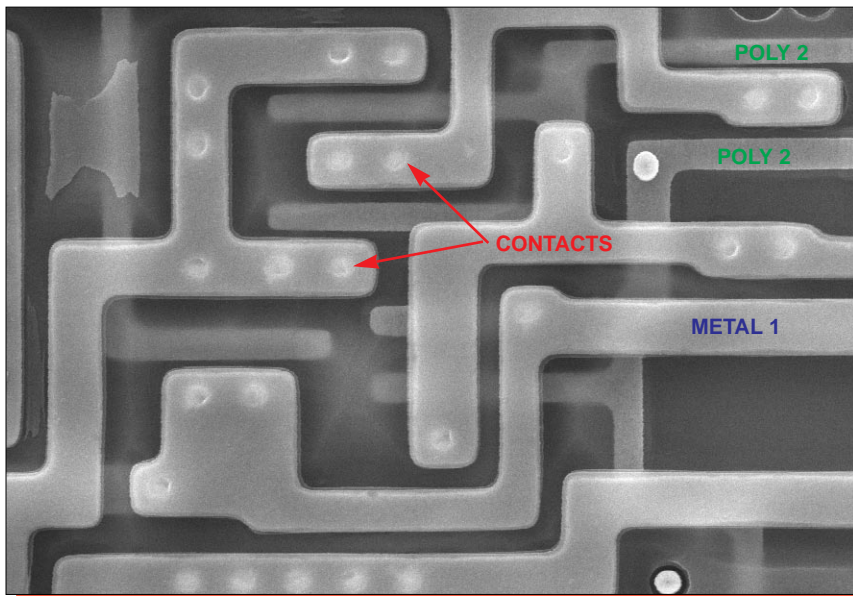


Mag. 34,000x

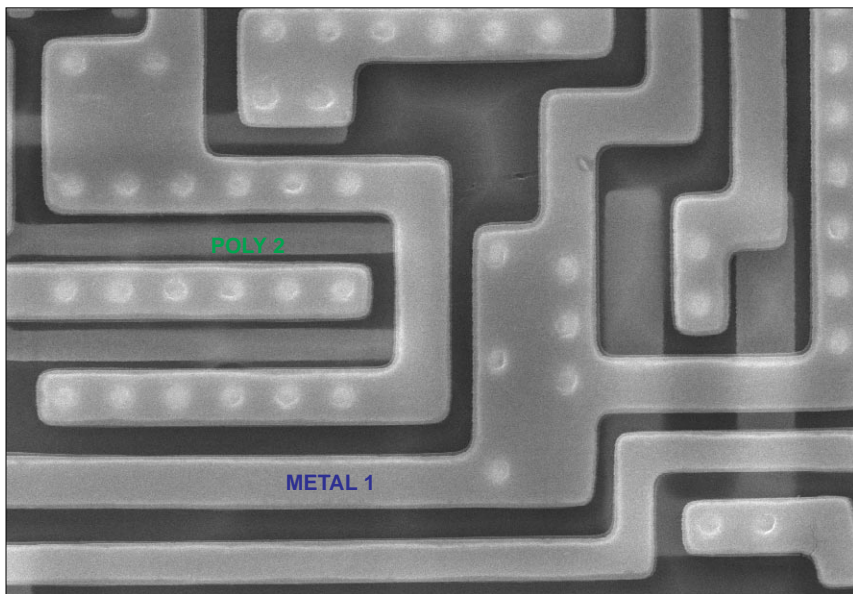
Figure 14. SEM section views of metal 1 line profiles.



Mag. 3500x

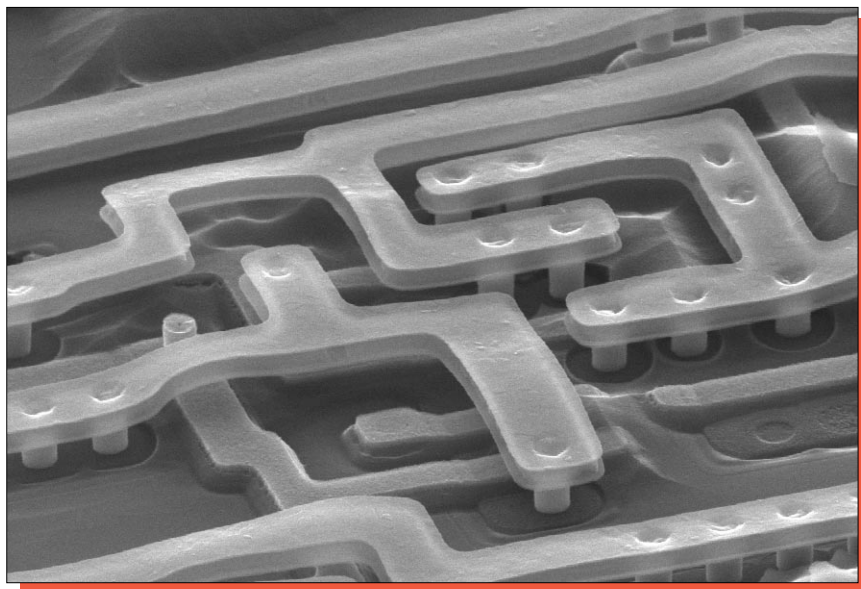


Mag. 5000x

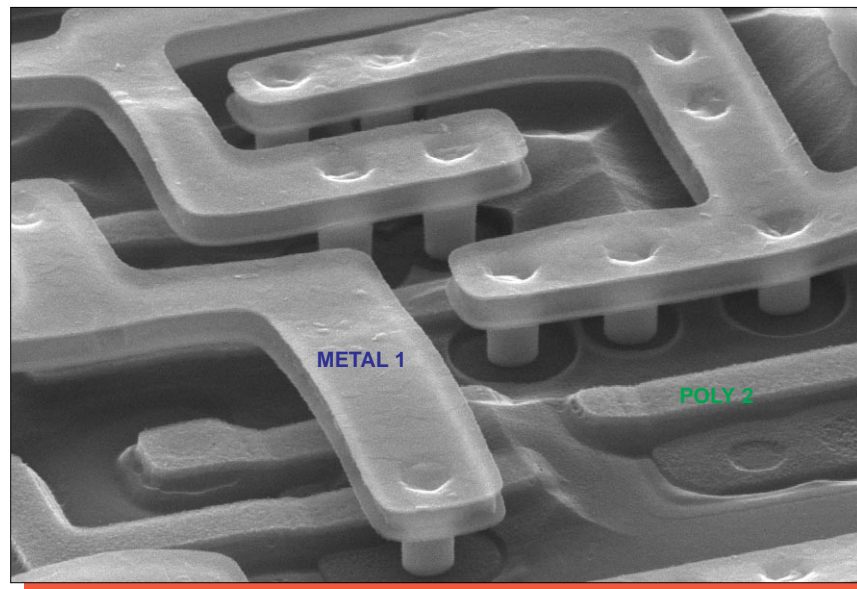


Mag. 5000x

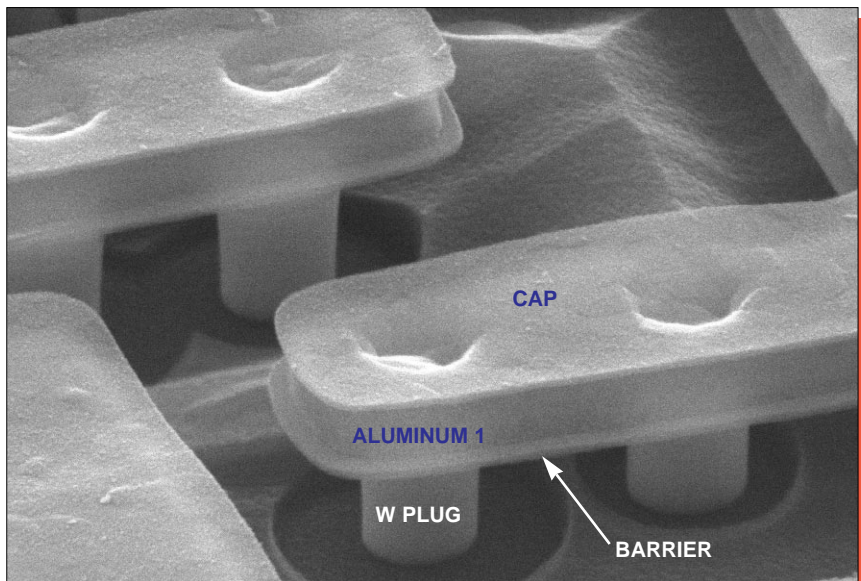
Figure 15. Topological views illustrating metal 1 patterning. 0°.



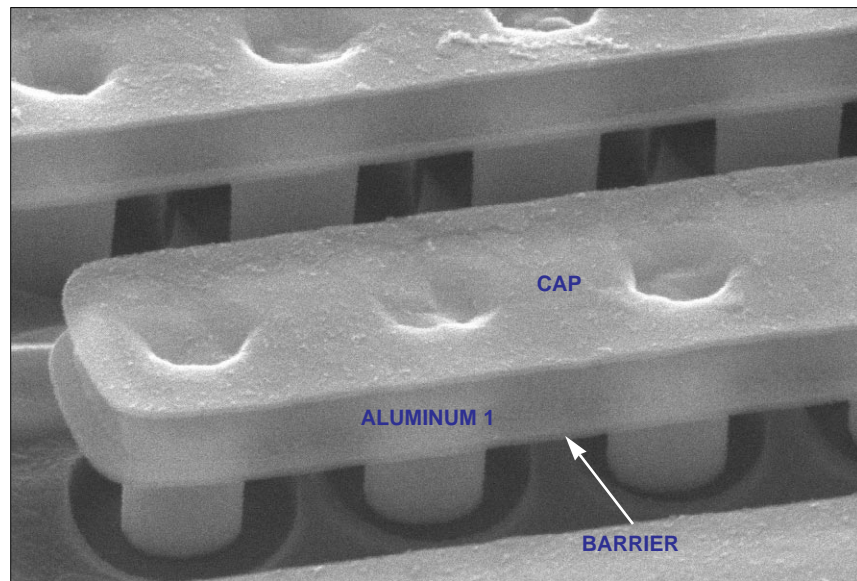
Mag. 6500x



Mag. 10,000x



Mag. 23,000x



Mag. 25,000x

Figure 16. SEM views of general metal 1 integrity. 60°.

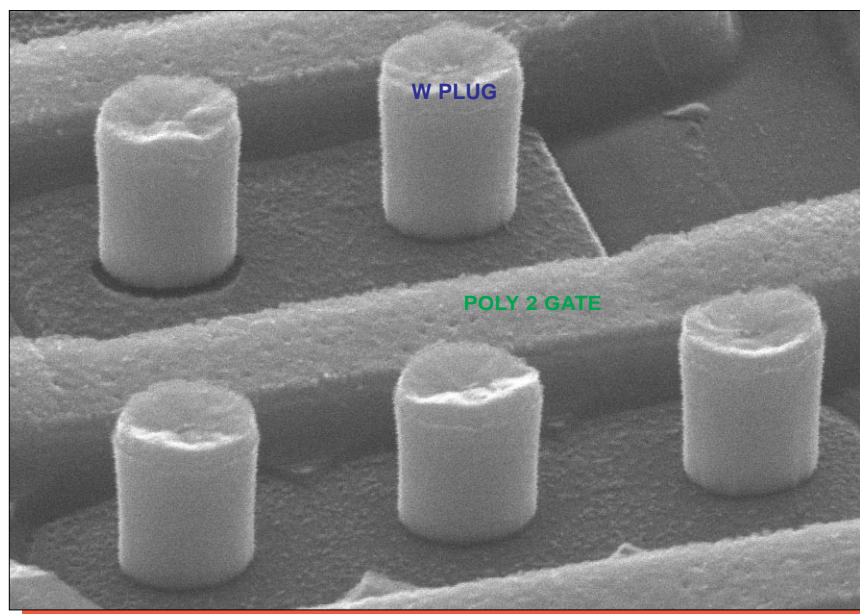
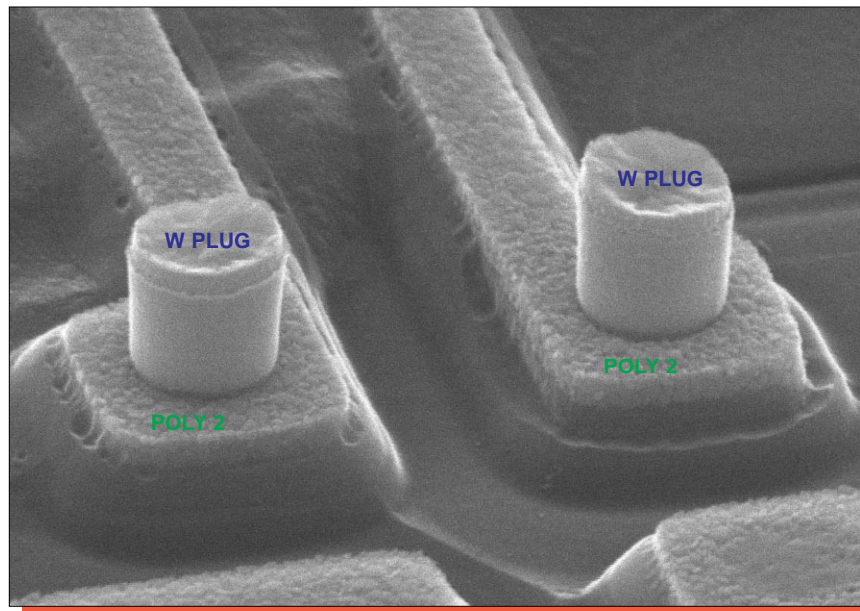
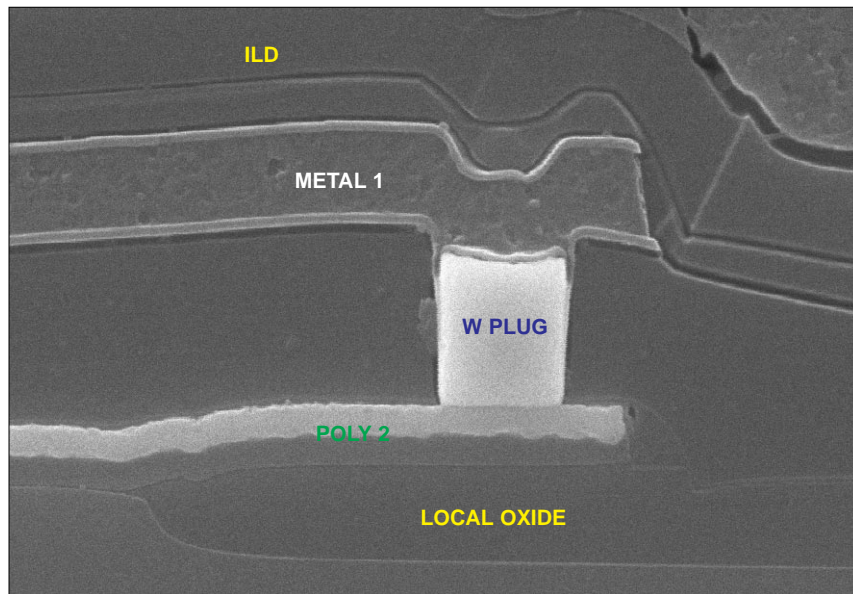
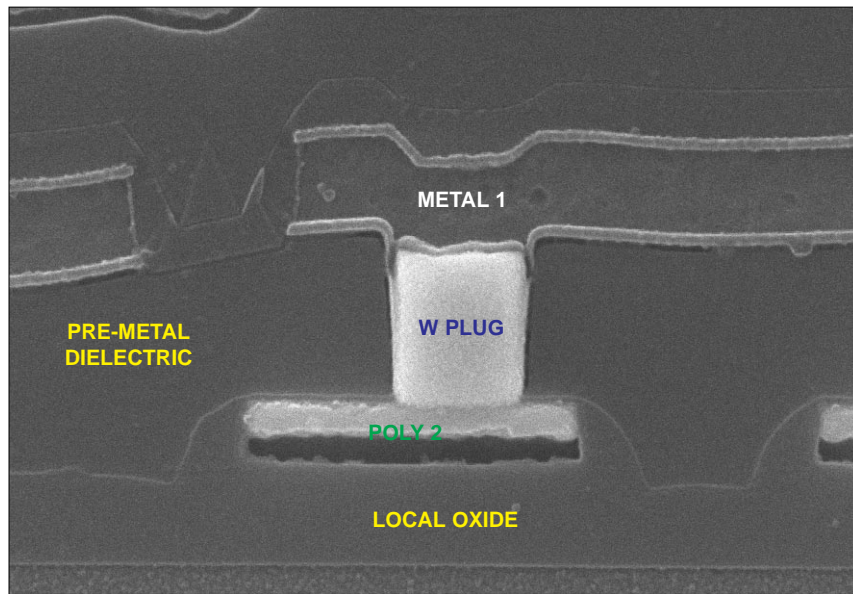


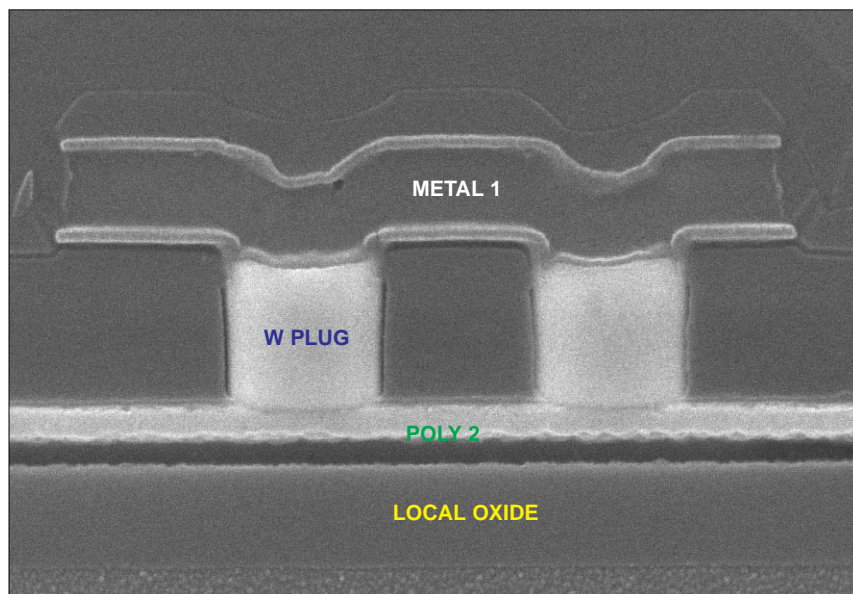
Figure 17. SEM views of metal 1 tungsten plugs. Mag. 30,000x, 60°.



glass-etch,
Mag. 26,000x

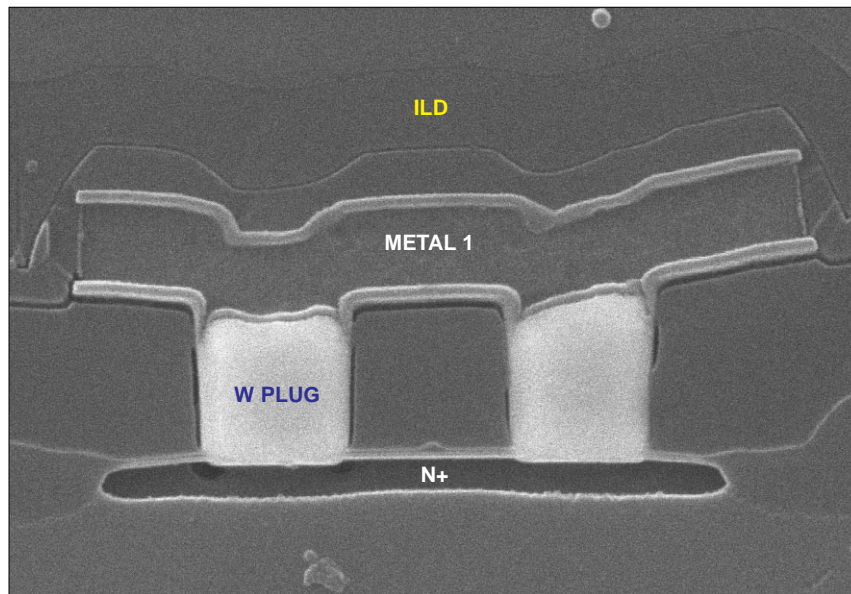


Mag. 26,000x

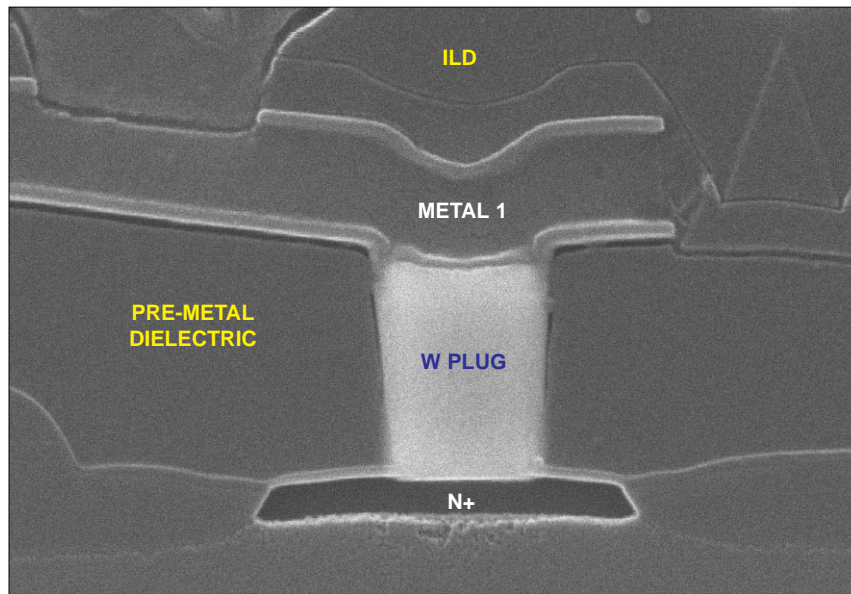


Mag. 25,000x

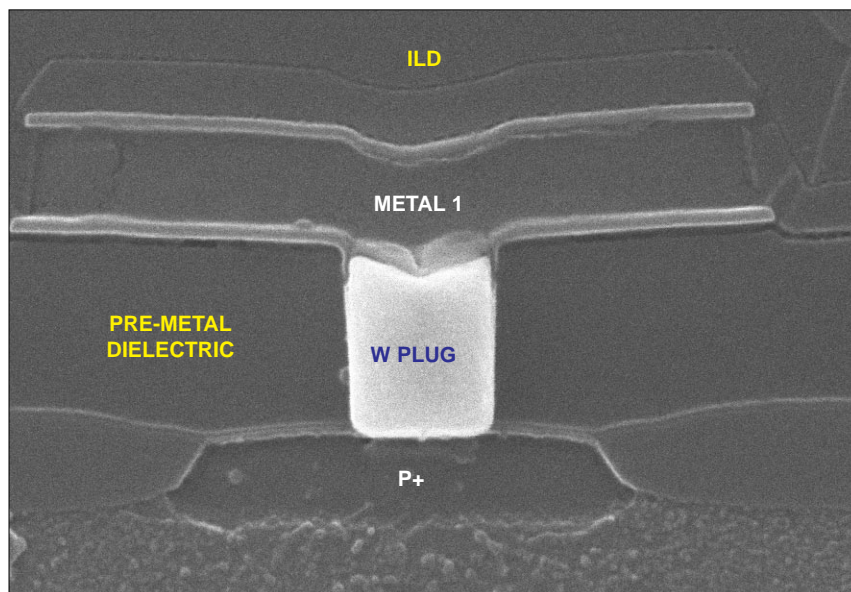
Figure 18. SEM section views of metal 1-to-poly 2 contacts.



metal 1-to-N+,
Mag. 25,000x

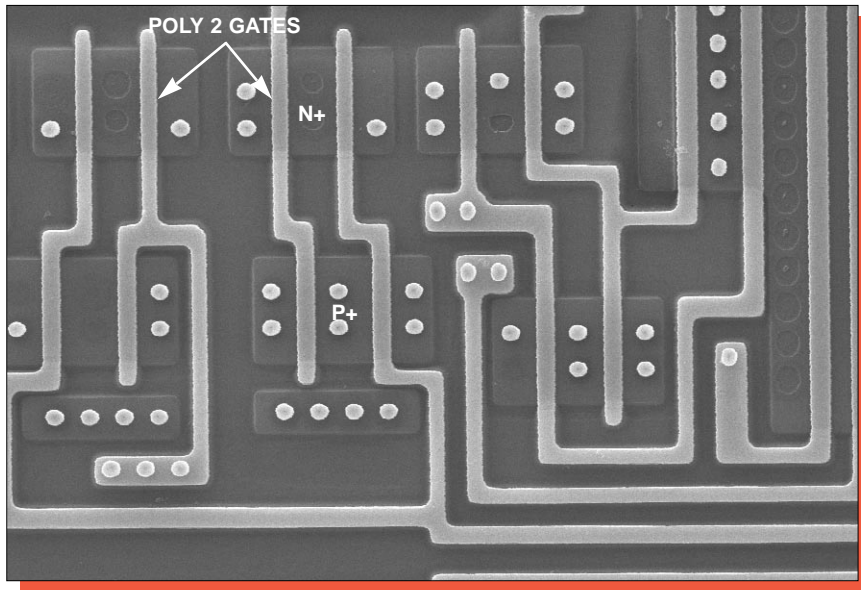


metal 1-to-N+,
Mag. 30,000x

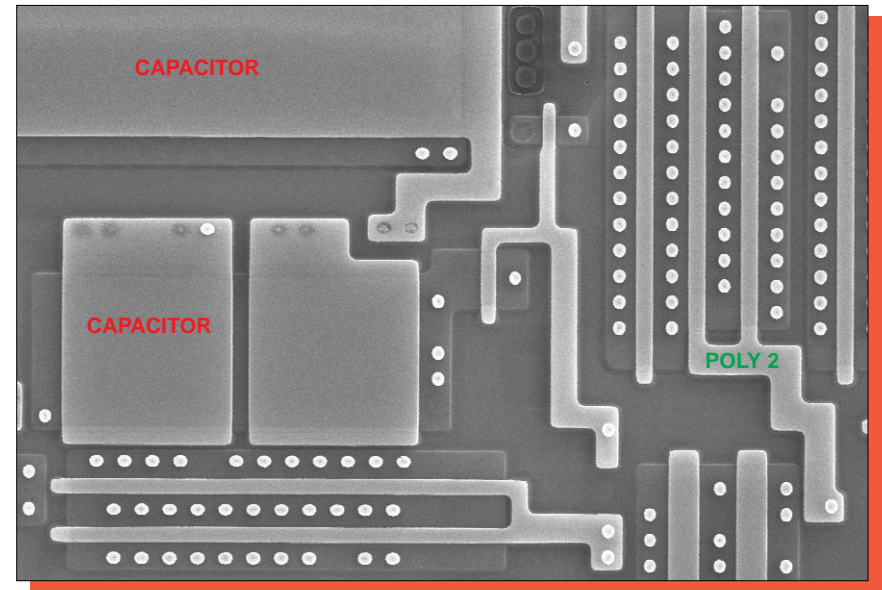


metal 1-to P+,
Mag. 30,000x

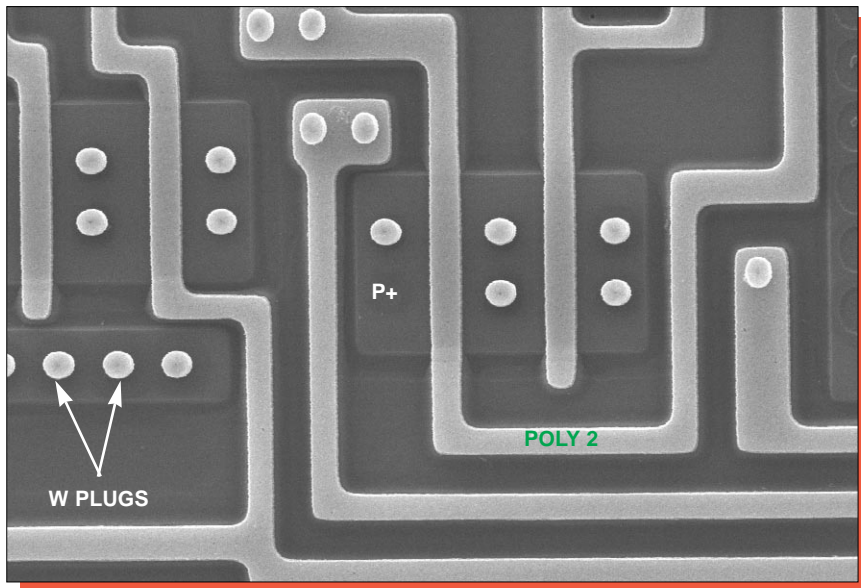
Figure 19. SEM section views of metal 1-to-diffusion contacts.



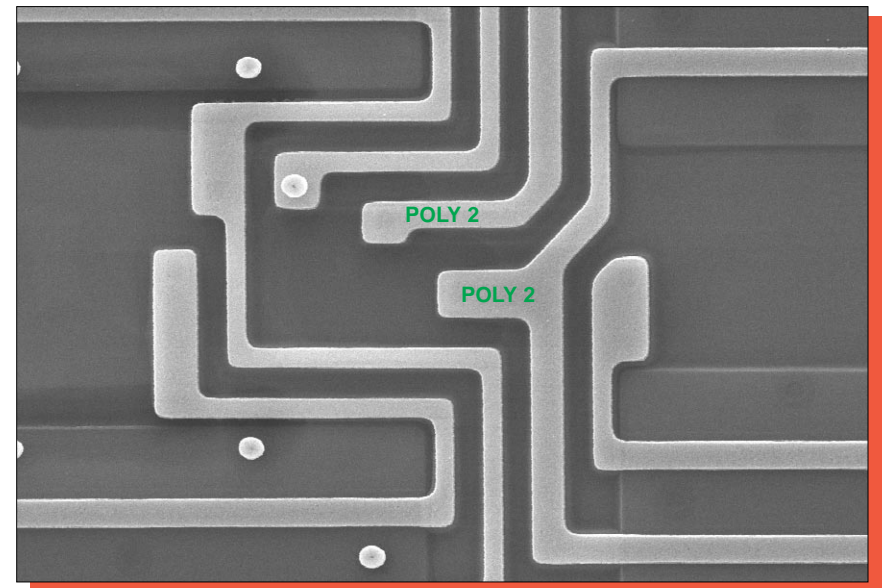
Mag. 3000x



Mag. 2200x

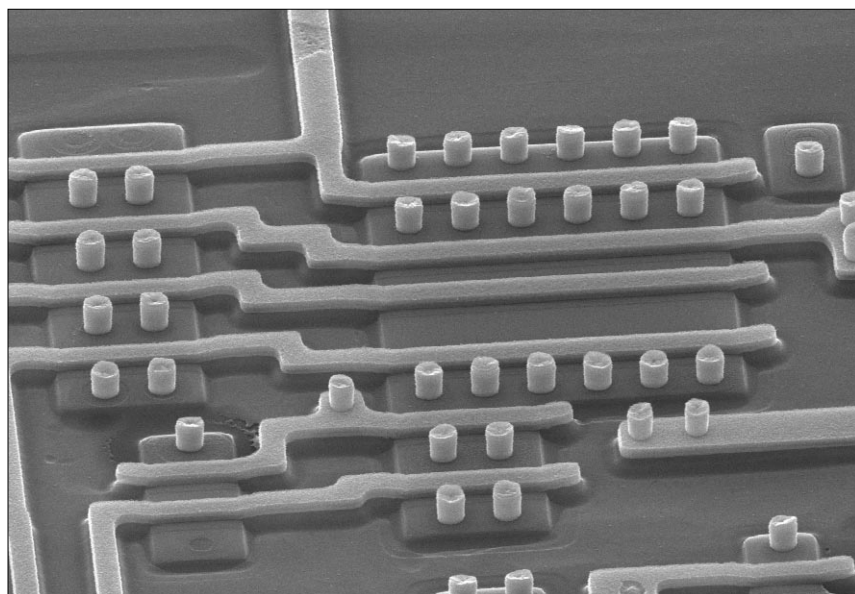


Mag. 5000x

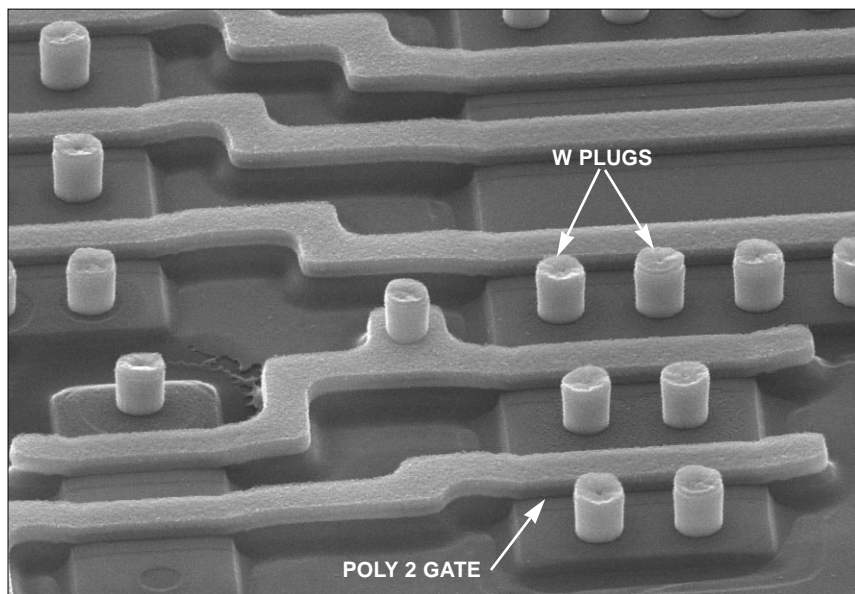


Mag. 4000x

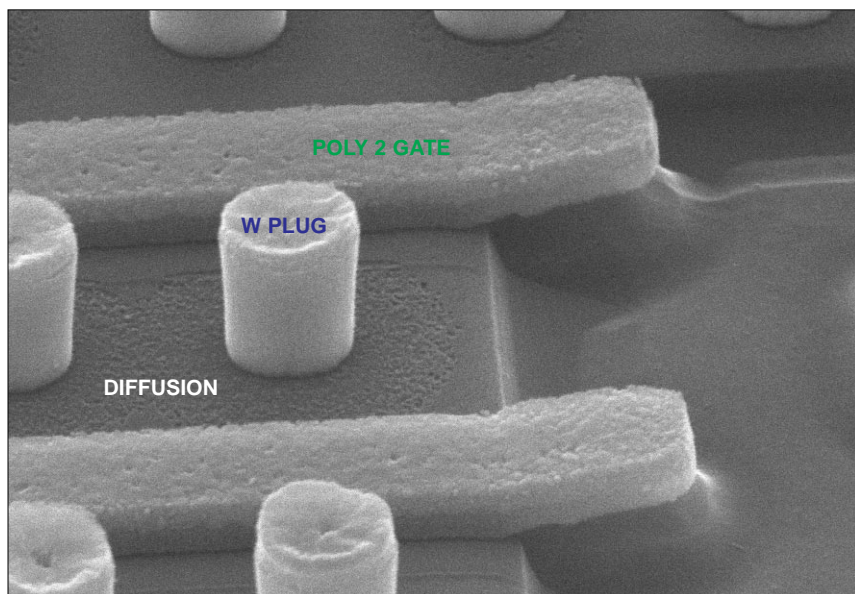
Figure 20. Topological SEM views illustrating poly 2 patterning. 0°.



Mag. 4600x

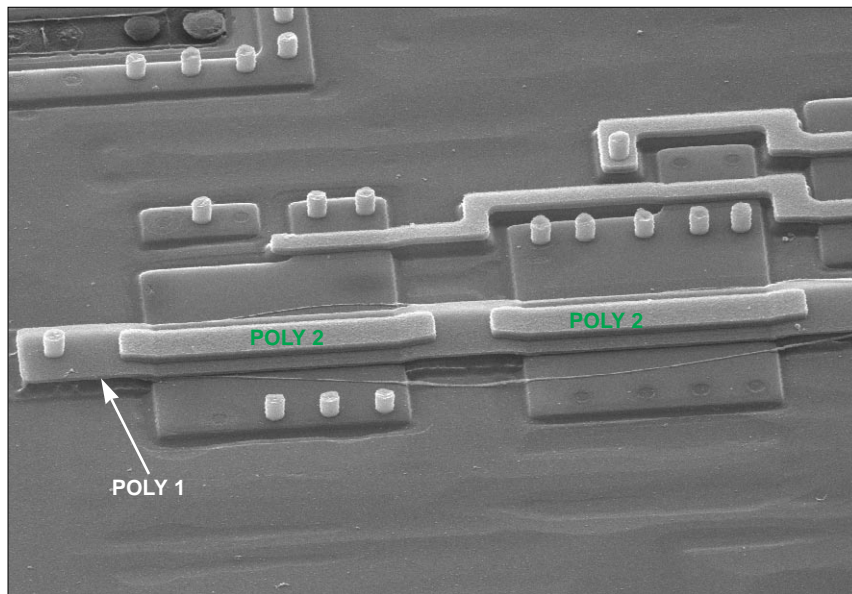


Mag. 8000x

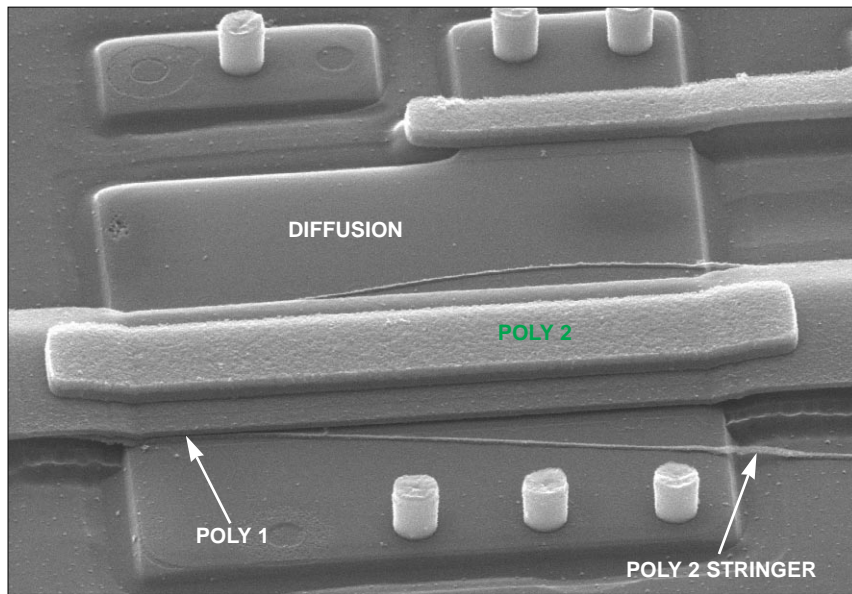


Mag. 24,000x

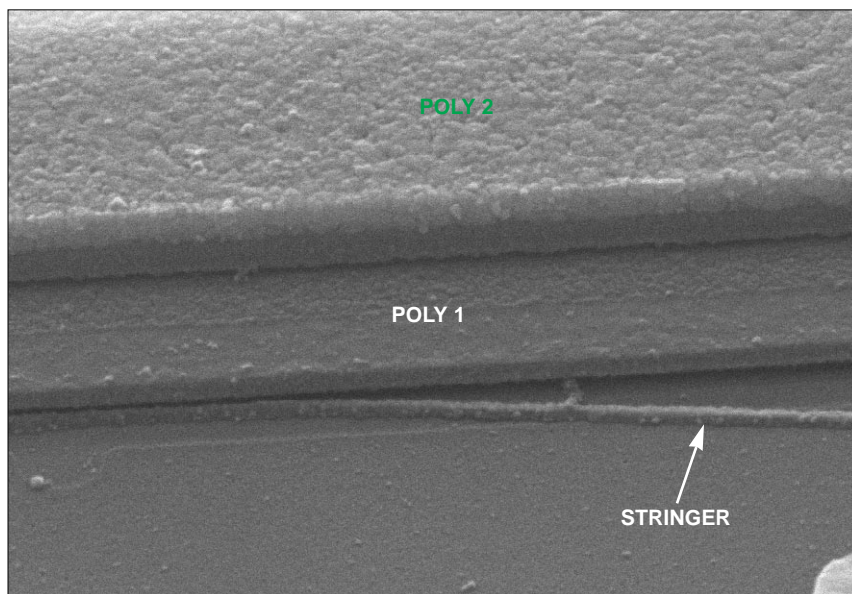
Figure 21. Perspective SEM views of poly 2 coverage. 55°.



Mag. 3500x

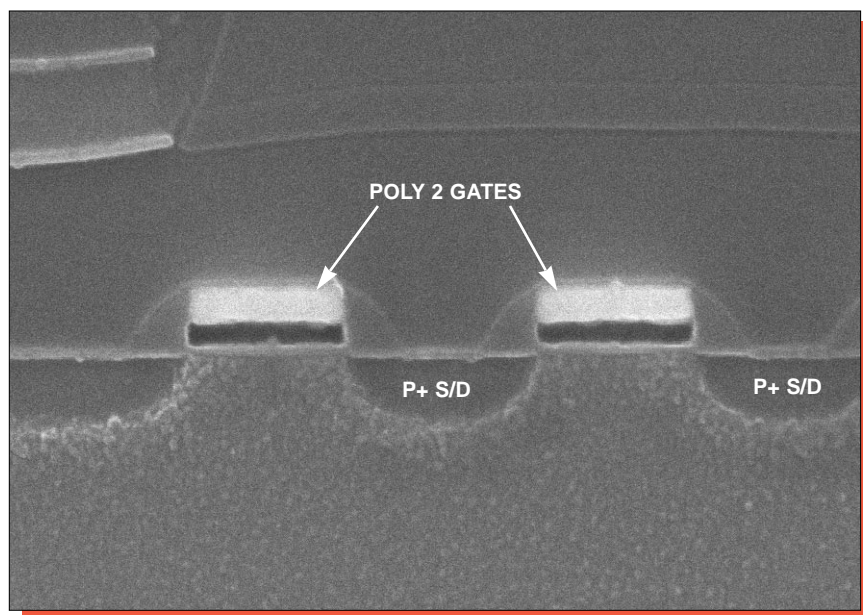


Mag. 8000x

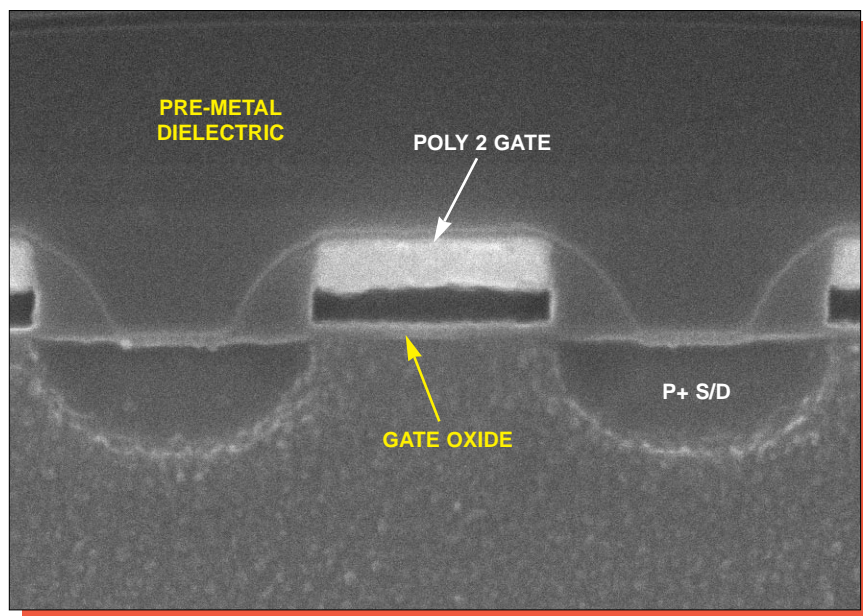


Mag. 30,000x

Figure 22. SEM views of a double poly transistor. 55°.

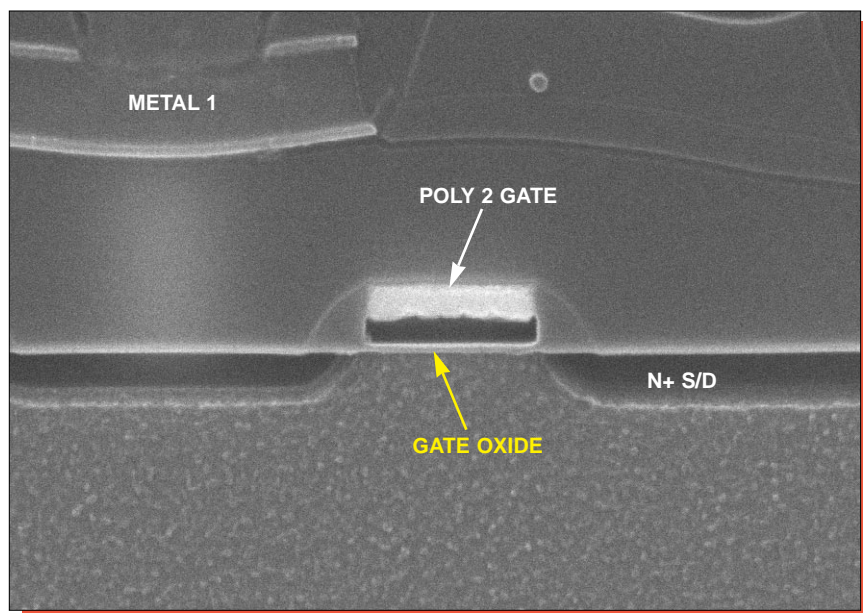


Mag. 26,000x

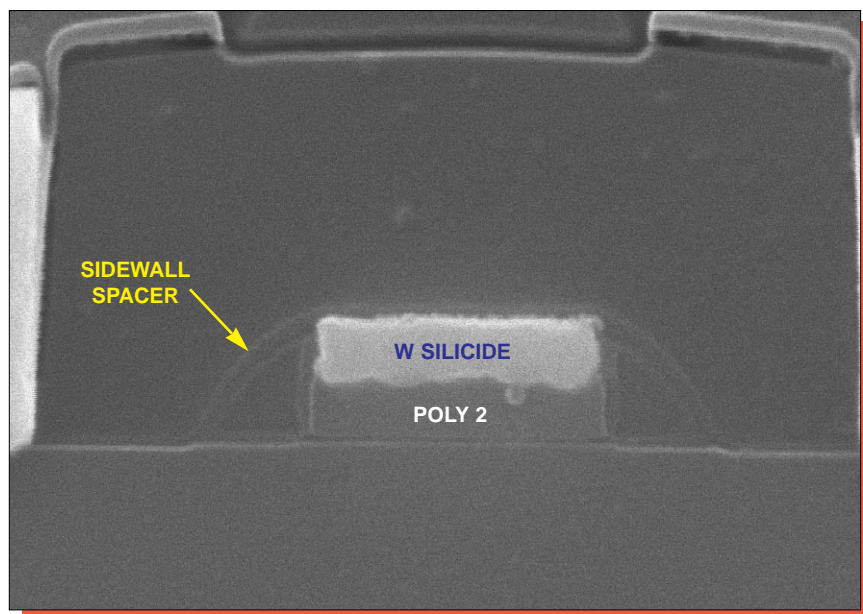


Mag. 40,000x

Figure 23. SEM section views of P-channel transistors.



Mag. 26,000x



glass etch, Mag. 52,000x

Figure 24. SEM section views of N-channel transistors.

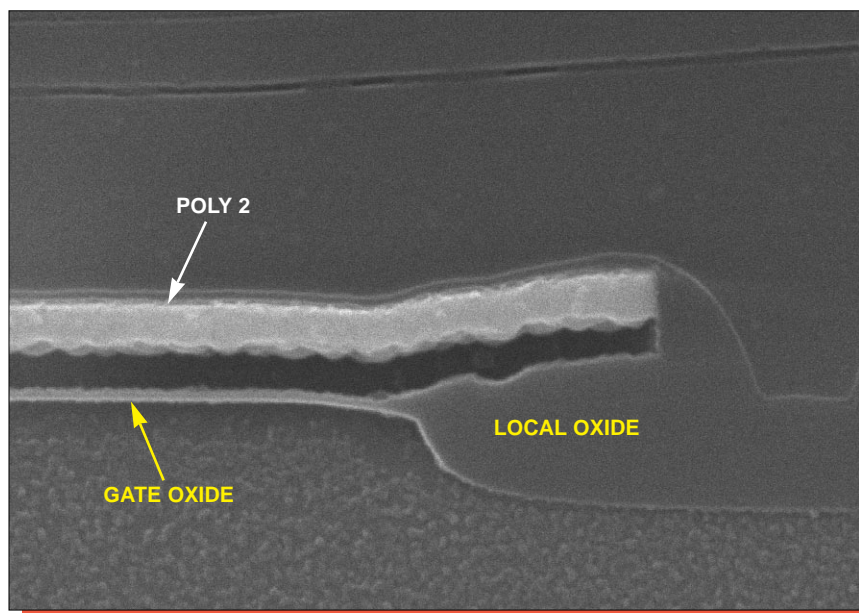


Figure 25. SEM section view of a local oxide birdsbeak. Mag. 40,000x.

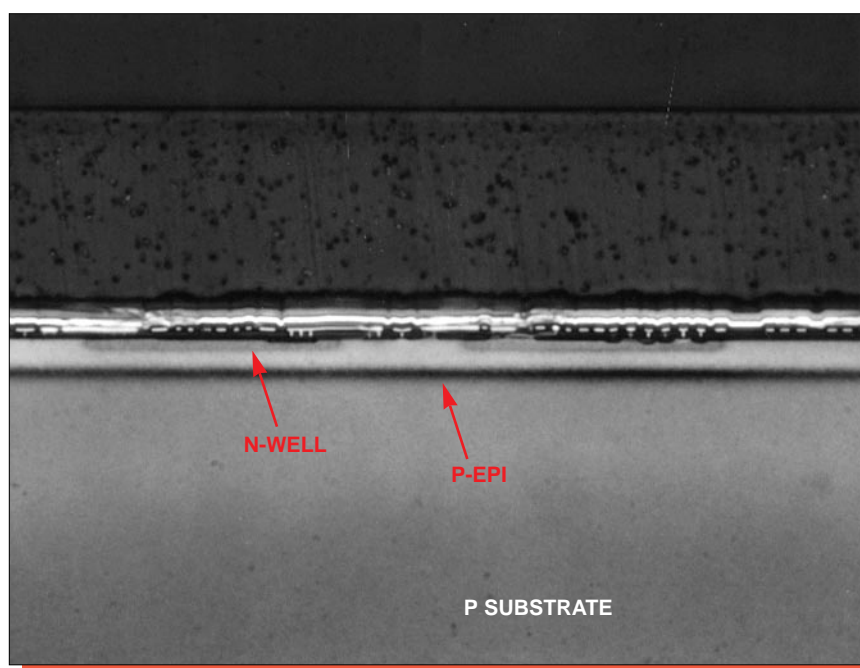
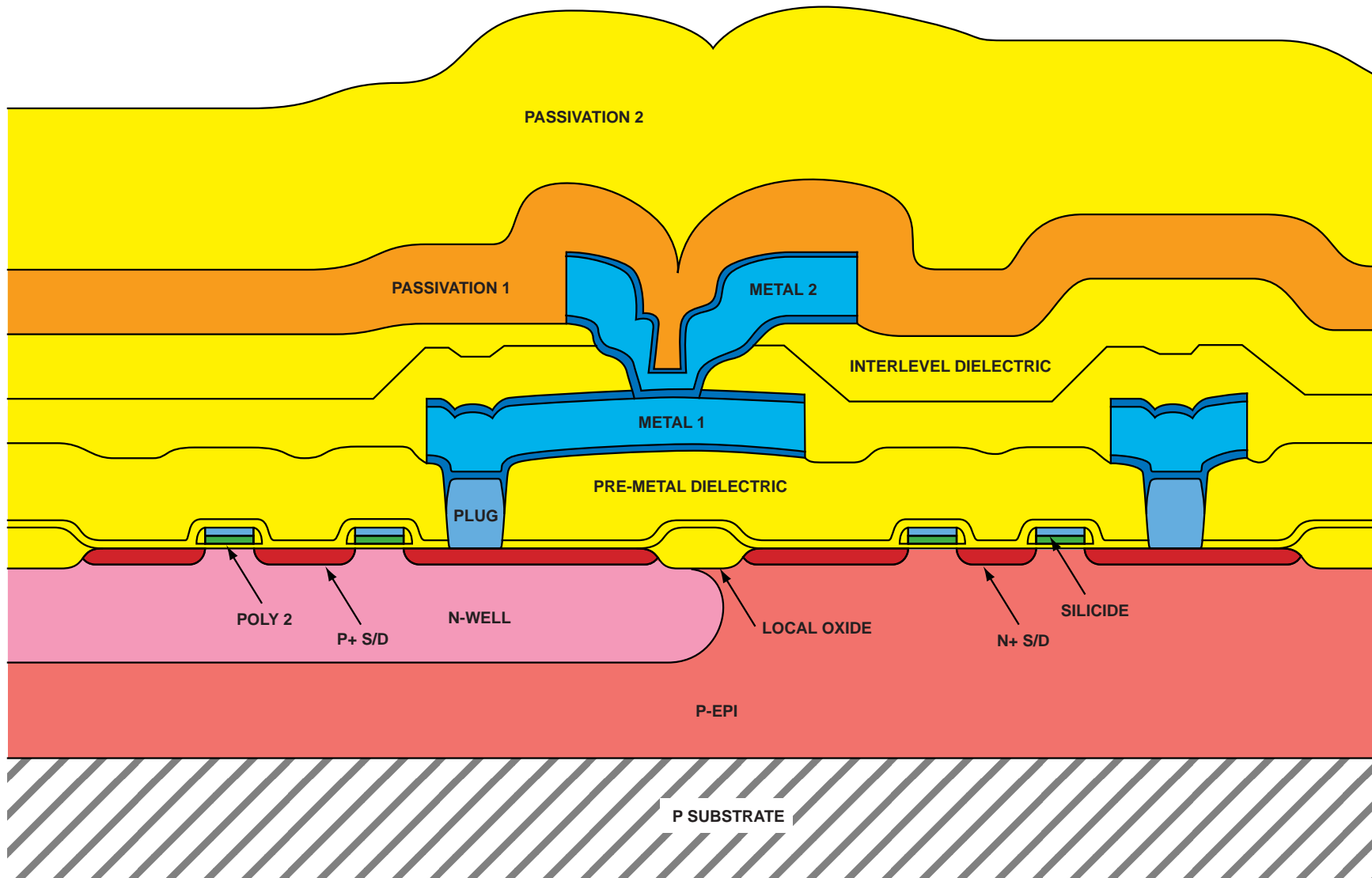


Figure 26. Optical section view of the well structure. Mag. 800x.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate

Figure 27. Color cross section drawing illustrating device structure.

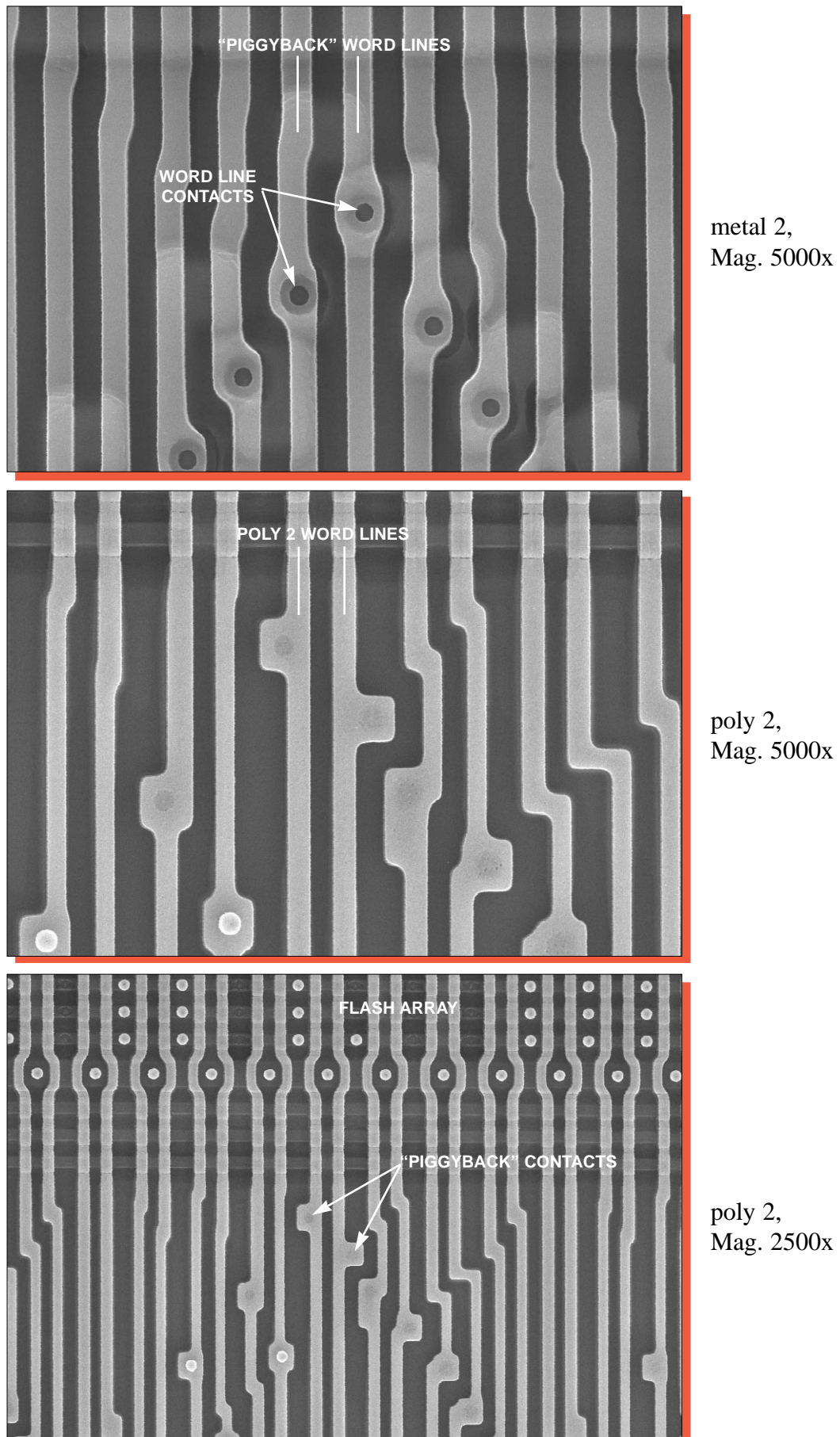


Figure 28. Topological SEM views of the Flash array illustrating "piggyback" word line connections. 0°.

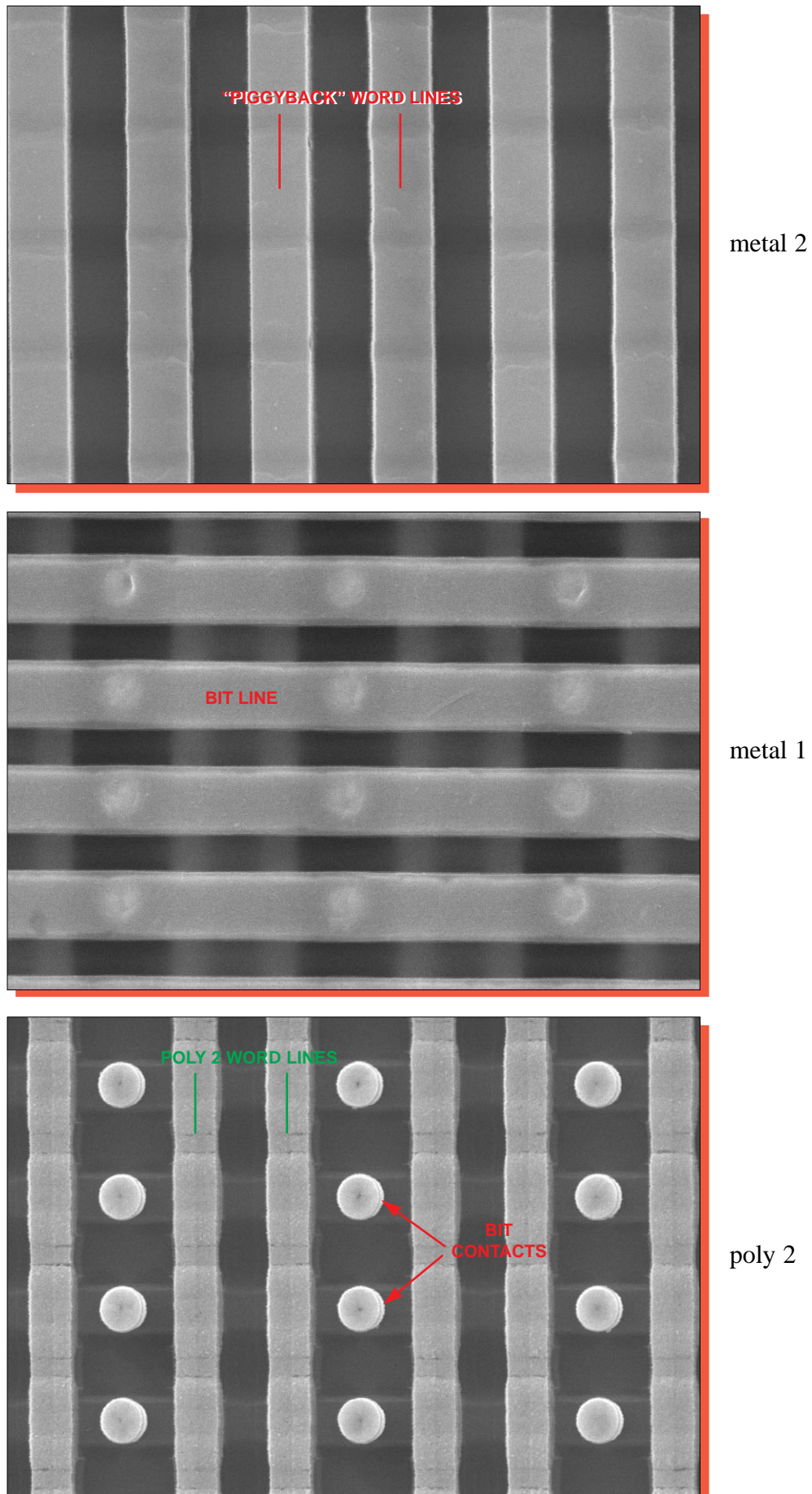
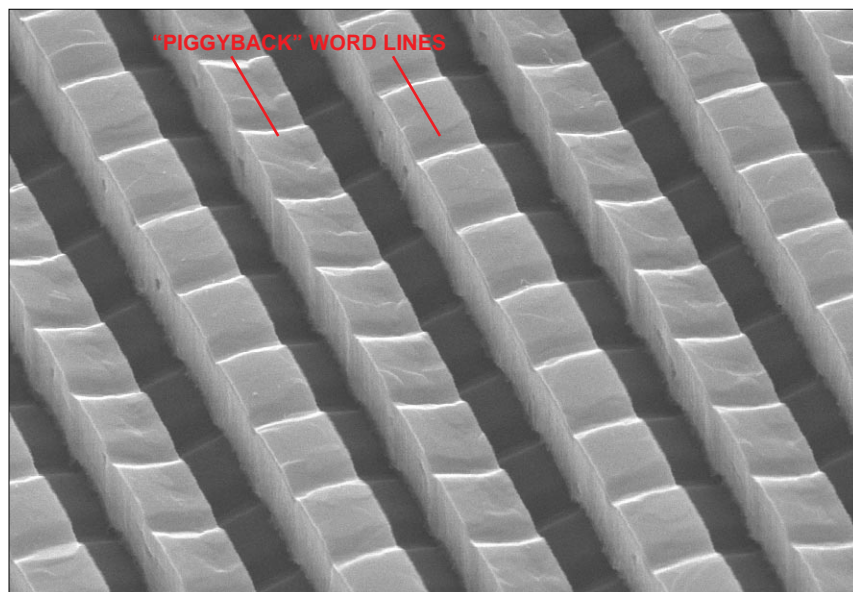
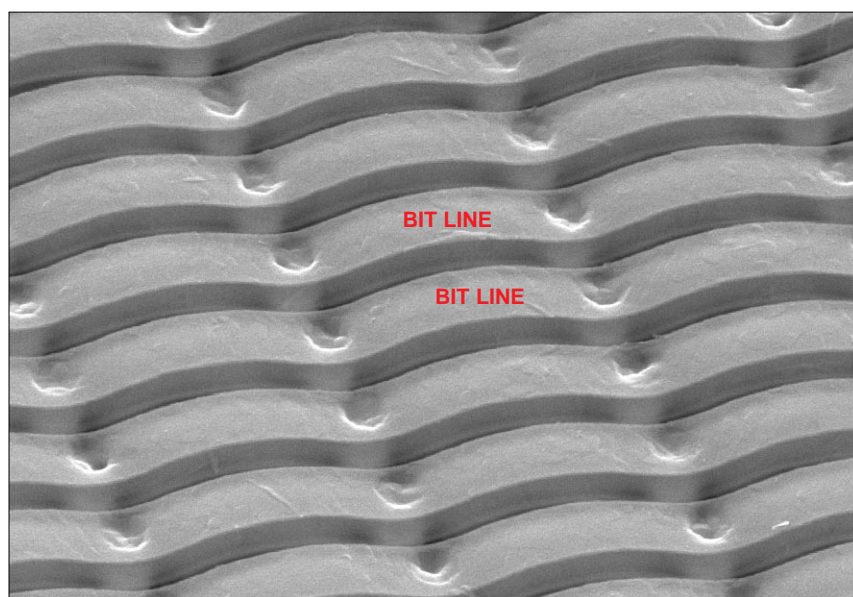


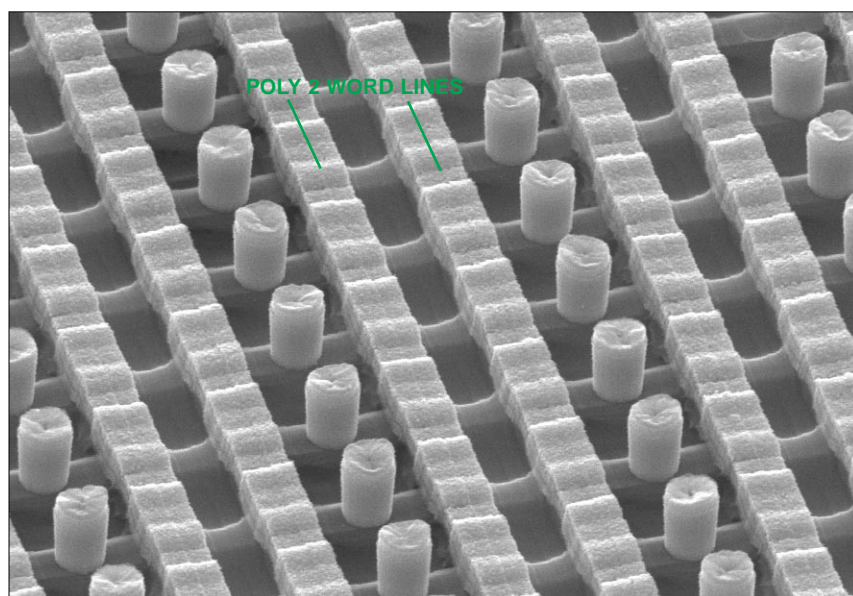
Figure 29. Topological SEM views of the Flash array. Mag. 10,000x, 0°.



metal 2

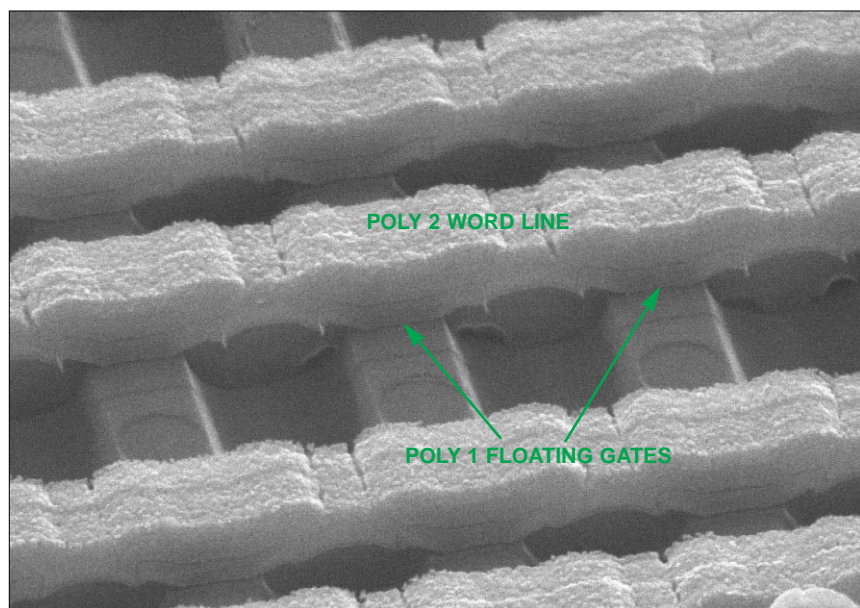


metal 1

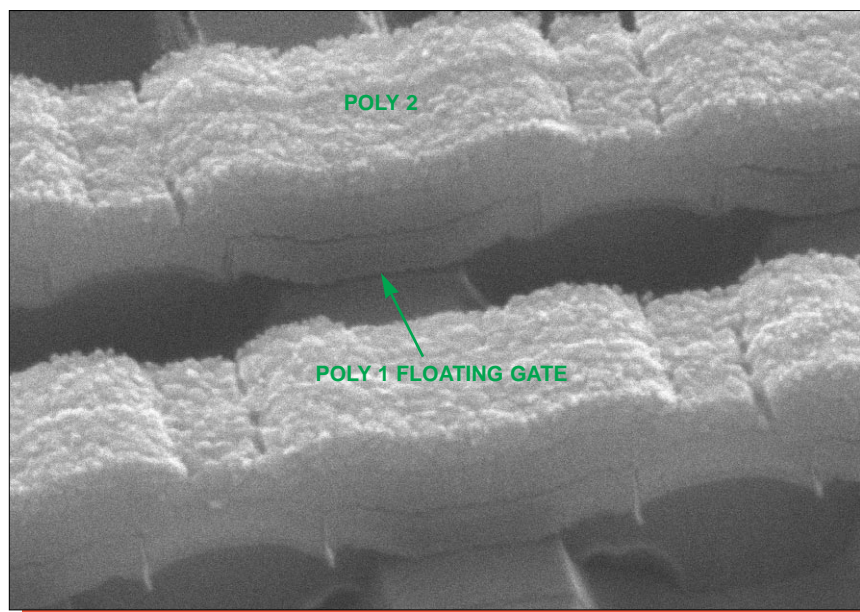


poly 2

Figure 30. Perspective SEM views of the Flash array. Mag. 10,000x, 55°.



Mag. 20,000x



Mag. 36,000x

Figure 31. Detail SEM views of the Flash array. Mag. 55°.

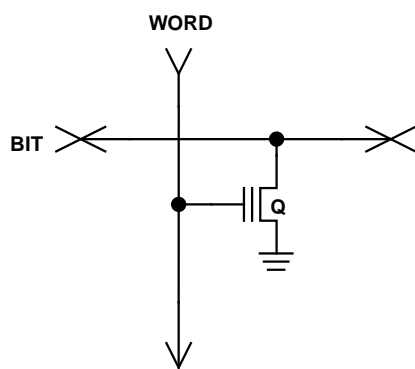
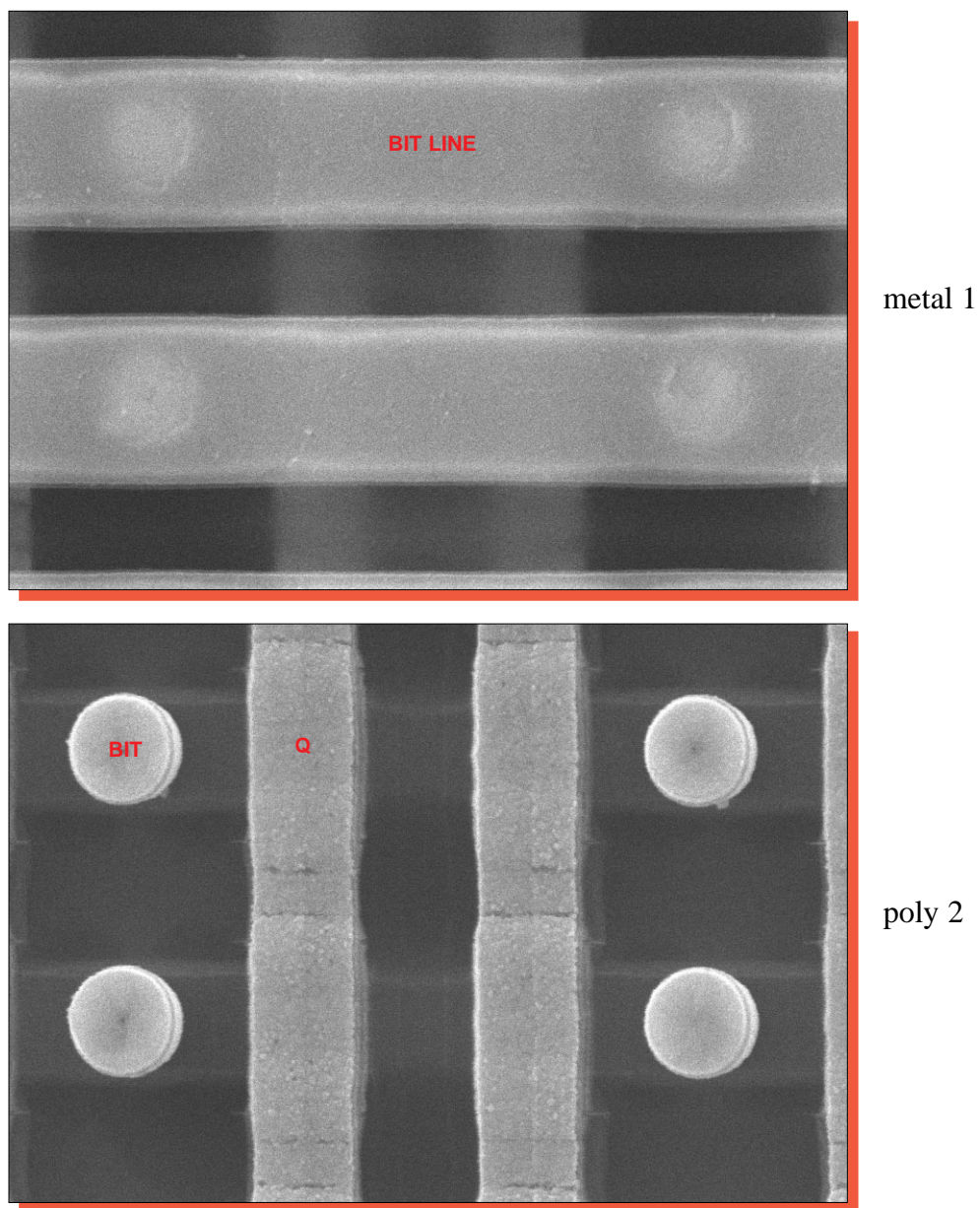
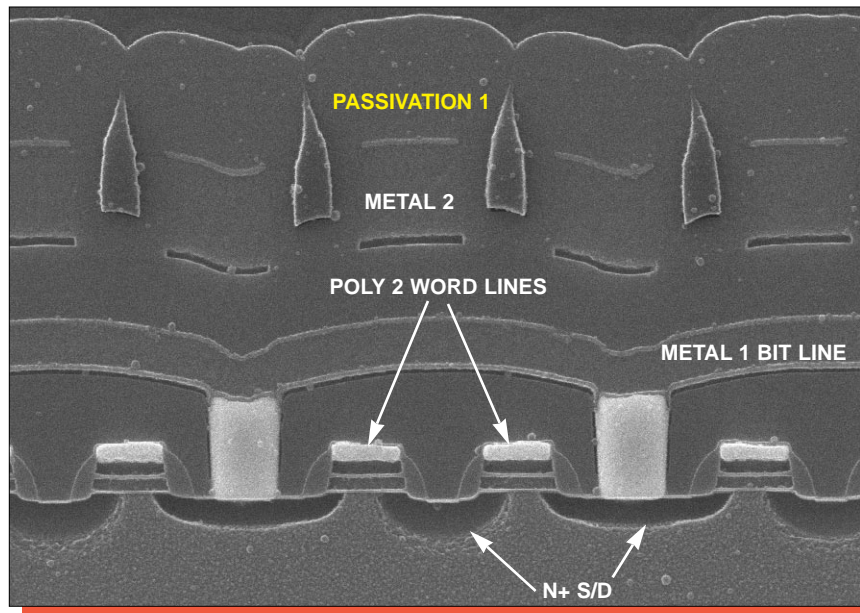
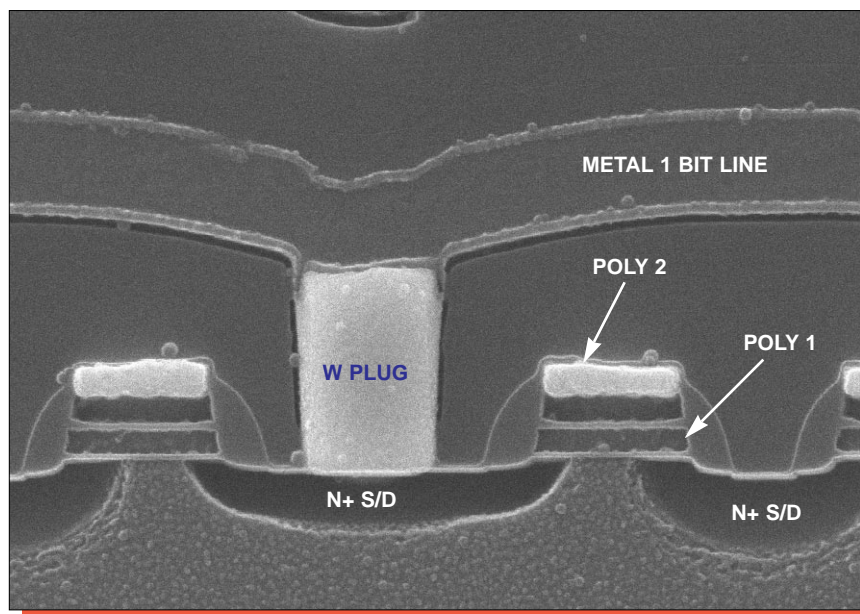


Figure 32. Topological SEM views of Flash cells with schematic. Mag. 20,000x, 0°.



Mag. 13,000x



Mag. 26,000x

Figure 33. SEM section views of Flash EEPROM cells(parallel to bit lines).

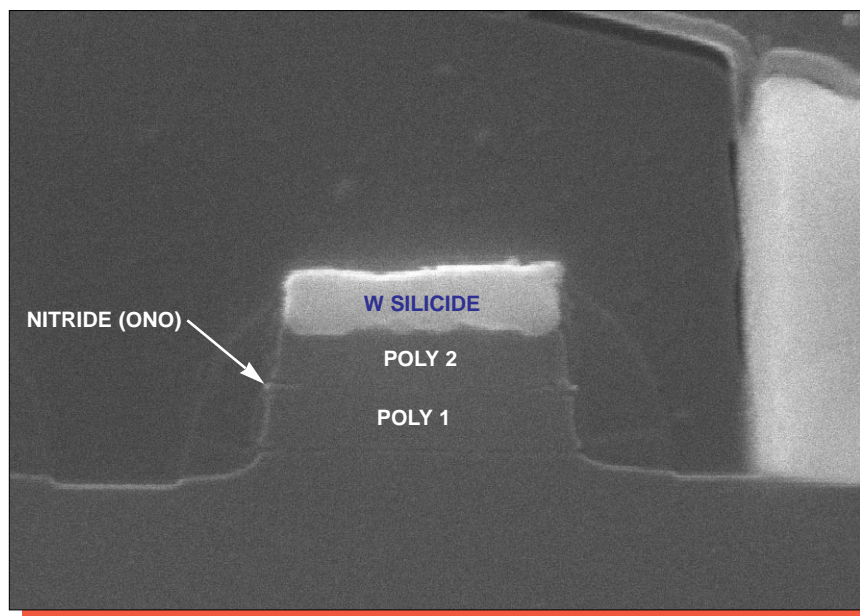
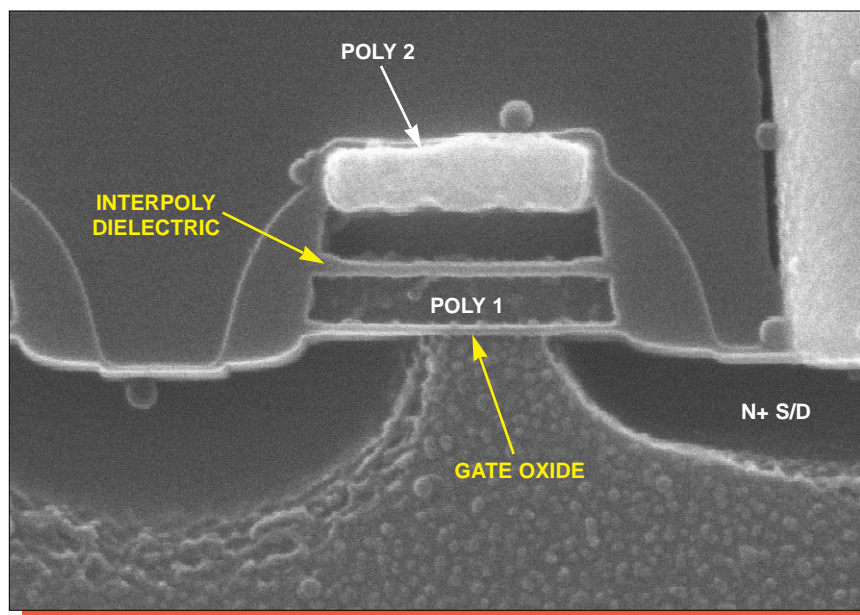
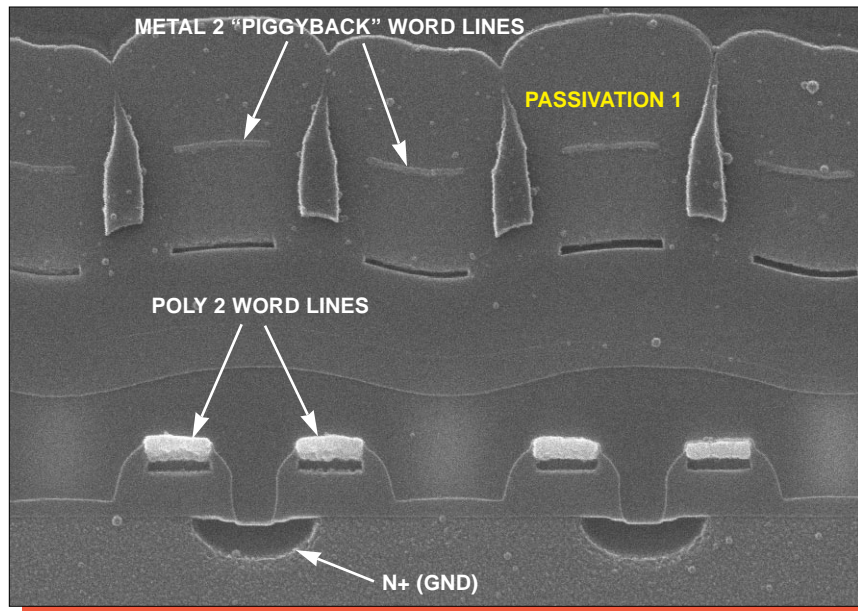
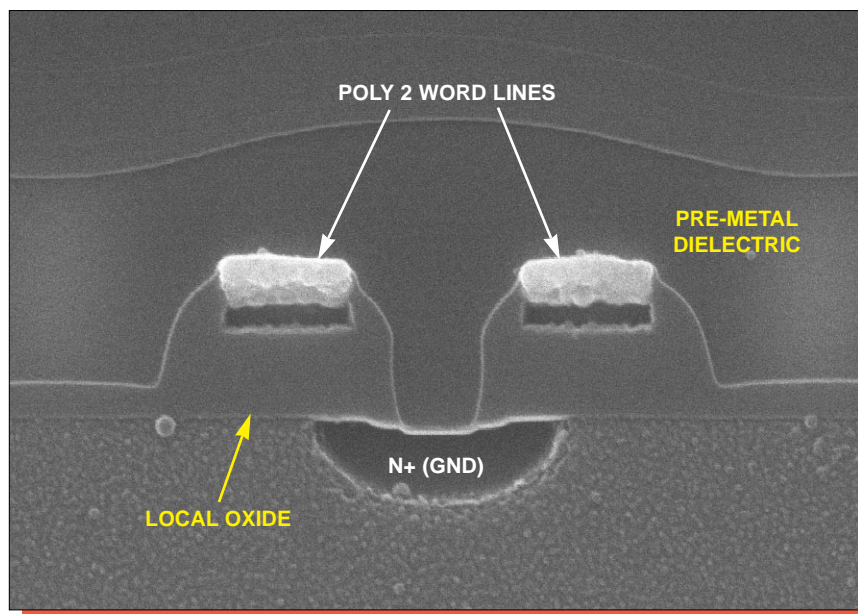


Figure 33a. SEM section details of an EEPROM cell. Mag. 52,000x.



Mag. 13,000x



Mag. 26,000x

Figure 34. SEM section views of the Flash EEPROM array (parallel to bit lines)

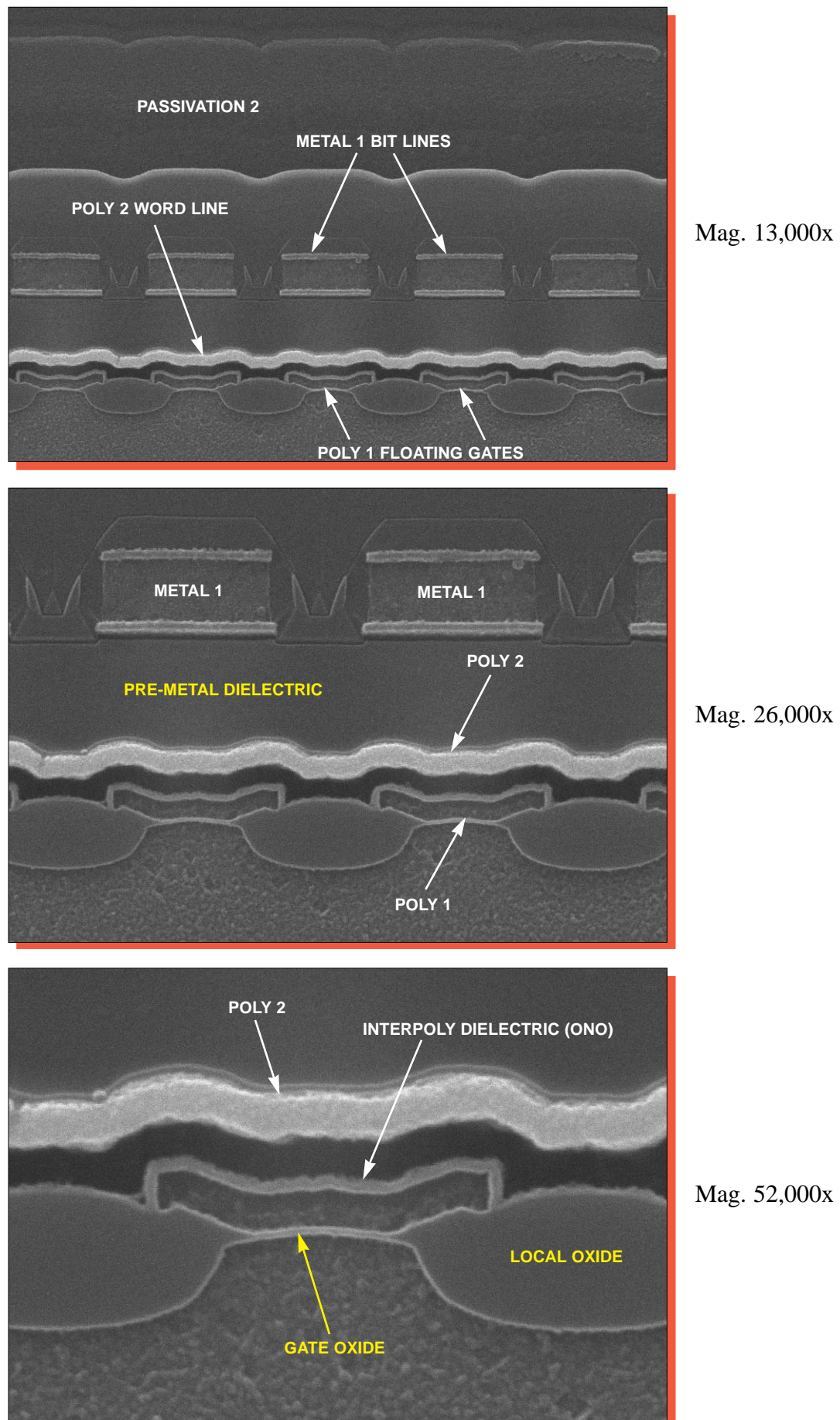
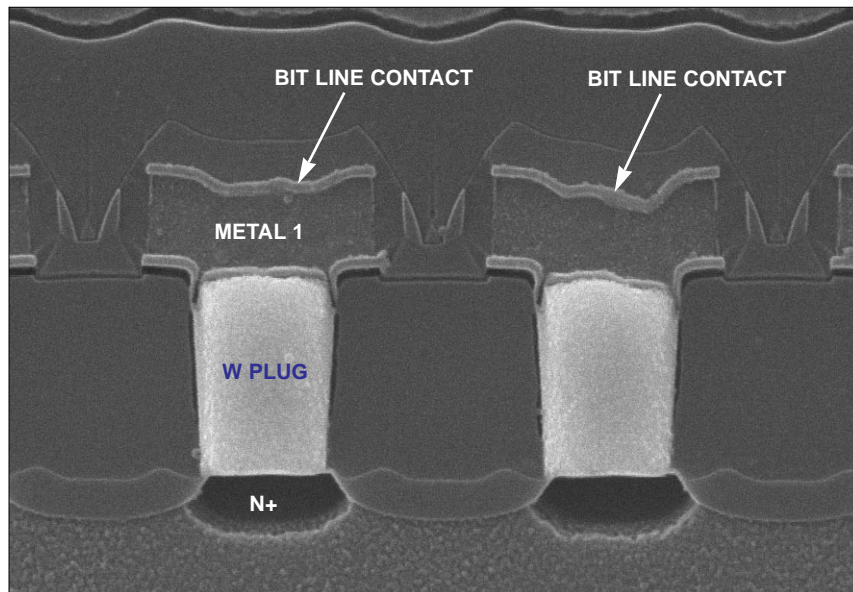
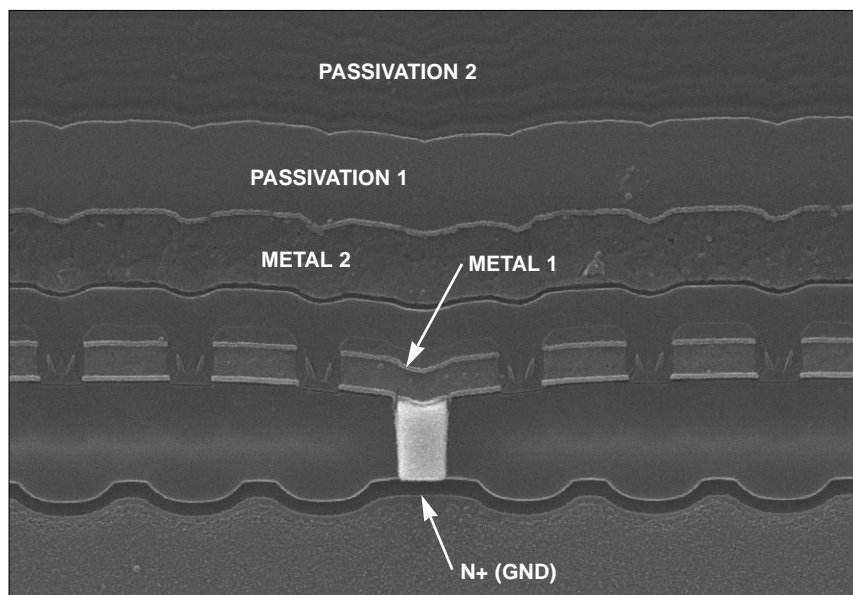


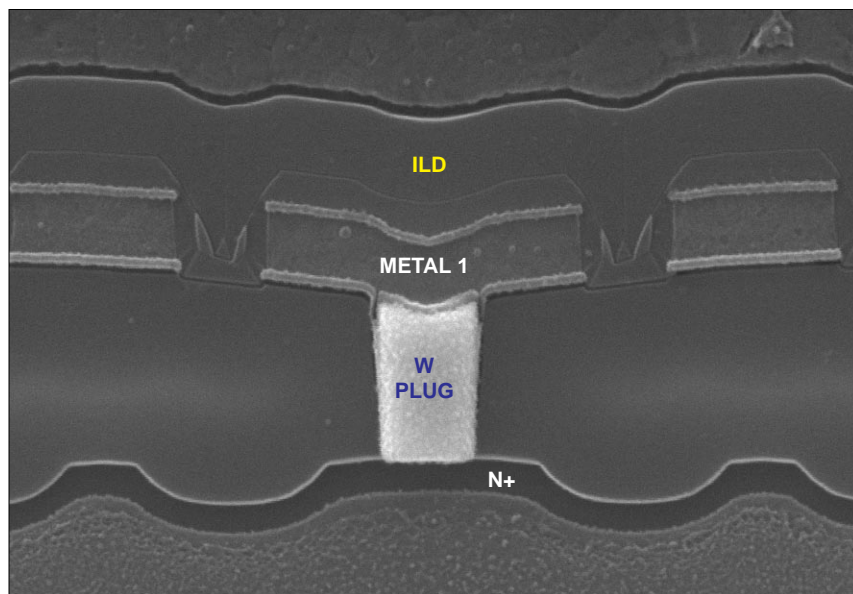
Figure 35. SEM section views of Flash EEPROM cells (parallel to word lines).



Mag. 26,000x



Mag. 10,000x



Mag. 20,000x

Figure 36. SEM section views of bit line contacts and GND connection in array (parallel to word lines).

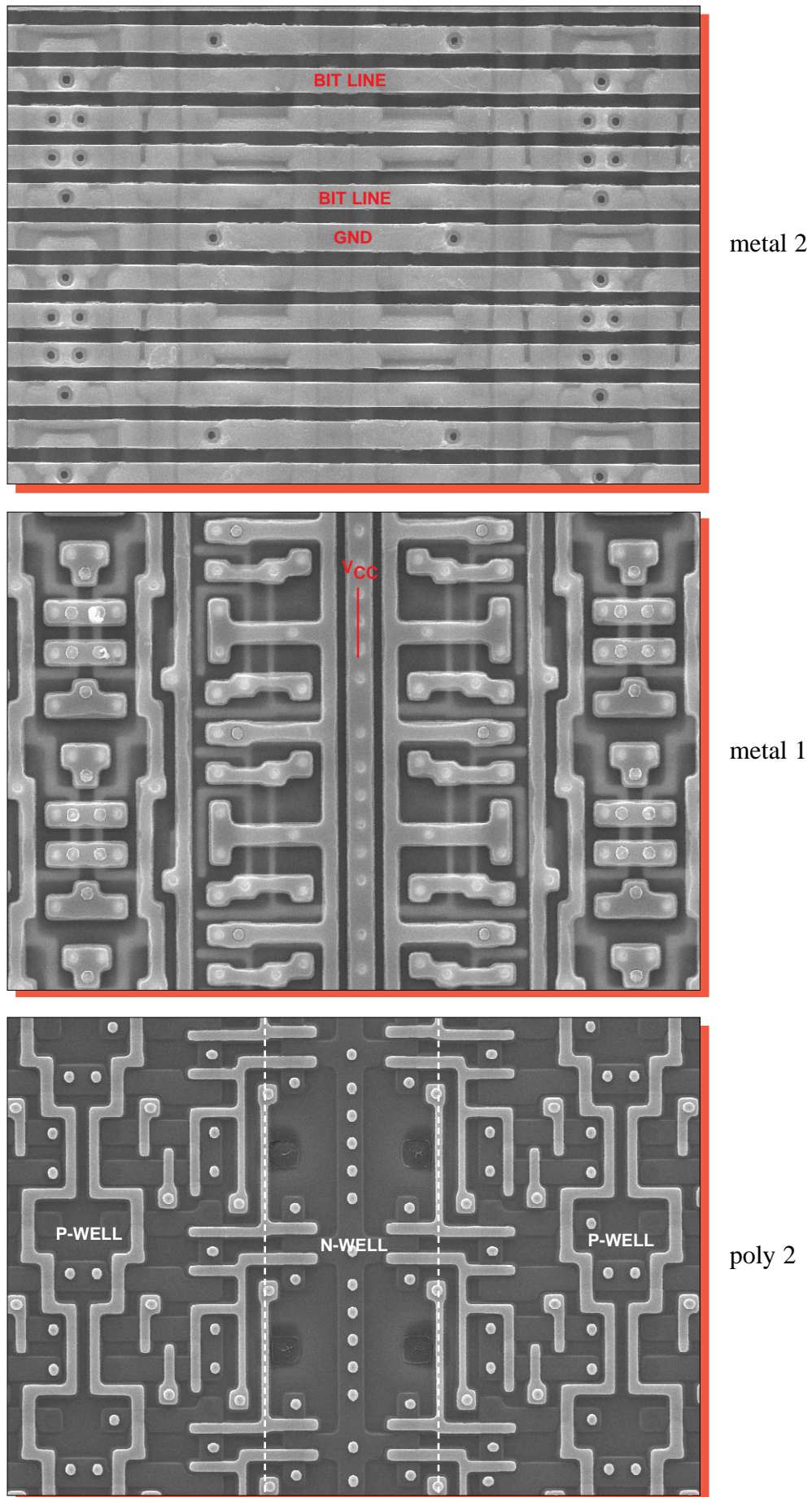
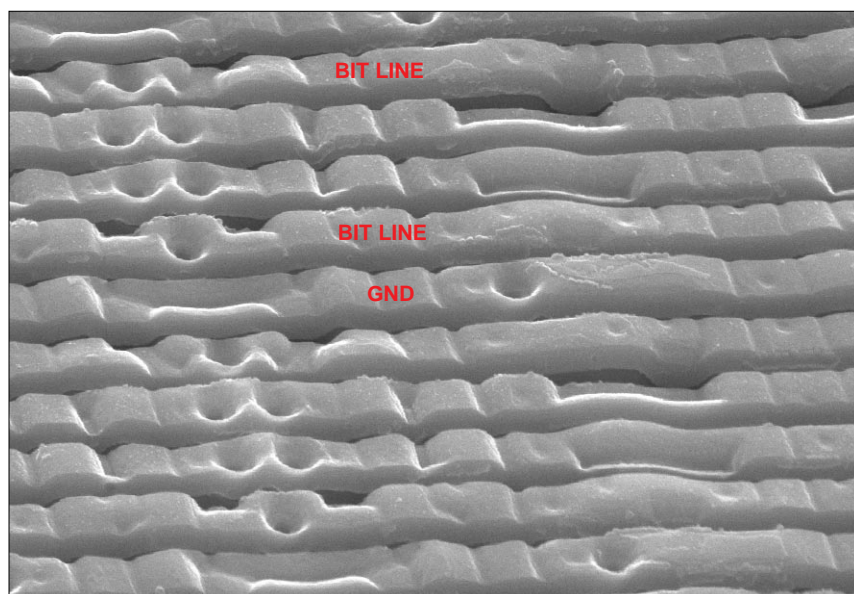
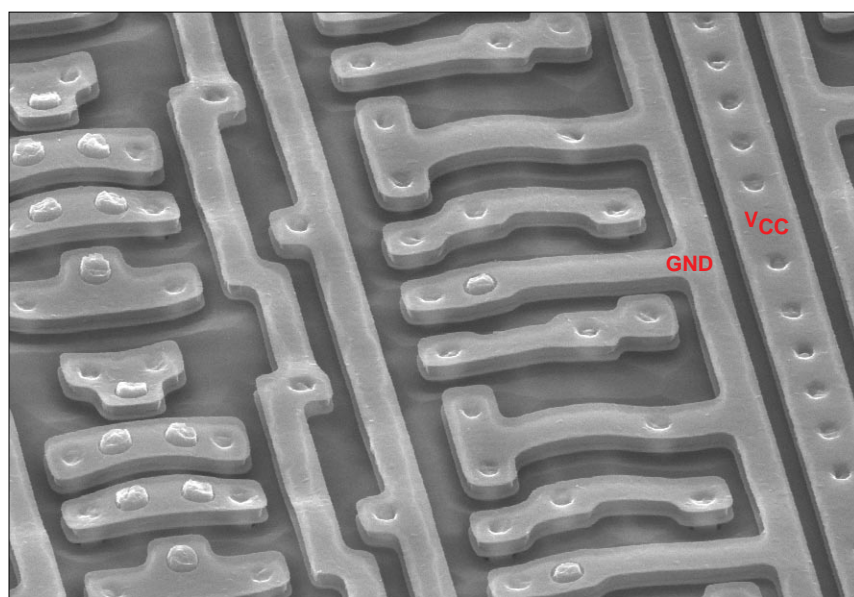


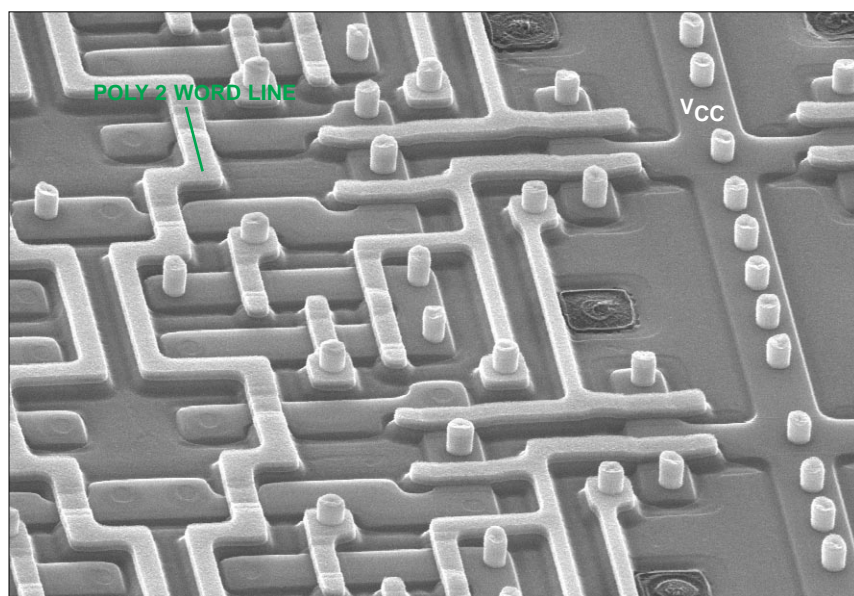
Figure 37. Topological SEM views of the SRAM array. Mag. 2200x, 0°.



metal 2

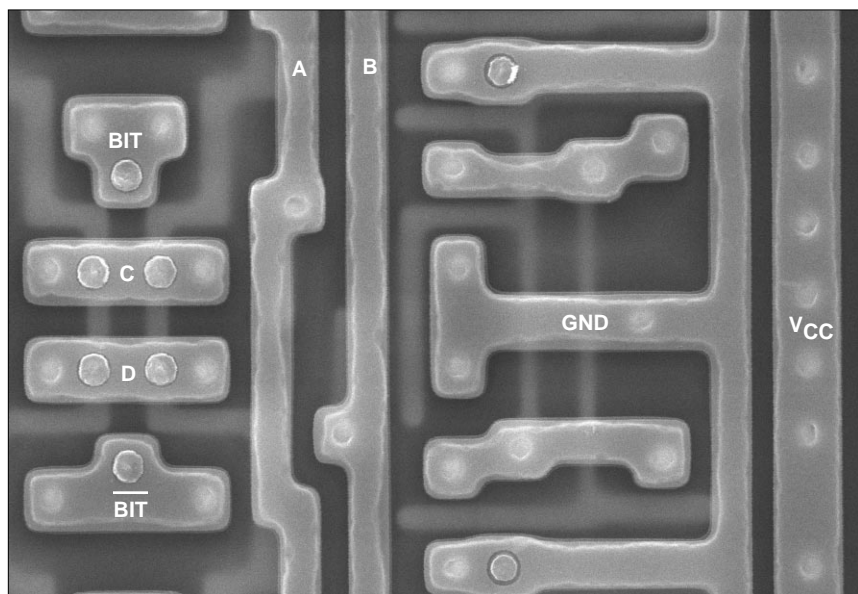


metal 1

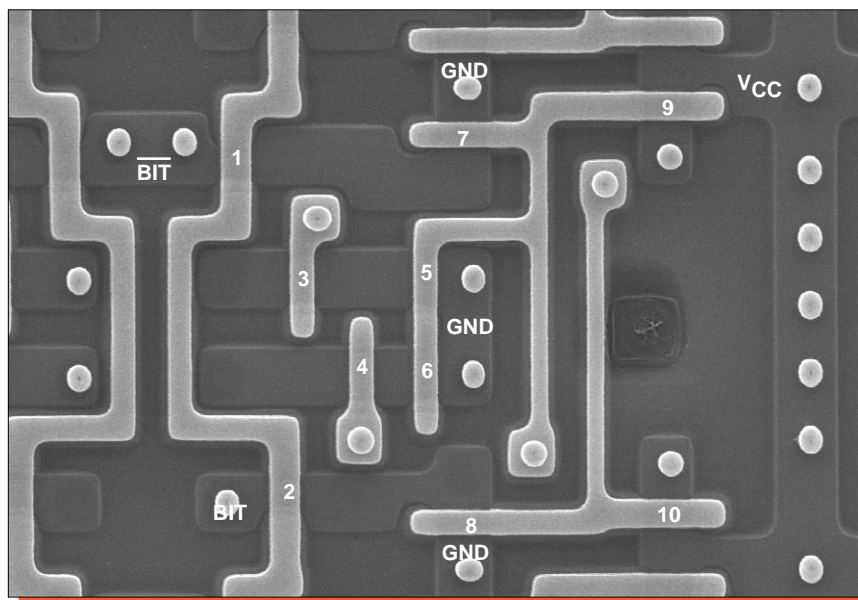


poly 2

Figure 38. Perspective SEM views of the SRAM array. Mag. 4000x, 60°.



metal 1



poly 2

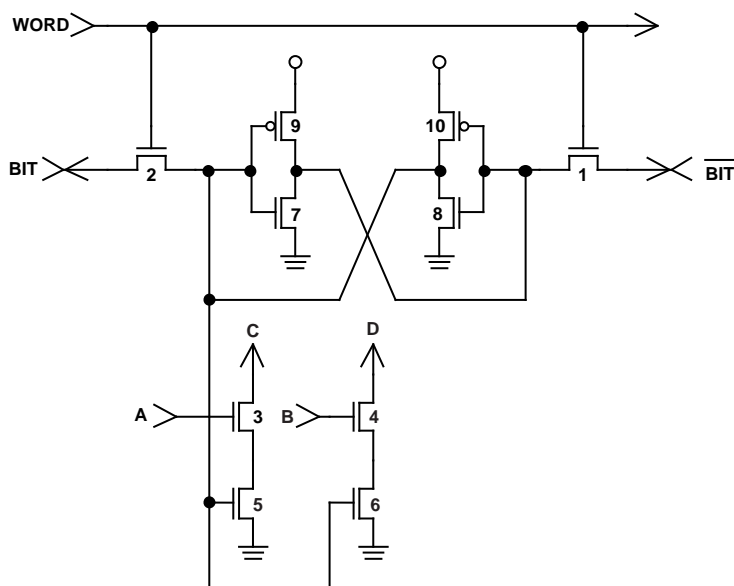


Figure 39. Topological SEM views of an SRAM cell with schematic. Mag. 4400x, 0°.