6 ASIC TECHNOLOGY TRENDS

OVERVIEW

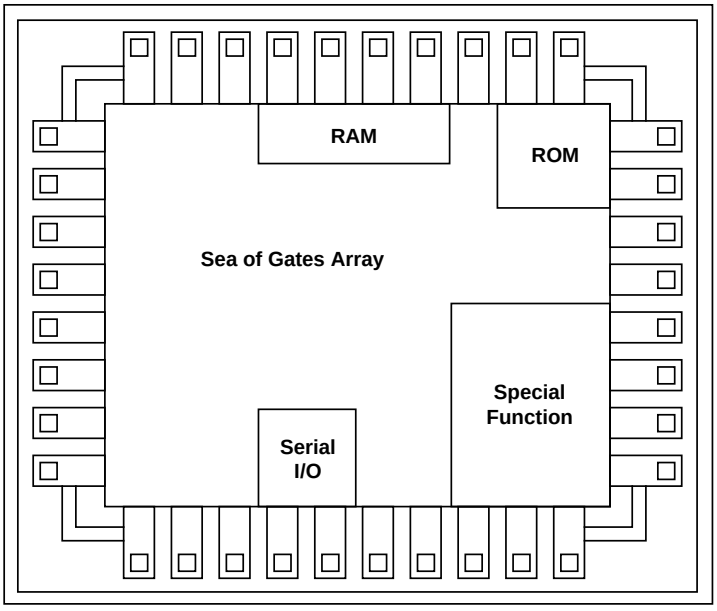
This section will discuss three general trends associated with today's ASIC industry: the rapid advancement of process technologies, the move toward specialization, and a blurring of the distinctions between each of the ASIC product categories. There is also an underlying trend linking these all together: each new ASIC generation requires greater cooperation between ASIC vendors and customers.

Distinguishing between each of the ASIC product categories is becoming increasingly difficult. Until recently, the ASIC industry could be divided up into the three well-defined product groups defined in Section 1: semicustom ICs (gate arrays and linear arrays), custom ICs (standard cells and full custom devices), and programmable logic devices (simple and complex PLDs, FPGAs, and EPACs). However, the lines separating those three categories are getting blurry. The best features of products from one category are increasingly showing up in products of other categories.

Take, for example, embedded arrays, which are based on a gate array structure but have large megacells such as compiled memories or microprocessor cores embedded in them (Figure 6-1). The cells / cores provide a higher level of integration than a pure gate-array structure, but can lead to longer prototype leadtimes, though, still shorter than the leadtimes for pure cell-based ASICs.

Then, there are Motorola's customizable standard products (CSPs), which have been described as a blend of hand-packed cells, standard cells, gate arrays, and / or embedded arrays.

One thing that's true for all types of ASIC devices is that they are becoming more specialized to serve the needs of systems companies. The ASIC industry is moving away from a one-size-fits-all approach, toward a tighter market focus—one that places greater emphasis on performance, power, functionality, and cost considerations on a per customer basis. ASICs are no longer just on the periphery of a system (i.e., glue logic), they are being designed as the core of the system. As a result, ASIC vendors are becoming more segmented or specialized in what they have to offer, including such devices as digital video, networking, telecommunications, or audio ASICs.



Source: EDN/ICE, "ASIC 1997" 19190B

Figure 6-1. Typical Embedded Array ASIC

To meet their complex chip requirements, ASIC customers are having to rely more on the design groups of ASIC vendors or third-party design houses (see Appendix for listing). This is in contrast to the past, when it was basically only a matter of drawing up a schematic and sending the design off to be implemented in silicon by an ASIC manufacturer.

Additionally, the use of third-party cell/core library providers (e.g., Aspec Technology, Cadence Design Automation, Compass, the Silicon Architects Group of Synopsys, and VLSI Libraries) and foundries is becoming an attractive option for ASIC customers. This strategy is sometimes called customer-owned-tooling (COT) ASIC design. COT customers purchase third-party libraries, create a tape of their mask layout using ASIC and physical design tools, and then take the design to foundries like TSMC and Chartered. Figure 6-2 provides a sampling of companies offering ASIC foundry services. Third-party library firms are attracting not only customers of ASICs, but also vendors of ASICs who may be seeking to broaden their own core libraries.

The increase in the functionality of ASICs has been realized by the industry's quick migration to deep-submicron process technologies. Figure 6-3 lists several ASIC producers that have been discussing their deep-submicron ASIC technologies. Note that the companies listed offering this leading-edge technology are all major ASIC producers. The rapid advancement in ASIC technology has not come without challenges or compromises, as will be discussed.

Company and Location	Technologies Offered	Feature Size (μm)	Number of Layers	Production Commitment Required	Fabrication/ NRE Cost
AMCC San Diego, CA	**Bipolar**	**1.0 (drawn)**	**3 metal; 2 poly**	**Varies**	**No typical**
AMI Pocatello, ID	**Digital and mixed-signal ASIC, CMOS**	**0.6**	**2 & 3 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**0.8**	**2 & 3 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**1.0**	**2 & 3 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**1.25**	**2 & 3 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**1.4**	**2 & 3 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**1.4**	**2 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**1.5**	**2 & 3 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**1.5**	**2 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**2.0**	**2 & 3 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**3.0**	**2 & 3 metal**	**no fixed requirements**	**$30,000 - $55,000**
	Digital and mixed-signal ASIC, CMOS	**5.0**	**2 & 3 metal**	**no fixed requirements**	**$30,000 - $55,000**
California Micro Devices Milpitas, CA	**CMOS & BiCMOS**	**1.5**	**2 metal; 2 poly**	**12,000 over 1 year**	**Depends on process/ layers and production commitment**
Honeywell Solid State Electronic Center (SSEC) Plymouth, MN	**Linear Bipolar**	**4.0**	**1 & 2 metal**	**Negotiable**	**$50,000 - $90,000**
	Advanced Linear Bipolar W/TFR	**4.0**	**2 metal**	**Negotiable**	**$50,000 - $90,000**
	CMOS (SOI) IV 5V/3.3V	**0.8**	**3 metal; 1 poly**	**Negotiable**	**$50,000 - $90,000**
IC Works San Jose, CA	**CMOS**	**0.8**	**3 metal; 1 poly**	**Varies**	**Varies by technology**
	CMOS	**0.6**	**3 metal; 1 poly**	**Varies**	**Varies by technology**
	BiCMOS	**0.7**	**2 metal; 2 poly**	**Varies**	**Varies by technology**
	BiCMOS	**0.8**	**2 metal; 2 poly**	**Varies**	**Varies by technology**
IMP San Jose, CA	**CMOS, BiCMOS, EECMOS**	**0.8, 1.0, 1.2, 2.0, 3.0, 5.0**	**2 metal; 2 poly**	**Yes**	**$30,000 - $40,000**
LG Semicon San Jose, CA	**CMOS**	**0.8**	**2 metal**	**50,000 units per month**	**No typical**
	CMOS	**0.6**	**1 poly**	**50,000 units per month**	**No typical**
Micrel San Jose, CA	**CMOS, PMOS, NMOS, BiCMOS, Bipolar**	**1.5 - 5.0**	**2 metal; 2 poly**	**N/A**	**$15,000**
Mitel Semiconductor Bromont, Quebec, Canada	**CMOS Silicon Gate**	**1.2**	**2 metal; 1 & 2 poly**	**100 wafers/year**	**$390 U.S. (per wafer). NRE cost (including masks): $15,000 US per device. Chip Finishing: $2,000 U.S. Masks (typical 11): $13,500 US**
	CMOS Silicon Gate	**1.5**	**2 & 3 metal; 2 poly**	**100 wafers/year**	**Same as above**
	CMOS Silicon Gate	**2.0**	**2 metal; 2 poly**	**100 wafers/year**	**Same as above**
	CMOS Silicon Gate	**3.0**	**2 & 3 metal; 2 poly**	**100 wafers/year**	**Same as above**
	CMOS Silicon Gate	**4.0**	**2 metal; 1 & 2 poly**	**100 wafers/year**	**Same as above**
	CMOS Silicon Gate	**5.0**	**2 metal; 1 & 2 poly**	**100 wafers/year**	**Same as above**
	CMOS Metal Gate 9.0 (15V)	**9.0**	**3 metal; 3 poly**	**100 wafers/year**	**Same as above**

Source: Integrated System Design/ICE, "ASIC 1997" 21248

Figure 6-2. ASIC Foundries

Company and Location	Technologies Offered	Feature Size (μm)	Number of Layers	Production Commitment Required	Fabrication/ NRE Cost
National Semiconductor Santa Clara, CA	**CMOS + Capacitor Module**	**1.0 drawn**	**2 metal; 1, 2 with module poly**	**Design dependent**	**$55,000 - $80,000**
	CMOS + Capacitor Bipolar Module	**0.8 drawn**	**3 metal; 1, 2 with module poly**	**Design dependent**	**$60,000 - $85,000**
	CMOS	**0.72 drawn**	**3 metal; 1 poly**	**Design dependent**	**$65,000 - $90,000**
	ABiC BiCMOS Ft = 12GHz	**0.8 drawn**	**4 metal; 1 poly**	**Design dependent**	**$100,000 - $200,000**
Orbit Semiconductor Sunnyvale, CA	**Digital CMOS, Mixed Analog Digital CMOS, Charge Coupled Device (CCD)**	**1.0 drawn**	**2 metal; 3 poly**	**No**	**Conversion $10,000 Manufacturing service tooling plus fabrication approximately $50,000**
Quality Semiconductor Australia* Homebush, NSW, 2140 Australia	**CMOS 12SPTW**	**1.0/1.2**	**2 metal; 1 poly**	**N/A**	**$20,000 - $50,000**
	CMOS 12DPTW	**1.2**	**2 metal; 2 poly**	**N/A**	**$20,000 - $50,000**
	CMOS DVTW	**1.5**	**2 metal; 2 poly**	**N/A**	**$20,000 - $50,000**
	CMPS LVCMOS	**1.5**	**2 metal; 1 poly**	**N/A**	**$20,000 - $50,000**
	CMOS EEPROM	**1.5**	**2 metal; 1 poly**	**N/A**	**$20,000 - $50,000**
	Bipolar	**5.0**	**2 metal**	**N/A**	**$20,000 - $50,000**
Raytheon Electronics, Semiconductor Division Mountain View, CA	**Bipolar process with precision thin film resistors**	**5.0**	**1 or 2 metal**	**N/A**	**To be determined**
	Linear B2 Process	**4.0**	**1 or 2 metal**	**N/A**	**To be determined**
	J12 Process (12V)	**3.0**	**2 metal**	**N/A**	**To be determined**
	High performance complimentary BiCMOS process	**2.0**	**2 metal**	**N/A**	**To be determined**
	High performance complimentary BiCMOS process	**2.0**	**2 metal**	**N/A**	**To be determined**
Ricoh Corporation, Electronic Devices Division San Jose, CA	**CMOS**	**1.2, 0.8**	**2 metal; 1 poly**	**Yes**	**Call**
S-MOS Systems San Jose, CA	**CMOS**	**0.6, 0.65, 0.8, 1.0**	**2 metal (2 & 3 for 0.65); 1 poly**	**N/A**	**$10,000 - $40,000**
Semtech** Santa Clara, CA	**20V Bipolar, 40V Bipolar, Metal Gate CMOS**	**4.0**	**1 & 2 metal**	**200 a month minimum**	**No typical**
Standard Microsystems Corporation (SMC) Hauppauge, NY	**RC/Thin Film, sensors**	**2.0**	**2 metal; 1 poly**	**Varies**	**Process dependent**
Thesys Microelectronics Erfurt, Germany	**HCN08, HCP08**	**0.8**	**2 metal; 1 poly**	**No**	**On request**
	BIC12 (BiCMOS)	**1.2**	**2 metal; 1 poly**	**No**	**On request**
	HCN15 modular process concept	**1.5**	**2 metal; 2 poly modular**	**No**	**On request**
TriQuint Semiconductor Beaverton, OR	**GaAs MESFET: Enhancement, Depletion, Power**	**0.5, 0.6, 1.0**	**4 layer gold metal**	**No**	**As low as $7,900 for prototype chips, and $51,000 for prototype run. Aditional NRE for package and test development**
TSMC Hsinchu, Taiwan	**Logic, memory, mixed-signal process**	**0.5 logic & mixed-signal**	**Varies up to 3 metal; 3 poly**	**Varies**	**Varies by technology, feature size, process, wafer size**
	Logic, memory, mixed-signal process	**0.45 memory**	**Varies up to 3 metal; 3 poly**	**Varies**	**Varies by technology feature size, process, wafer size**
	Logic, memory, mixed-signal process	**0.35**	**4 metal**	**Varies**	**Varies by technology, feature size, process, wafer size**

*** Formerly AWA MicroElectronics**
**** Formerly ECI Semiconductor**

Source: Integrated System Design/ICE, "ASIC 1997" 21249

Figure 6-2. ASIC Foundries (continued)

Company	Year	Series	Feature Size (L_{eff})	Metal Layers	Gate Oxide (Å)	Voltage
IBM Microelectronics	1995	CMOS 5S	0.25μm	6	90	3.3V
	1996	CMOS 5X	0.4μm	5	70	2.5V
	1997	CMOS 6S	0.18μm	6	—	2.5V
Hitachi/ VLSI Technology	1996	—	0.35μm	5	60	2.5V
NEC	1995	CMOS-9	0.27μm	4	—	2.5V/3.3V
Toshiba	1994	TC200	0.36μm	3	—	3.3V
	1996	TC220	0.3μm*	3	––	3.3V
Oki	1995	MSM98R	0.4μm	3	—	3.3V/5V
LSI Logic	1995	G10	0.25μm	5	—	2.5V/3.3V
Lucent Technologies	1996	System-ASIC	0.32μm	4	50/65	2.5V/3.3V
Texas Instruments	1996	Timeline	0.18μm	6	—	2.5V/3.3V

*** Drawn gate length**

Source: ICE, "ASIC 1997" 19177D

Figure 6-3. Sampling of Leading-Edge ASIC Technologies

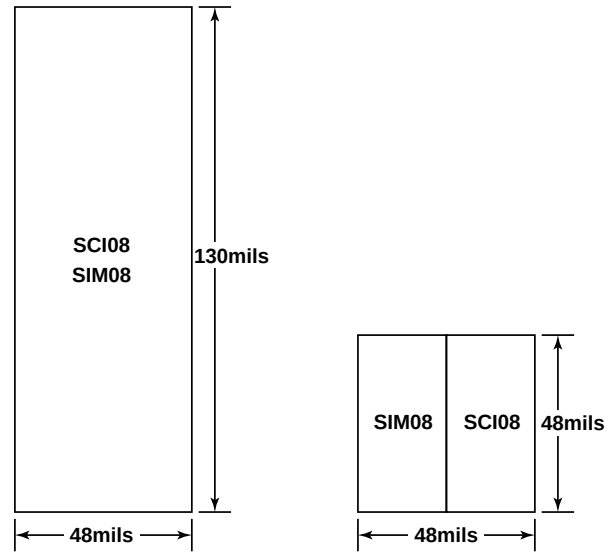
FULL CUSTOM ICs

As was shown in Section 4, the full custom or "handcrafted" IC market is not expected to show much strength in the late 1990's. Still, at $2.75 billion (1995), the market for full custom ICs is sizable.

The full custom methodology is generally used where the absolute smallest die size or highest performance is desired or if the technology required is unusual. However, it is an expensive option due to the complexity of the layout process.

Figure 6-4 compares the silicon area needed for two circuit modules used in Motorola's 68HC08XL36 customer-specific microcontroller by a standard-cell version and a full-custom version. Although the standard-cell version required over two-times as much area as the custom version, it was produced more quickly.

Overall, the flexibility and shorter turnaround times of the standard cell-based approach, as compared to full custom, will make the cell-based methodology a more popular choice for custom ASICs in the late 1990's and beyond. Nevertheless, there will continue to be some demand for "handcrafted" ASICs for high-volume, cost-sensitive systems that require the most efficient device designs.



Source: EBN/Motorola/ICE, "ASIC 1997" 21256

Figure 6-4. Comparison of Silicon Requirements for Standard Cell and Full Custom Layouts (Based on Motorola's 68HC08XL36 MCU)

GATE ARRAY, EMBEDDED ARRAY, AND CELL-BASED ASICs

The primary ASIC methodologies in use today are CMOS gate array, embedded array, and standard cell. Which methodology to use depends on the particular application. Figure 6-5 shows a comparison of the three techniques.

	Design Flexibility	Number of Standard Die Sizes (Typical)	Prototype Manufacturing Time	Design Changes	Core Availability	Memory Density	NRE Cost	Factor Determining Use
Gate Array	Medium	14	Fast (only metal layers); typical TAT* = 1-2 weeks; QuickTAT = 3 days	Fast (only metal layers) (QTAT = 3 days)	Metallized RAM/ROM; controllers; standard functions, etc.	Low (metal limited)	Lowest	Design cost, time to market
Embedded Array	High	30	Needs all mask stages (base layers can be signed off early, reducing TAT); typical TAT = 1-12 weeks	Fast (if only metal change required)	Microcontrollers; microprocessors; DSP; SRAM; DRAM	High (diffused) + very high (DRAM)	Needs to cover full mask set and processing	Megacell performance/ density; standard masters for customized variations (i.e., µP-based print engines)
Standard Cell	High	30	Needs all mask stages; typical TAT = 6-12 weeks	Usually needs all mask stages	Microcontrollers; microprocessors; DSP; SRAM; DRAM	High (diffused) + very high (DRAM)	Needs to cover full mask set and processing	Maximum customization ability; need for high percentage of customized design (i.e., data paths with little standard logic)

*** Turn-around time**

Source: Computer Design/ICE, "ASIC 1997" 21257

Figure 6-5. Gate Array, Embedded Array, and Cell-Based ASIC Comparison

As already mentioned, ASICs are increasingly being used to build systems on a chip, which requires blocks (or cores) of high-performance memory, processor, and special I/O functions. This rise in complexity is the reason behind the prediction that standard cell and embedded array ASICs will dominate over gate arrays before the end of the decade. The transistors in gate arrays are generally not laid out conveniently for some of the more-complex logic functions, resulting in a mess of wires (and a large chip).

Cores may be selected from a vendor's core library and ordered, like a product off the shelf, for design into a standard cell or embedded array ASIC. Advanced cores featured in some core libraries include high-performance RISC or CISC microprocessors, MPEG coder/decoders, network communications controllers, high-density memories, and high-performance analog functions.

Shown in Figure 6-6 is a macrocell/core roadmap for Lucent Technologies, the world's largest standard cell ASIC supplier in 1995. Several other companies offering hardware-based and software-based cores and megacells are listed in Figures 6-7 and 6-8.

Application	1995	1996	1997
PC	MPEG Decoder PCI Controller Fast SRAM 120-200MHz PLL	Video Scaler Video Decoder Video-DAC Audio DAC/ADC Card Bus Interface I^2C Bus Interface	Multimedia, PLL Extensions
Office Automation	960-RISC Z80 μC	68K RISC SPARCDSP LCD Controller Z180 μC USB Interface	RISC Core Extensions P1394 Serial Port
Data Communications	C2XLP DSP	C5x DSP 12-bit DAC/ADC Fiber Channel Controller	DSP Core Extensions Fiber Channel Transceiver
Telecom	10 Base-T MAC updates 10/100 Base-T MAC 6-port SRAM HDLC Controller	ISDN-S Interface TI/EI Framer FDDI/Tx Transceiver 1627 DSP	ATM Interface RAMBUS Interface

Source: Lucent Technologies/ICE, "ASIC 1997" 21200

Figure 6-6. Lucent Technologies' Macrocell Roadmap

Demand for DSP core-based ASICs is surging in high-volume, cost-sensitive applications such as wireless and wireline communications, consumer electronics, and multimedia computers. Figure 6-9 is a sample listing of companies offering DSP core cells.

Company and Location	Cells	Models*	Process Technology	Gates/ mm^2	Bits/ mm^2	Verified	License
American Microsystems (AMI) Pocatello, ID	**PCI, Datapath, 805x processors, 804x processors, 29xx bit slice, Peripherals**	**G, H**	**1.0-, 0.8-, 0.6μm**	**N/A**	**N/A**	**Yes**	**Call**
Aspec Technology Sunnyvale, CA	**RAM (high-density)**	**H**	**0.8-, 0.6-, 0.5μm**	**N/A**	**6-, 9-, 12k**	**Yes**	**$45,000**
	RAM (low-power)	**H**	**0.8-, 0.6-, 0.5μm**	**N/A**	**N/A**	**Yes**	**$45,000**
	ROM	**H**	**0.8-, 0.6-, 0.5μm**	**N/A**	**21-, 41-, 53k**	**Yes**	**$45,000**
Focus Semiconductor Lower Gwynedd, PA	**RAM, ROM, DSP, PLL, VCO, DAC, ADC, synthesizers**	**G**	**0.6μm-3μm CMOS**	**N/A**	**N/A**	**Yes**	**Call**
Hitachi America Brisbane, CA	**H8 MPU, DMA, ADC (10 bit), DAC (8 bit), Peripherals**	**N/A**	**0.8μm CMOS 2LM**	**2,000**	**N/A**	**Yes**	**Call**
Honeywell Solid State Electronics Center Plymouth, MN	**8051, RAM, 82xx peripherals**	**N/A**	**RICMOS IV 0.8μm, SOI IV 0.8μm**	**Varies**	**N/A**	**Mixed**	**None**
IBM Microelectronics Essex Junction, VT	**N/A**	**N/A**	**CMOS 5L 0.46μm L_{eff} 0.5μm Lith 1.5M gate wireable**	**N/A**	**N/A**	**N/A**	**Call**
Lucent Technologies Allentown, PA	**82xx peripherals, 85xx peripherals 8-bit processors, UART, DMA, DSP, LAN MAC, PCI**	**N/A**	**N/A**	**2,300**	**9,200**	**Yes**	**Call**
NEC Electronics Mountain View, CA	**V20/V30 processors, Peripherals, PLL, Analog cells, RAM, ROM, RAMbus**	**VH, VL, G**	**0.8-, 0.5μm**	**4.0k**	**4.3k**	**Yes**	**Call**
OKI Semiconductor Sunnyvale, CA	**Programmable Peripherals, SCSI, PCMCIA, PCI, UART, Real-time clocks**	**VH, VL, G**	**0.8-, 0.5μm CMOS**	**N/A**	**N/A**	**Yes**	**Call**
Samsung Semiconductor San Jose, CA	**ARM RISC processor**	**VH, VL**	**CMOS 0.8μm**	**N/A**	**N/A**	**Yes**	**Call**
	16-bit DSP, 80C51	**N/A**	**CMOS 0.8μm**	**N/A**	**N/A**	**Yes**	**Call**
	I/O, timer, UART	**VH, VL, G**	**N/A**	**N/A**	**N/A**	**Yes**	**Call**
Silicon Engineering Scotts Valley, CA	**Microcontrollers**	**G, H**	**0.6μm**	**N/A**	**N/A**	**N/A**	**Call**
Silicon Systems Tustin, CA	**AGC, PLL, Filters, Synthesizers, ECC, SCSI, ATAP interface, PCMCIA interface**	**VH**	**CMOS 0.8μm**	**N/A**	**N/A**	**N/A**	**Call**
Symbios Logic Fort Collins, CO	**RAM, ROM, Dual port RAM, SRAM**	**H**	**0.75-, 0.5μm CMOS**	**3,700 or 5,800**	**5,000 or 7,700**	**Yes**	**Normal NRE**
Synergy Semiconductor Santa Clara, CA	**PLL, DAC, ADC, AGC, RAM**	**N/A**	**Bipolar 1.2μm**	**N/A**	**N/A**	**Yes**	**Call**
Vitesse Semiconductor Camarillo, CA	**Register files, PLL, Datapath, Instrumentation**	**N/A**	**H-GaAs 0.6μm**	**2,000**	**2,300**	**Yes**	**Call**

*** VL: Verilog, VH: VHDL, G: Gate Level, H: HDL**

Source: Integrated System Design/ICE, "ASIC 1997" 21260

Figure 6-7. Hardware-Based Megacells and Cores

Company and Location	Cells	Models*	Process Technology	Gates/ mm^2	Bits/ mm^2	Verified	License
3Soft San Jose, CA	**Microcontrollers (8 bit), DSP, SCSI, Peripherals**	**VH, VL, G**	**N/A**	**N/A**	**N/A**	**Most**	**Call**
Advancel Logic Cupertino, CA	**ATM, SONET**	**VH, VL, G**	**CMOS 0.5μm-0.8μm**	**N/A**	**N/A**	**Yes**	**$60,000-$120,000**
Advanced RISC Machines (ARM) Los Gatos, CA	**RISC processors RISC peripherals**	**VH, VL**	**Various**	**N/A**	**N/A**	**Yes**	**Call**
Aspec Technology Sunnyvale, CA	**Datapath**	**G**	**0.8-, 0.6-, 0.5μm**	**1,500, 3,300, 4,700**	**N/A**	**Yes**	**$55,000**
	SCSI Controllers	**G**	**0.8-, 0.6-, 0.5μm**	**1,500, 3,300, 4,700**	**N/A**	**Yes**	**$50,000**
	DSPs	**G**	**0.8-, 0.6-, 0.5μm**	**1,500, 3,300, 4,700**	**N/A**	**Yes**	**$30,000**
	6502	**G**	**0.8-, 0.6-, 0.5μm**	**1,500, 3,300, 4,700**	**N/A**	**Yes**	**$20,000**
Cascade Design Automation Bellevue, WA	**82xx peripherals, Video compression**	**VL, G**	**N/A**	**N/A**	**N/A**	**Yes**	**Call**
Compass Design Automation San Jose, CA	**RAM, ROM, MAC, ALU, Datapath**	**VH, VL, G**	**N/A**	**c. 15k (0.35μm)**	**9,800 (0.35μm)**	**Yes**	**Call**
DQDT Carlsbad, CA	**DSP functions, Datapath**	**VH**	**N/A**	**N/A**	**N/A**	**Yes**	**Call**
Eureka Technologies Milpitas, CA	**PowerPC, PCI, 80x86, Peripherals**	**VL**	**N/A**	**N/A**	**N/A**	**Yes**	**Call**
Logic Innovations San Diego, CA	**PCI bus, Processor core**	**VH, VL**	**ASIC/FPGA/ custom**	**N/A**	**N/A**	**Yes**	**Call**
RAVIcad Sunnyvale, CA	**PCI, DMA carbus, PCI2PCI bridge, PCI2Cardbus**	**VH, VL**	**0.6μm**	**N/A**	**N/A**	**N/A**	**$70,000**
Sierra Research and Technology Inc. Mountain View, CA	**6085 CPU, 6816 CPU 78014 CPU, 100M Ethernet PCI+DMA+ MAC**	**VL**	**N/A**	**Varies**	**N/A**	**N/A**	**Call**
S-MOS Systems San Jose, CA	**PCI bus interface**	**H**	**1.0-, 0.65-, 0.6μm CMOS**	**2,450 @ 0.6μm**	**700**	**Most**	**Call**
	PLL, UART PCMCIA, CPU, MCU, PIT, PIC	**G**	**1.0-, 0.65-, 0.6μm CMOS**	**2,450 @ 0.6μm**	**700**	**Most**	**Call**
Technical Data Freeway Concord, MA	**Microprocessors, Viterbi generators, 82xx peripherals, DSP**	**VH, VL**	**N/A**	**N/A**	**N/A**	**N/A**	**Call**
	RAM, ROM	**N/A**	**N/A**	**N/A**	**N/A**	**Yes**	**Call**
VAutomation Nashua, NH	**Z80, 6502, 80x86, Ethernet LAN**	**VH, VL**	**N/A**	**N/A**	**N/A**	**Yes**	**Call**
VLSI Libraries, Inc. Santa Clara, CA	**Standard Cells, RAM, ROM, I/O Cells Multipliers, Datapath**	**VH, VL, G**	**0.35μm-0.8μm CMOS**	**8,000-9,000 at 0.5μm**	**11,000 at 0.5μm**	**Yes**	**Call**
Western Design Center Mesa, AZ	**65xx microcontrollers, 65xx peripherals, RAM, ROM**	**N/A**	**0.8μm**	**N/A**	**c. 1,200**	**Yes**	**$5,000**

*** VL: Verilog, VH: VHDL, G: Gate Level, H: HDL**

Source: Integrated System Design/ICE, "ASIC 1997" 21261

Figure 6-8. Software-Based Megacells and Cores

Company and Location	Family	Data Width	Program Width	Native MIPS*	Notes
3Soft Corporation San Jose, CA	**M320C25**	**16 bits**	**16 bits**	**15 MIPS**	**Provided as synthesizable HDL**
Adaptive Solutions Beaverton, OR	**CNAPS**	**16 bits**	**64 bits**	**1,280 MIPS**	**Scalable 2-chip SIMD multiprocessor**
Analog Devices Norwood, MA	**ADSP-21xx**	**16 bits**	**24 bits**	**20 MIPS**	**No visible pipeline effects**
	ADSP-216x	**16 bits**	**24 bits**	**25 MIPS**	**Two serial ports, timer, power-down mode**
	ADSP-217x	**16 bits**	**24 bits**	**33 MIPS**	**Host port, two serial ports, power-down mode**
	ADSP-2181	**16 bits**	**24 bits**	**33 MIPS**	**Host port, two serial ports, DMA**
	ADSP-21msp5x	**16 bits**	**24 bits**	**26 MIPS**	**Integrated 16-bit A/D and D/A**
	ADSP-21020	**32 bits**	**48 bits**	**33 MIPS**	**Two off-chip memory buses**
	ADSP-2106x	**32 bits**	**48 bits**	**40 MIPS**	**Strong support for multi-processor designs**
Clarkspur Design Saratoga, CA	**CD2400**	**16 bits**	**16 bits**	**30 MIPS**	**Simple, very compact architecture**
	CD2450	**16-24 bits**	**16 bits**	**50 MIPS**	**Adjustable data word width**
DSP Group Santa Clara, CA	**PINE**	**16 bits**	**16 bits**	**30 MIPS**	**Provided as synthesizable HDL and layout**
	OAK	**16 bits**	**16 bits**	**40 MIPS**	**Provided as synthesizable HDL and layout**
IBM Microelectronics Hopewell Junction, NY	**MDSPxxxx**	**16 bits**	**24 bits**	**25 MIPS**	**Intended for PC multimedia applications**
Lucent Technologies Allentown, PA	**DSP16xx**	**16 bits**	**16 bits**	**50 MIPS**	**Flash memory versions available for prototyping**
	DSP32xx	**32bits**	**32 bits**	**20 MIPS**	**Intended for PC multimedia applications**
Motorola Austin, TX	**DSP561xx**	**16 bits**	**16 bits**	**30 MIPS**	**Integrated 16-bit A/D and D/A**
	DSP5600x	**24 bits**	**24 bits**	**33 MIPS**	**24-bit data word**
	DSP9600x	**32 bits**	**32 bits**	**20 MIPS**	**Dual external memory buses**
NEC Mountain View, CA	**μPD7701x**	**16 bits**	**32 bits**	**33 MIPS**	**Two serial ports, one parallel port, 4-bit I/O lines**
SGS-Thomson Carrollton, TX	**D950-CORE**	**16 bits**	**16 bits**	**40 MIPS**	**Coprocessor interface provided**
Tensleep Design Austin, TX	**A/DSC321**	**16 bits**	**16 bits**	**12.5 MIPS**	**Similar to TMS320C25**
	A/DSC421	**16 bits**	**16 bits**	**25 MIPS**	**Similar to TMS320C25**
	A/DSC521	**16 bits**	**16 bits**	**30 MIPS**	**Similar to TMS320C25**
Texas Instruments Dallas, TX	**TMS320C1x**	**16 bits**	**16 bits**	**8.8 MIPS**	**First commercially successful DSP**
	TMS320C2x	**16 bits**	**16 bits**	**12.5 MIPS**	**TI's second-generation fixed-point DSP**
	TMS320C3x	**32 bits**	**32 bits**	**30 MIPS**	**Low-cost versions compete with fixed-point DSPs**
	TMS320C4x	**32 bits**	**32 bits**	**30 MIPS**	**Intended for multiprocessor applications**
	TMS320C5x	**16 bits**	**16 bits**	**50 MIPS**	**TI's latest fixed-point family**
	TMS320C80	**32/64 bits**	**8/16/31 bits**	**250 MIPS**	**Contains four fixed-point DSPs plus a RISC CPU**
Zilog Campbell, CA	**Z89Cxx**	**16 bits**	**16 bits**	**20 MIPS**	**Available with a microcontroller on one chip**
Zoran Santa Clara, CA	**ZR3800x**	**20 bits**	**32 bits**	**33 MIPS**	**20-bit data word is unique, intended for audio**

*** Native MIPS for fastest member of family.**

Source: Integrated System Design/ICE, "ASIC 1997" 21262

Figure 6-9. Digital Signal Processors and Cores

Although a DSP core can be used to process analog functions, it may or may not be the most effective solution, depending on the application. As a result, demand for ASICs incorporating analog circuitry continues to be strong. Furthermore, functions like audio, imaging, temperature sensing, and frequency modulation will always require at least an analog, or "real world" interface. Applications such as HDTV, cellular communications, multimedia, teleconferencing, voice synthesis/recognition, modems, etc., are pressuring standard cell vendors to offer state-of-the-art mixed-signal capabilities. Unfortunately, the sophisticated design, manufacturing, and testing of mixed-signal devices continues to pose formidable challenges.

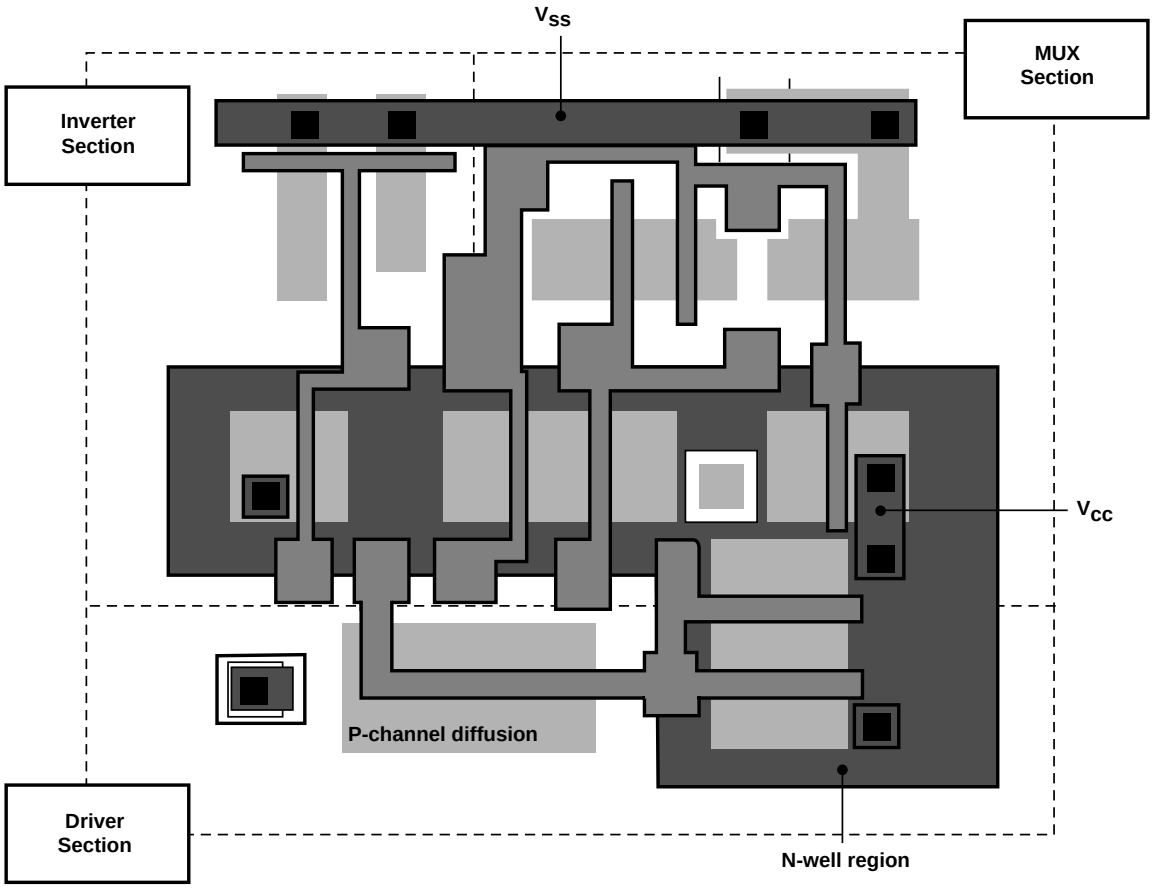
As evidence to the significance of the mixed-signal ASIC industry, NEC has said that about one-third of its standard cell customers desire analog circuitry in their chip designs. SGS-Thomson is one example of a large standard analog IC supplier using its analog expertise and experience to enhance the mixed-signal capabilities of its standard cell product line. National, Harris, and Lucent Technologies are other examples of this trend.

Demand for high-density gate arrays continues to be high, due to a considerable number of advanced ASIC designs being pad-limited. Pad limited means the die size is determined by the number of I/O pads needed rather than the number of gates used. For non-pad-limited designs, the leading manufacturers of high-density (greater than 50,000 gates) CMOS gate arrays are implementing at least three-layer metal processes in order to increase the efficiency of gate usage (and also increase performance). Three layers of metal interconnection provide up to 70 percent gate utilization as opposed to about 35-45 percent for double-layer metal arrays.

The performance limits of gate arrays are being extended by several developments not only in CMOS technology, but also in GaAs and BiCMOS technologies. Examples are provided below.

- Sunnyvale, California-based Silicon Architects (acquired by Synposys in 1995) is promoting its cell-based array (CBA) technology, which the company says combines standard cell density, performance, and power with gate array time-to-market and portability. The CBA architecture utilizes a small compute cell and a larger adjustable-size drive cell. The basic compute cell is optimized for memory and data path operations, while the drive cells are optimized for performance in critical paths. This structure allows for the implementation of the more-complex logic functions, including, eventually, functions such as an MPEG chip.

- Researchers at Texas Instruments have developed a CMOS gate array architecture that replaces the standard NAND base cells with multiplexers (Figure 6-10). Besides simplified interconnection schemes, TI claims the approach offers lower power dissipation and a denser cell layout that will allow gate array technology to move well beyond the million-gate level. The architecture is based on a simple four-transistor layout with the first metal layer defined. The final wiring is simplified by requiring only short "poly jumpers" to connect the transistors as needed.



Source: EETimes/TI/ICE, "ASIC 1997" 21258

Figure 6-10. TI Develops Architecture for High-Density Gate Arrays

- In September 1995 NEC introduced its QB-8 ASIC family incorporating a new proprietary BiCMOS gate array architecture called "PUZZLE" (Figure 6-11). Based on a 0.5µm three-level metal process, the QB-8 family offers the low power and short turnaround time of a CMOS process combined with the high-speed of a bipolar ASIC. The PUZZLE process combines three different size transistors into a single high-density architecture, with MOS elements used for input signals and BiCMOS elements used for output signals.

- In October 1995 Vitesse Semiconductor announced a major advancement in high-performance gate arrays with the introduction of its GLX family of ASICs. Based on a 0.6µm five-layer-metal GaAs process, the GLX family of devices can perform at up to 800MHz and have up to 250K raw gates with 60-70 percent utilization. The GLX arrays provide per-gate power as low as 0.07mW and volume pricing below 0.1 cent per usable gate. Megacell blocks can also be embedded into base arrays.

Physical Description	
Device Size	**0.5μm (0.35μm L_{eff})**
Process	**CMOS-based epi-less BiCMOS**
Metal Options	**3 Layers**
Raw Gates	**32,000 to 379,000**
Usable Gates	**19,000 to 223,000**
Pad Counts	**156 to 672**
Voltage Level	**3.3V ±5%**
Performance	**139ps (F/O = 2, L = 0.5mm)**
Power Dissipation	**0.26μW/MHz/gate**
I/O Capabilities	
LVTTL	**100MHz, std. buffers, fail-safe function**
pECL	**High speed clock input (250MHz)**
PCI (spec 2.1)	**3.3V or 5V**
GTL	**Interface for processor buses (75MHz)**
HSTL	**Interface for V_R10000 processor bus (250MHz)**
Packaging	
PQFP	**Up to 376 pins**
PGA	**Up to 524 pins**
BGA	**Up to 524 solder balls**

Source: NEC/ICE, "ASIC 1997" 21259

Figure 6-11. NEC's "PUZZLE" BiCMOS Gate Array Specs

Demand for high-density ECL arrays has been lessened by advances in CMOS, BiCMOS, and GaAs gate arrays. Moreover, because of the inherent problems encountered with high-density ECL devices (e.g., high heat dissipation), most ECL array manufacturers will not pursue the technology beyond the 50K density level. Likewise, ICE does not expect to see a recognizable market for greater than 50K-gate ECL gate arrays.

Analog and mixed-signal arrays continue to represent a niche ASIC technology. Most of the analog array companies do less than 25-50 designs per year, quite small when compared to the large number of digital gate array designs realized each year. Overall, very high-end analog and mixed-signal ASIC requirements are still best handled by standard cell or full custom approaches.

Recent notable announcements regarding gate arrays, embedded arrays, and standard cells are provided below.

- In 4Q95 Hitachi began offering its SH-1 32-bit RISC controllers as part of its 0.5μm ASIC cell library. The company also added to its cell library, an MPEG decompression core licensed from CompCore Multimedia Inc.

- Hitachi began taking orders for its HG73G gate array and HG73E embedded array 0.35μm CMOS ASICs in April 1996. The triple-metal process enables designs of up to 1.5 million gates.

- In 4Q95 IBM Microelectronics unveiled an extensive plan to target the cell-based ASIC marketplace using a wide range of what it calls "system building blocks" (Figure 6-12). IBM's most advanced ASIC family, dubbed the System ASIC-12 (SA-12), was unveiled in May 1996. Details concerning the SA-12 architecture are provided below.

Production Volumes:	2Q97 (netlists accepted in 4Q96)
Technology:	0.25µm drawn (0.18µm effective) gate length
Metal Pitch:	1.0µm
Metal Layers:	Up to 6
Raw Gates:	Up to 5M
Usable Gates:	Up to 3.5M
I/Os:	Up to 1,088
Power Supply:	2.5V with power dissipation of 0.08-0.18µW/MHz/gate
Special Macros:	32-/64-bit PowerPC MPU/MCU, DSP, VGA, Rambus interface, audio compression, MPEG-2

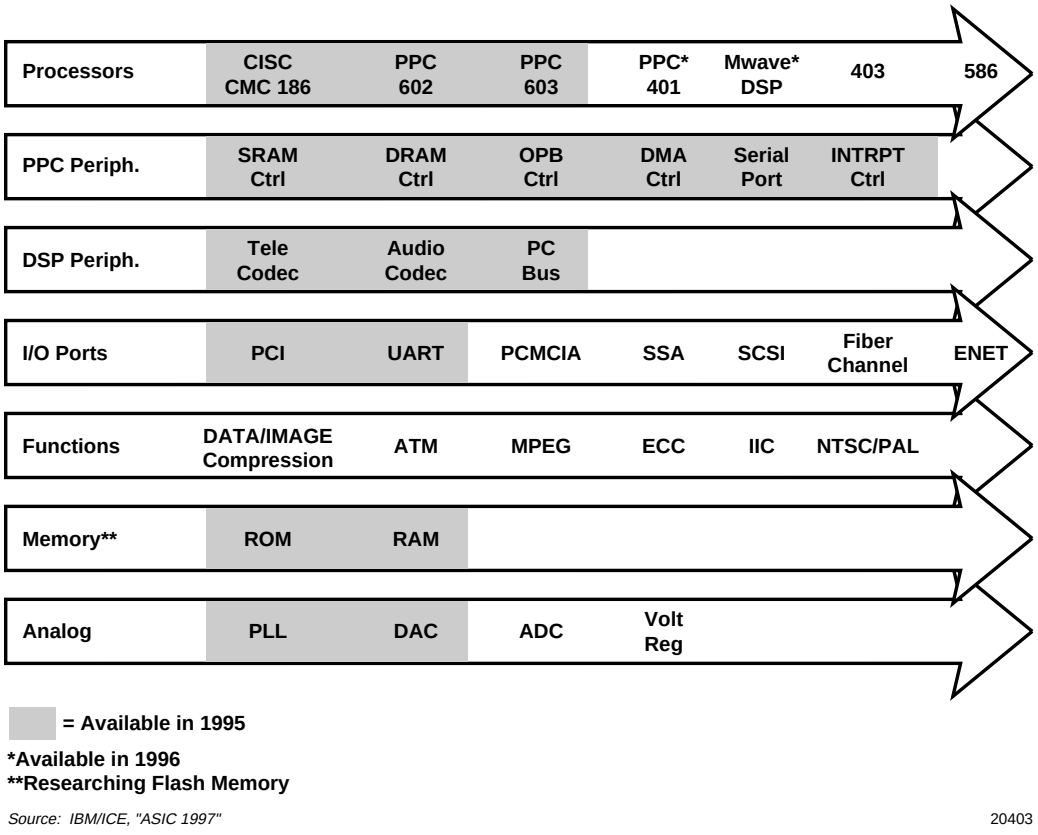


Figure 6-12. IBM's System Building Block Roadmap

- In early 1996, IBM Microelectronics began accepting netlists for its CMOS 5X process—the third and final derivative of the company's 0.5µm ASIC process. The process uses 0.25µm effective gate lengths (0.35µm drawn) and offers up to 1.6 million usable gates and as many as 748 I/O pins. Other features of the architecture include 1.2µm metal pitch and 70Å oxide thickness.

- IBM rolled out its PowerPC 401GF core, which is targeted at low-cost battery-operated systems. Initially offered in 25MHz and 50MHz versions, the 401GF consumes as little as 40mW (typical, @25MHz) from a 2.5V power supply. The chip, measuring 4.5mm^2, is manufactured using IBM's 0.5µm three-layer metal CMOS-5S process technology. 75MHz and 100MHz versions are expected to follow before the end of 1996.

- LG Semicon added the ARM7 microprocessor and ARM710 microcontroller cores, licensed from Advanced RISC Machines Limited, to its cell library.

- In 2Q96 LSI Logic added the new Gigabit SeriaLink™ interface core to its CoreWare cell library. The CMOS-based Gigabit SeriaLink supports the Fibre Channel data transmission protocol, which allows for the transmission of up to 1.0625 billion bits of data per second, the equivalent of several 350-page novels a second.

- LSI Logic introduced its G10™ ASIC process technology in 3Q95. Figure 6-13 offers a look at some of the new G10 characteristics along with a history of previous LSI Logic ASIC technologies. Figure 6-14 shows the various sub-families of the G10 technology and their targeted applications. Volume production of G10 ASICs began in 1Q96.

LSI CMOS Process	G10™ Family	500K	600K	400K	405K	300K
Drawn	0.35µm	0.5µm	0.6µm	0.7µm	0.8µm	0.6µm
Effective	0.25µm	0.38µm	0.45µm	0.55µm	0.65µm	0.45µm
Architectures	Cell Based Embedded Array Gate Array	Cell Based Embedded Array Gate Array	Cell Based	Gate Array	Cell Based Embedded Array Gate Array	Cell Based Embedded Array Gate Array
Metal Interconnect	2, 3, 4, & 5 Layer	2, 3, & 4 Layer	2 & 3 Layer	2 Layer	2 Layer	2 & 3 Layer
Operating Voltages	3.3 & 2.5 Volts	3.3 Volts	3.3 Volts	3.3 Volts	5.0 Volts	5.0 Volts
I/O Options	GTL/NTL/HSTL PECL to 622 MHz PCI Impedance Controlled LVTTL LVDS to 1.2GHz Mixed Signal	GTL/NTL/HSTL PECL to 622MHz PCI Mixed Signal	GTL/NTL PECL to 155MHz PCI Mixed Signal	GTL/NTL Universal PCI Mixed Signal	GTL/NTL PCI Mixed Signal	GTL/NTL PECL to 155MHz PCI Mixed Signal
Gate Capacities						
Usable (max)	5,000,000	1,500,000	1,200,000	165,000	250,000	600,000
Typical (used)	100K to 2,500K	60 to 500K	40 to 400K	20 to 75K	20 to 100,000K	40 to 300K
Power Dissipation	0.4-0.7µW/Gate/MHz	1.0µW/Gate/MHz	1.5µW/Gate/MHz	1.4µW/Gate/MHz	5.0µW/Gate/MHz	3.2µW/Gate/MHz

Source: LSI Logic/ICE, "ASIC 1997" 20405

Figure 6-13. LSI Logic ASIC Technology Trends

	G10-p	G10-i	G10-m
Product Focus	Performance (gate speed)	Maximum integration	Mainstream, low power
Target Applications	Workstations and desktop, telecomm	Servers, supercomputers, workststions	Desktop, digital video, mobile telecomm
Secondary Markets	Digital video encoding	Mobile computing	High-end consumer
Core Voltage	3.3V	2.5V	3.3V
I/O Voltages	5V compatible, 3.3V, 2.5V	3.3V, 2.5V	5V compatible, 3.3V, 2.5V
Target Design Size (gates)	100,000 to 500,000	500,000 to 2 million	100,000 to 1 million
Maximum Capacity Random Logic (gates) Memory (half die, Mbits)	 3.5 million 8	 5 million 10	 5 million 10

Source: LSI Logic/EDN/ICE, "Status 1997" 20406

Figure 6-14. LSI Logic's G10 Product Sub-Families

- In May 1996 Mitsubishi introduced its 0.35 Micron ASIC architecture for gate arrays, embedded arrays, and cell-based ICs. Figure 6-15 describes the features of the 0.35 Micron series as well as Mitsubishi's other ASIC capabilities.

Series	Feature Size (μm, drawn)	Supply Voltage (V)	Performance (ps)	Gates (max. usable)	Power (μW/gate/MHz)
0.35 Micron	0.35	3	101 (1)	2,000K	0.9 (3)
Ultra Performance	0.50	3	145 (1)	700K	1.3 (3)
Micro Power	0.50	3 (5V I/O)	200 (1)	500K	0.8 (3)
5 Volt	0.60	5 (or 3)	190 (2)	400K	2.2 (4)
M6007x/8x	0.80	5 (or 3)	215 (2)	250K	2.2 (4)

(1) 2-NAND, 3.3V, F.O. =2, 2mm Al
(2) 2-NAND, 5.0V, F.O. =2, 2mm Al
(3) 2-NAND, 3.3V, F.O. =1
(4) 2-NAND, 5.0V, F.O. =1

Source: Mitsubishi/ICE, "ASIC 1997" 21201

Figure 6-15. Mitsubishi's ASIC Capabilities

- NEC introduced its cell-based 0.35μm CMOS ASIC technology (CB-C9) in 4Q95. The CB-C9 technology is based on the company's CMOS-9 architecture that has been used in the fabrication of gate arrays since mid-1995. Volume production of CB-C9 devices began in 1Q96. Some key aspects of the process are given below.

Technology:	0.35µm drawn (0.27µm effective) gate length
Metal Layers:	2 or 3
Raw Gates:	80K to 3.5M
Usable Gates:	50K to 1.6M
Pad Count:	104 to 1,200
Performance:	113ps at F/O=2, L=0.44mm, V_{dd}=3.3V
	151ps at F/O=2, L=0.44mm, V_{dd}=2.5V
Special Macros:	ARM7 RISC MPU, V30MX (Intel 286 compatible), multiplier, PLL, A/D and D/A, Rambus interface

- NEC announced its QB-8 BiCMOS ASIC technology incorporating a new proprietary gate architecture called "PUZZLE" (discussed earlier).

- Oki Electric licensed the ARM7 32-bit RISC microprocessor core from Advanced RISC Machines to design into ASIC devices.

- In November 1995 Samsung announced it had licensed DSP Group's PineDSPCore. The core is being used for 0.6µm- and 0.5µm-based communications, multimedia, and embedded control ASIC products.

- In 3Q95 SGS-Thomson introduced the first member (ST20C4) of its 0.5µm 32-bit RISC core processor (40MIPS at 50MHz) family. SGS-Thomson also introduced its ST486DX core for ASICs, which can run at up to three times the bus clock speed (maximum internal speed of 120MHz). The ST486DX core is based on a 0.35µm five-layer-metal CMOS process.

- Symbios Logic licensed the ARM7TDMI "Thumb" 32-bit RISC microprocessor core from Advanced RISC Machines.

- In May 1996 Texas Instruments introduced what it calls its Timeline Technology (Figure 6-16) for building ASICs with 0.18µm linewidths (L_{eff}) and 125 million transistors on a chip. The Timeline technology is slated to be in volume production in 1H97.

Density: 20 million gates, 125 million transistors

Process: 0.25µm (0.18µm effective channel length) CMOS

Cores Available: DSPs, MCUs, ASIC logic, SRAM, Flash, and DRAM

Target Applications: Wireless telecom, workstations, audio/visual systems, and hard disk drives

Availability: Beta testing late 1996, volume production 1H97

Source: ICE, "ASIC 1997" 21043

Figure 6-16. TI's "Timeline" ASIC Technology

- Texas Instruments added to its TCG Series of ASICs, the TCG4000 series of gate arrays and the TEG4000 series of embedded arrays. The arrays are manufactured using a four-level-metal 0.35µm CMOS process and offer up to 1.7 million usable gates.

- Toshiba described its new TC220 0.3µm drawn CMOS ASIC process in 4Q95. Some characteristics of this technology are shown below.

Production volumes:	3Q96
Technology:	0.35µm drawn CMOS
Metal Layers:	Two or three
Raw Gates:	Up to 3M
Usable Gates:	1.9M on a 17.5mm x 17.5mm die

- In 3Q95 Toshiba introduced its TC203 0.4µm CMOS family of ASICs for mixed 3V/5V operation. The family offers up to 690K usable gates.

- Vitesse unveiled its new GLX™ family of 0.5µm GaAs-based gate arrays (discussed earlier).

A noticeable trend in the preceding announcements is that ASIC technology is definitely entering the deep-submicron realm (issues concerning deep-submicron technologies are covered later in this section).

While 0.35µm ASICs will represent only a small portion of the total ASIC market through 1996, VLSI Technology and Hitachi envision fast rising demand for the technology, from many different system segments (Figure 6-17). As shown in Figure 6-18, the average gate density of the five system categories included is forecast to rise from about 35K gates in 1993 to 1.4M gates in 1997. Moreover, average performance of these five segments is forecast to surge from 35MHz to 150MHz over the same timeperiod. There is little doubt that million-plus gate devices operating at 150MHz or higher will demand 0.35µm technology.

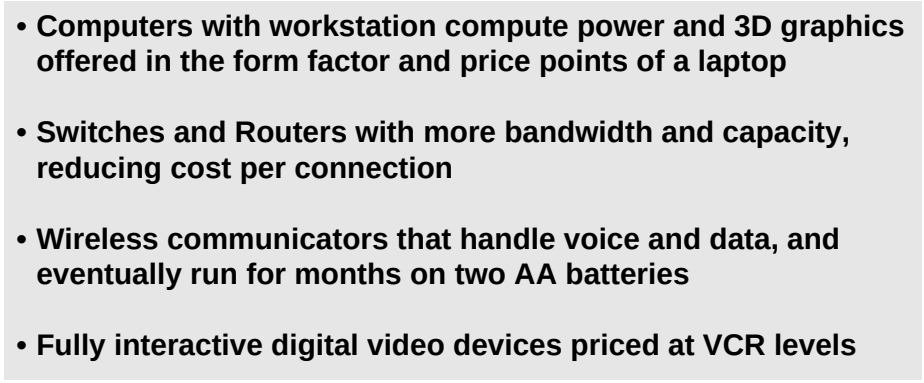


Figure 6-17. Market Impact of 0.35µm Cell-Based ASICs

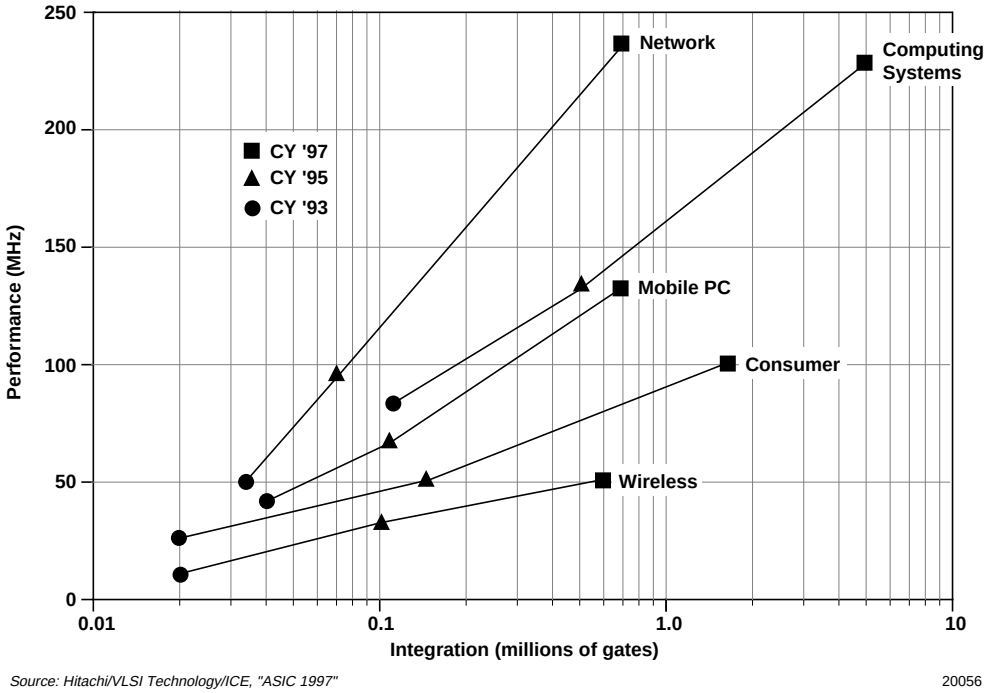


Figure 6-18. New Digital Markets for Advanced Cell-Based ASICs

As shown in Figure 6-19, the rapid increase in gate density and clock frequency in advanced ASIC devices is driving the need for new packages, like the ball grid array (BGA), that can support the requirements for higher pin counts and improved heat dissipation.

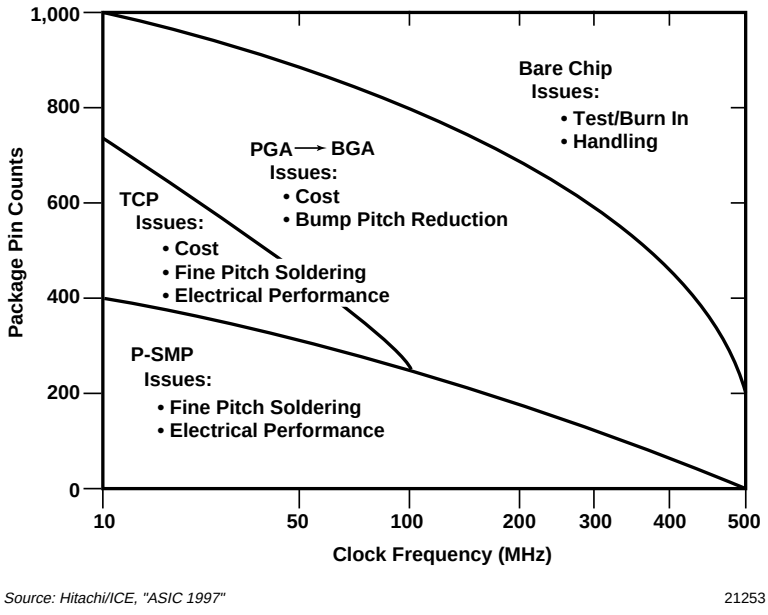


Figure 6-19. Advanced ASICs Need Advanced Packages

PLDs AND FPGAs

The first field programmable logic devices were introduced almost 25 years ago. Figure 6-20 shows a programmable logic device timeline with product introduction highlights labeled. Basically, the benefits of using programmable logic have been shortening time to market and risk reduction. This has been true for over 20 years and will continue to be true in the foreseeable future.

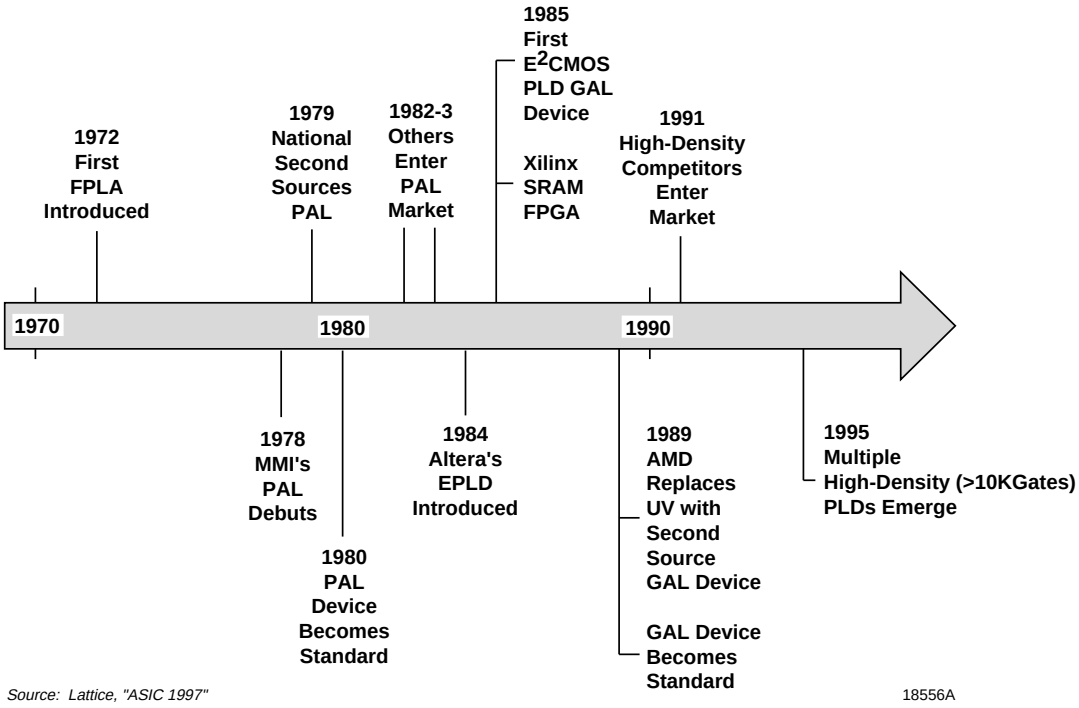


Figure 6-20. Programmable Logic History

Figure 6-21 shows how PLDs fit in an overall logic alternative comparison. As was mentioned, "development lead time" and "ease of design changes" are where PLD technology shines.

Over the twenty years of programmable logic offerings, the term PLD has evolved to encompass more than just low-density bipolar products. The PLD industry has gone from using strictly bipolar technology and simple architecture to using CMOS EPROM, EEPROM, SRAM, flash, and antifuse processing with very elaborate circuit designs.

In an industry as dynamic as the IC industry, the natural trend has been toward high-density and high-performance technologies. In the PLD market this is very obvious as simple bipolar PLDs are now steadily losing marketshare to the more flexible and higher density CMOS PLD technologies.

Criterion	Standard Components	PLDs	Gate Arrays	Standard Cells	Full Custom
Time to market	Short/medium	Short	Medium	Medium	Long
Development lead time	Immediate	Immediate	Weeks/months	Weeks/months	Years
Development cost	None	Low	Medium/high	Medium/high	Very high
Availability	High	High	Medium	Medium	Low
Available sources	Many	Many	Few	Few	Few
Volume independence (sensitivity)	Low	Low	High	High	High
Application support	Much	Much	Some	Some	None
Architectural flexibility	Low	Medium/high	High	Higher	Highest
Ease of design changes	Medium	High	Low	Lower	Lowest
Performance	Low/medium	Medium	High	High	Very high
Density	Low	Medium	Very high	Very high	Very high
Solution efficiency	Low/medium	Low	High	High	Very high
Cost of design changes	Low	Medium	High	High	Very high

Source: AMD / ICE, "ASIC 1997" 18557A

Figure 6-21. Selection Criteria for Different Logic Alternatives

Provided in Figure 6-22 is a representative selection of high-density PLDs and FPGAs available on the market. Figure 6-23 shows the PLD gate densities expected to be achieved by the end of the decade. The figure also shows that along with the large increases in PLD gate density come some of the same "design productivity" issues that the gate array and cell-based ASIC suppliers must deal with. Luckily, the programmable logic design tool industry can pull some productivity enhancement strategies from existing gate array and cell-based tools.

Company	Device Family	Density Range (usable gates)	Highest Density Available (as of mid-1996)
Actel	3200DX	6,500 - 40,000	32200DX (20,000)
Altera	FLEX 10K	10,000 - 100,000	EPF10K100 (100,000)
Atmel	AT6000	2,000 - 20,000	AT6010 (20,000)
Cypress	Ultra38000	7,000 - 20,000	CY7C38012 (12,000)
Gatefield	GF100K	9,000 - 100,000	GF51K (51,000)
IBM	Series 10000	8,000 - 42,000	IBM10016 (16,000)
Lattice	ispLSI 6000	up to 25,000	ispLSI 6192 (25,000)
Lucent Technologies	ORCA Series	4,000 - 60,000	ATT2C40 (40,000)
Motorola	MPA1000	3,500 - 22,000	MPA1100 (22,000)
QuickLogic	pASIC2	3,000 - 20,000	Q12020 (20,000)
Xilinx	XC4000	28,000 - 125,000	XC4052EX (52,000)

Source: ICE, "ASIC 1997" 21254

Figure 6-22. High-Density PLD/FPGA Offerings

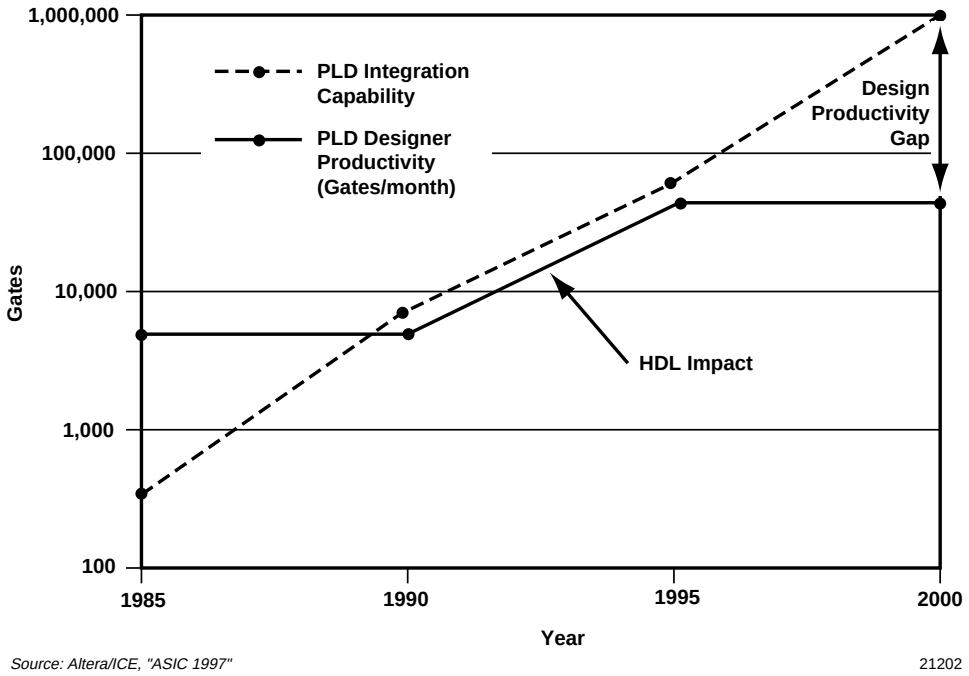


Figure 6-23. PLD Design Productivity Gap

As was discussed in Section 4, the CMOS CPLD and FPGA markets have been and will continue to be the star performers in the ASIC marketplace. This stellar growth has caused a significant increase in competition, which in turn has spurred a steady stream of new product innovations and introductions.

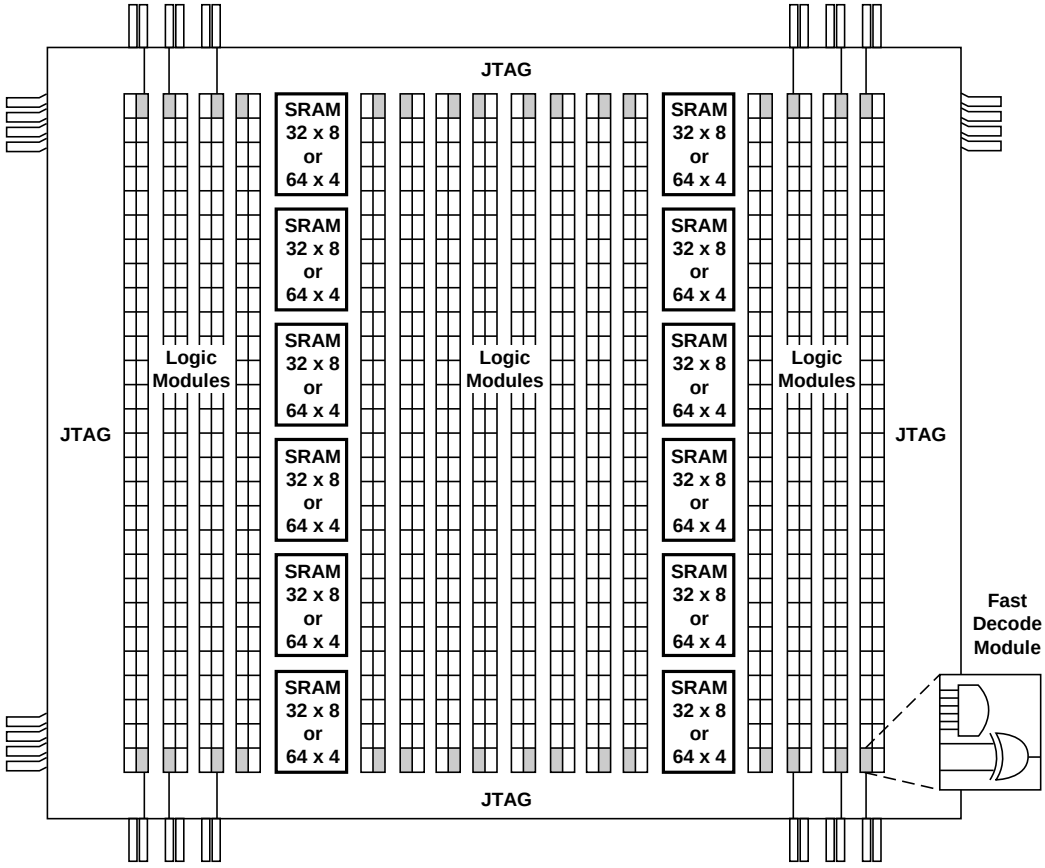
Shown below is a sampling of some of the major PLD technology announcements made since mid-1995.

- Actel and Synopsys are jointly developing what they call system programmable gate arrays (SPGAs), which combine on one die an FPGA and Synopsys' cell-based array (CBA). SPGAs will give users access to both the field programmability of an FPGA and the high performance and system integration capabilities of an ASIC. Actel expects that by 2000, 20 to 25 percent of its revenues will be from SPGA sales.

- Actel introduced a series of radiation-hardened FPGAs designed for use in commercial satellites. The 0.8µm CMOS devices are offered in densities ranging from 2,000 to 8,000 gates.

- Actel signed an agreement with intellectual property provider Technical Data Freeway (TDF) that gives Actel a wide range of synthesizable cores to be used in Actel devices. The cores include DSPs and MCUs, as well as telecom and multimedia cores.

- Actel introduced its 3200DX family of PLDs in 3Q95. Initially offered in 0.6µm technology, the family moved to 0.5µm processing in early 1996. Members of the 3200DX family are able to incorporate blocks of high-speed (5ns) dual-port SRAM (Figure 6-24).



Source: Actel/ICE, "ASIC 1997" 20409

Figure 6-24. Actel's 3200DX FPGA Architecture

- Altera announced it is using a patented redundancy technology to increase the wafer yields of its high-density CPLDs by more than 40 percent. The technology adds an extra, unconnected logic block on each die on a wafer that can be wired into the CPLD to replace a defective section.

- Altera announced the availability of the industry's highest density PLD, a 100,000-usable-gate version of its FLEX 10K architecture. The FLEX 10K100 has over 10 million transistors and a die size of over 600K square mils. The company says the key to achieving the high density is an embedded architecture, which allows the implementation of logic functions in the logic array blocks (LABs), as well as memory and specialized logic functions (e.g., multiplier, ALU, and DSP) in embedded array blocks (EABs).

- Altera announced its MegaCore function library of preverified system-level building blocks (Figure 6-25). The company also launched OpenCore, a program that allows designers to "test drive" the megafunctions before licensing them. The MegaCore library complements the Altera Megafunctions Partners Program (AMPP), launched in late 1995.

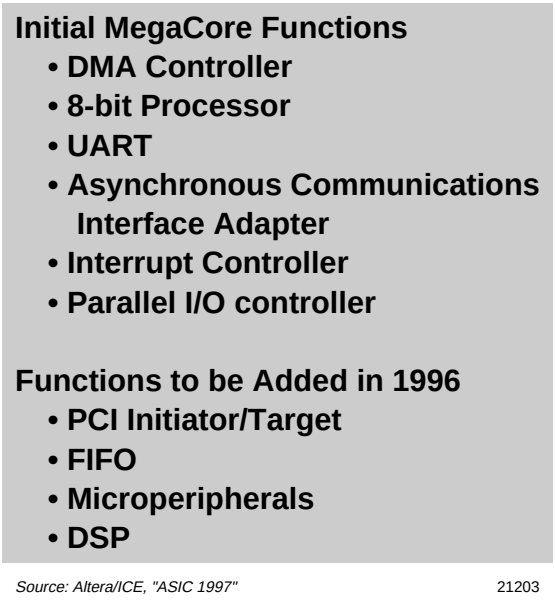


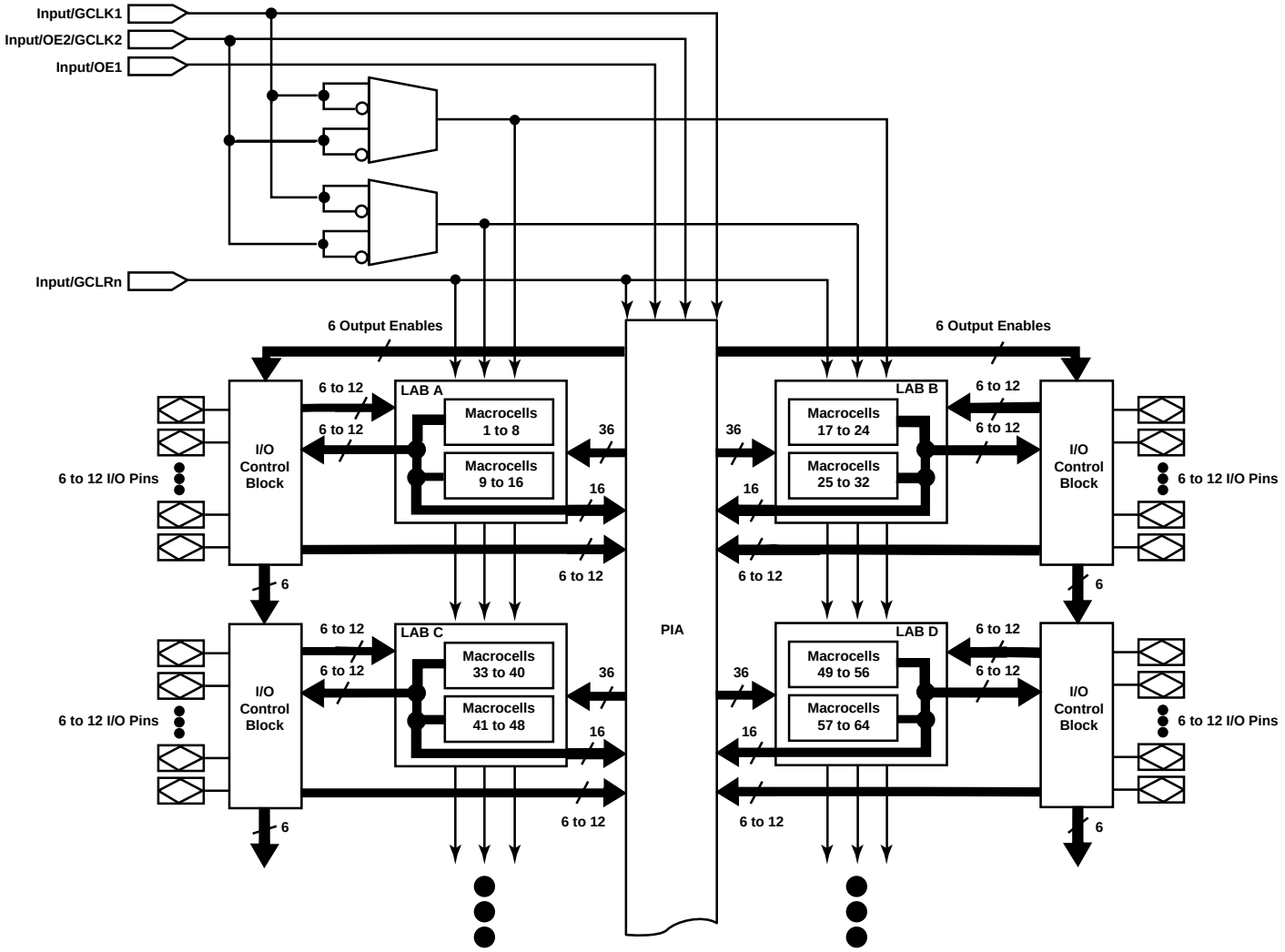
Figure 6-25. Altera Announces MegaCore Functions Library

- Altera spruced up its MAX7000 line of PLDs with the addition of in-system programmability features (Figure 6-26). The new MAX7000S family includes chips with between 2,500 and 12,000 usable gates and offered in 7.5ns, 10ns, and 15ns speed grades.

- AMD added devices to its MACH CPLD family featuring in-system programming capabilities. The chips feature speeds as fast as 7.5ns (pin-to-pin) and are said to be PCI compatible.

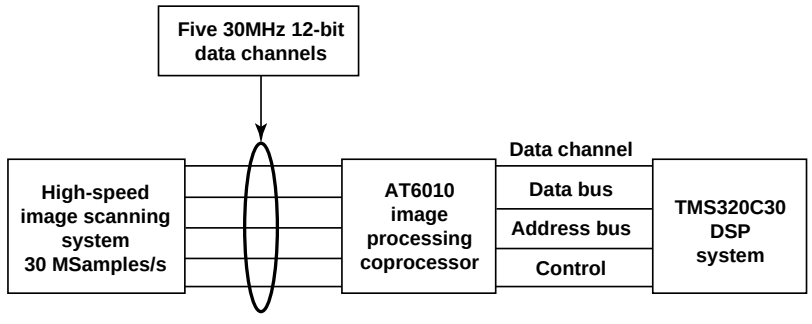
- Atmel unveiled the AT6010, a member of its AT6000 FPGA family, which is based on the company's Cache Logic architecture. The 20,000-gate AT6010 features 6,400 registers and supports system speeds of 100MHz, making it well suited to process DSP functions. Atmel is, in fact, marketing the device as a DSP coprocessor (Figure 6-27).

- Crosspoint Solutions unveiled its CP100K family of CrossFire™ FPGAs having densities up to 100,000 gates. CrossFire is a proprietary sea-of-gates architecture that allows 60-80 percent gate utilization. The FPGAs will initially be implemented in a 0.5µm 3/4-layer metal CMOS process, with plans for a migration to 0.25µm technology resulting in chips at 250K and beyond gate levels. The CrossFire family is supported by a set of system-level cores, such as DSP engines, graphics accelerators, and ATM framers.



Source: Altera/ICE, "ASIC 1997" 21255

Figure 6-26. Altera's New MAX7000S PLD



Source: Atmel/ICE, "ASIC 1997" 21250

Figure 6-27. Atmel Targets AT6010 at DSP

- Cypress entered the PLD core business with the introduction of a synthesizable VHDL PCI target core in July 1996. The company's core program has been named UltraCore.

- Cypress enhanced its Flash370 CPLD product line to create the new Flash370i family. The 370i chips add in-system reprogrammability, a new technique for controlling noise in bus-oriented I/Os, PCI-compliant outputs, and automatic power reduction.

- Cypress introduced the PALCE20V8, a flash erasable and reprogrammable device manufactured using the company's 0.65µm flash CMOS technology.

- Cypress introduced a new generation of its advanced UltraLogic™ FPGAs, the Ultra38000 family. The antifuse-programmed devices are fabricated using a 0.65µm three-layer metal CMOS process and are available with up to 20,000 usable gates in 1,440 logic cells with 336 I/Os. QuickLogic is Cypress's antifuse FPGA second-source partner.

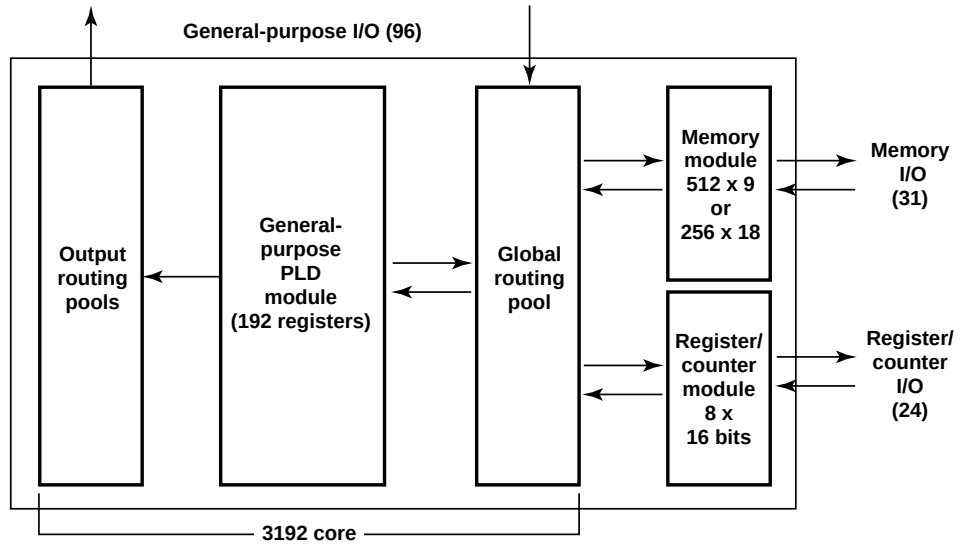
- IMP introduced the second member of its electrically programmable analog circuit (EPAC™) family. The new chip integrates the functions of over 18 discrete analog and digital CMOS IC components, providing user-configurable monitoring, diagnostic, and data acquisition features.

- Lattice Semiconductor extended its ispLSI 2000 line of CPLDs to include 3.3V devices. The family of low-voltage parts offer gate densities from 1,000 up to 6,000 and operating speeds as fast as 10ns (80MHz). Device specifications also feature 100,000 erase/write cycles.

- Lattice added three members to its ispLSI family that feature integrated predefined, function-specific memory and counter-timer megacells (Figure 6-28). The three versions include either a single-port SRAM, a dual-port SRAM, or a FIFO.

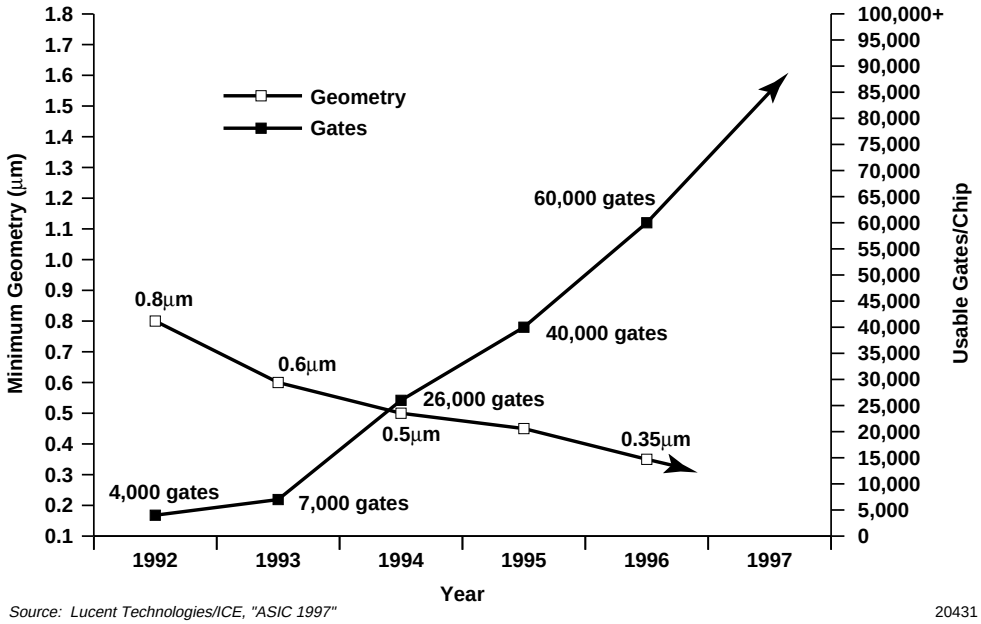
- Lattice announced a pair of very fast GAL PLDs, both operating at 3.3V. The GAL22LV10D is rated at a 4ns propagation delay and 3ns clock-to-out time, making possible 182MHz state machines. The GAL22LV8D features a 3.5ns propagation delay, a 2.5ns clock-to-out delay, and a 200MHz frequency.

- Lucent Technologies unveiled its 0.35µm CMOS process technology, which is optimized for ASICs and FPGAs. The new technology will support designs of 2.5 million usable gates, 200MHz system frequencies, and 1G/sec. I/O interfaces. The first product implementation is a series of ORCA™ FPGAs with gate counts ranging from 4,000 up to 60,000 (Figure 6-29).



Source: Lattice Semiconductor/ICE, "ASIC 1997" 21251

Figure 6-28. Lattice ispLSI Family Turns Application-Specific



Source: Lucent Technologies/ICE, "ASIC 1997" 20431

Figure 6-29. Lucent Technologies' FPGA Density and Feature Size Trends

- Microcontroller and nonvolatile memory manufacturer Microchip Technology entered the programmable logic market through the acquisition of ASIC Technical Solutions (ATS) of San Jose, California. ATS provides its QuickASIC array family which replaces FPGAs and CPLDs with a masked ASIC at a reduced price.

- Motorola announced its long-anticipated entry into the programmable logic market in April 1996, with the introduction of new FPGAs based on technology licensed from Pilkington Micro-Electronics in the U.K. The first devices in the Motorola Programmable Array (MPA) family are available with as many as 14,200 gates. They are reprogrammable SRAM-based products manufactured on a standard 0.6µm triple-layer metal CMOS process. In late 1995, Motorola announced it had also licensed Pilkington's field-programmable analog array (FPAA) technology.

- Long-time simple PLD player, Philips Semiconductors announced its entrance into the complex PLD market in April 1996 by forming a new CPLD business unit to sell its new high-performance, low-power 3.3V devices. The new "CoolRunner" CPLDs are an extension of the PLA architecture called eXtended Programmable Logic Array (XPLA). The devices feature a design technique called Fast Zero Power (FZP), which provides low static (≤100µA) and dynamic power (50mA @>100MHz).

- Space Electronics Inc. (SEI) introduced a radiation-hardened FPGA for space-borne applications, such as satellites, space craft, rockets, and probes. SEI's device is based on a 0.65µm CMOS antifuse process and is available with densities ranging from 2,000 to 9,000 gates. It also features chip-to-chip operating speeds of up to 135MHz with output delays of 3ns.

- Citing the strong market acceptance of SRAM and flash technologies, Xilinx announced in late July, 1996 that it would discontinue its XC8100 family of one-time programmable antifuse FPGAs.

- Xilinx inaugurated its LogiCore program, which offers a PCI bus controller module as well as third party software including DSP filters, bus interfaces, UARTs, and DMAs for various Xilinx PLDs.

- Xilinx unveiled its XC4000EX family of FPGAs, which feature between 28,000 and 62,000 nominal gates. The high density is accomplished through the use of a 0.5µm process and significant architectural changes. As shown in Figure 6-30, the major architectural difference between the XC4000EX and the older XC4000E is the approximate two-fold increase of routing resources available to the logic cells. The density of the 4000EX FPGAs will increase to 125,000 gates in 1997 when Xilinx moves to a 0.35µm process.

There is an increasing number of PLDs that are being tailored for specific applications. In fact, nearly every major PLD/FPGA supplier has recently announced the availability of a library of system-level cores/megacells that can be embedded in their device designs, thereby allowing PLDs to be used as system-level chips. Blocks of circuitry that can be embedded in some of today's PLDs include SRAMs, ROMs, ALUs, DSP filters, and even MPU and MCU functions.

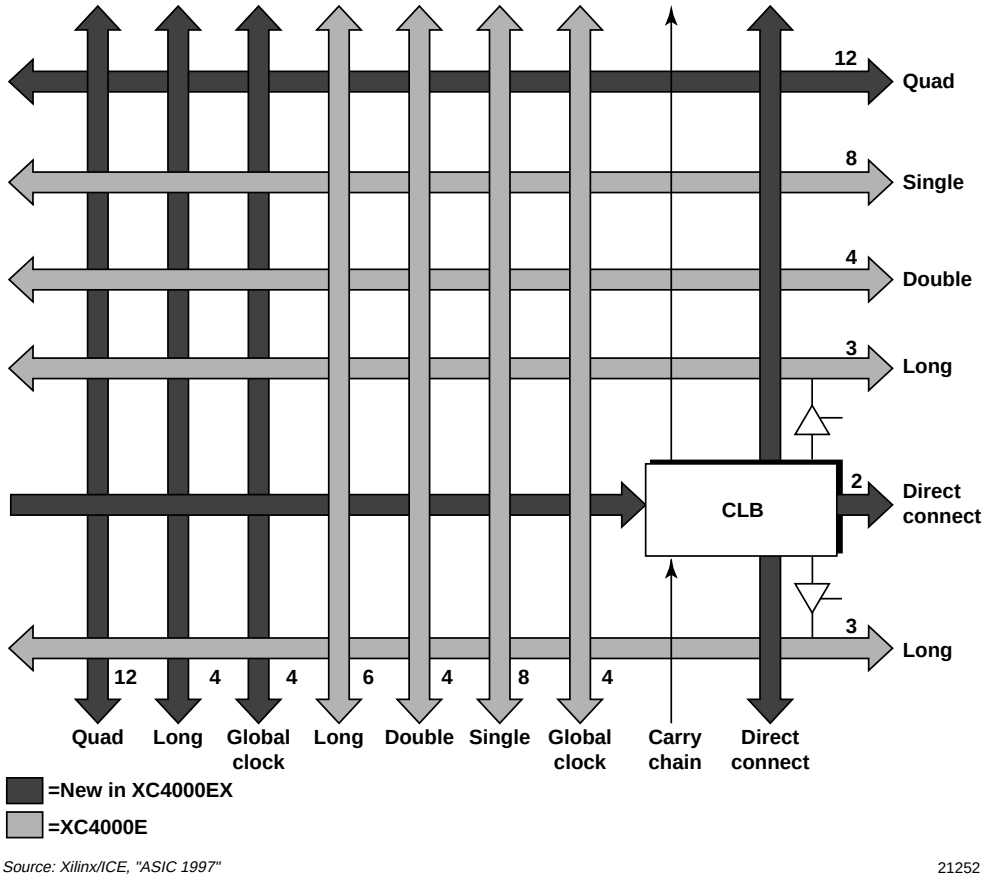


Figure 6-30. Xilinx XC4000EX Family Architectural Enhancements

Embedded functionality is opening up a variety of new applications for PLDs, including Asynchronous Transfer Mode (ATM) data communications, Peripheral Component Interconnect (PCI), and DSP functions such as filtering. Some of the companies offering DSP-tailored PLDs include Altera, Atmel (AT6000 FPGAs), and Xilinx (XC4000 series).

The topic of PLDs offering in-system-reprogrammability features is one that surfaced only a relatively short time ago (1994). It has been stated by Lucent Technologies that there are three major benefits of logic reconfigurability: "first, to meet standards, which are evolving and therefore are in a constant state of flux; second, to keep up with system functionality changes; and third, to accommodate multiple data formats in a singe device."

Atmel describes its reconfigurable logic as "cache logic." Since much of a system's hardware logic is idle at a given time, the ability to reconfigure the logic on-the-fly to optimally serve the software's immediate computational requirements can greatly accelerate the performance of the system.

Some possible early system applications for reprogrammable logic include telecommunications, geophysical information processing, medical imaging, and computer architecture simulation. In the telecommunications area one can easily envision the need for a PLD device to dynamically reconfigure itself to accommodate multiple interface or telecommunications protocols and standards (Figure 6-31).

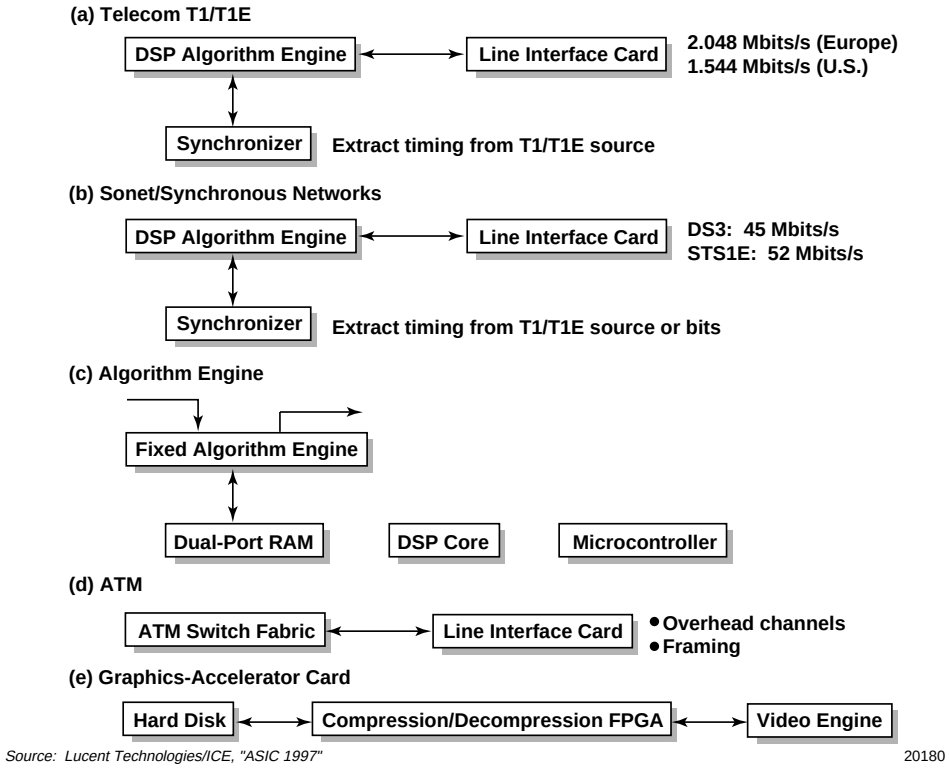


Figure 6-31. FPGA Can Reconfigure to Meet Various Standards

As another example of a reconfigurable application, Altera states that its reprogrammable PLDs can be configured as a display accelerator or circuit simulator as needed. Altera says "that by using reprogrammable logic the potential exists to configure the hardware for more direct processing of the data."

Xilinx has stated that it believes the reconfigurable systems market will grow to more than $1 billion in sales by the end of the decade with the FPGA chip portion estimated at approximately $200 million.

There is little doubt that reconfigurability will be a powerful tool to enhance a system's efficiency. Still, it should be noted that in-system-reconfigurable PLD logic is still in its infancy. Current design tools and programs are still not sufficient to manage dynamically reconfigurable hardware efficiently. However, as system designers continue to explore ways to increase system performance, ICE expects that reconfigurable PLDs will find an increasing market to serve.

In general, the MOS PLD market will continue to be one of the most dynamic in the entire IC industry. As PLD technology and capabilities increase, ICE expects the PLD logic segment to be a cornerstone of the ASIC industry. Some key PLD developments to watch for throughout the remainder of 1996 and into 1997 include:

– Implementation of 0.35µm feature size technology.

– Increased offerings of high-gate-count devices.

– Migration of PLD propagation delays to as low as 3.5ns (or lower) and operating frequencies as high as 200MHz.

– Further offerings of specialized core cells for PLDs.

– Additional development of in-system-reprogrammable infrastructure (hardware and software).

ASIC PROCESS TECHNOLOGY ISSUES

In the mid-1980's, ASIC devices were typically using process technology that was 2-3 years behind high-volume memory part types (Figure 6-32). Today, however, processes rivaling the technological advancement of state-of-the-art memory devices are being developed specifically for ASICs. As an example, Figure 6-33 shows Toshiba's DRAM and ASIC technology convergence. Notice also in Figure 6-34 how Mitsubishi's ASIC process roadmap parallels its DRAM development.

While deep submicron integration has allowed for unprecedented performance and economies of scale, it has also brought with it a new set of design challenges. With larger geometry chips, circuit timing is limited primarily by gate delays. However, as geometries shrink, delay from the resistance and capacitance of the wiring interconnect between transistors begins to dominate (Figure 6-35). Interconnect delays have increased, as a percent of total delay, from 15-30 percent at the 1.0µm level to 50-75 percent at the 0.35µm level.

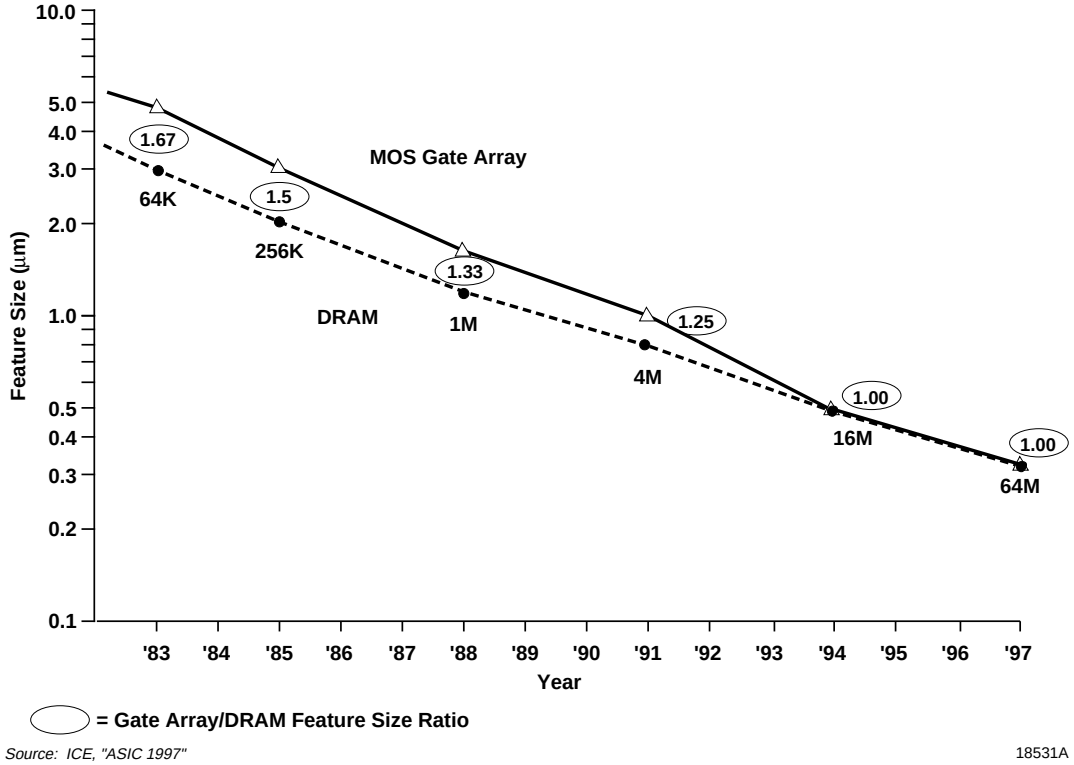


Figure 6-32. ASICs Narrow Technology Gap

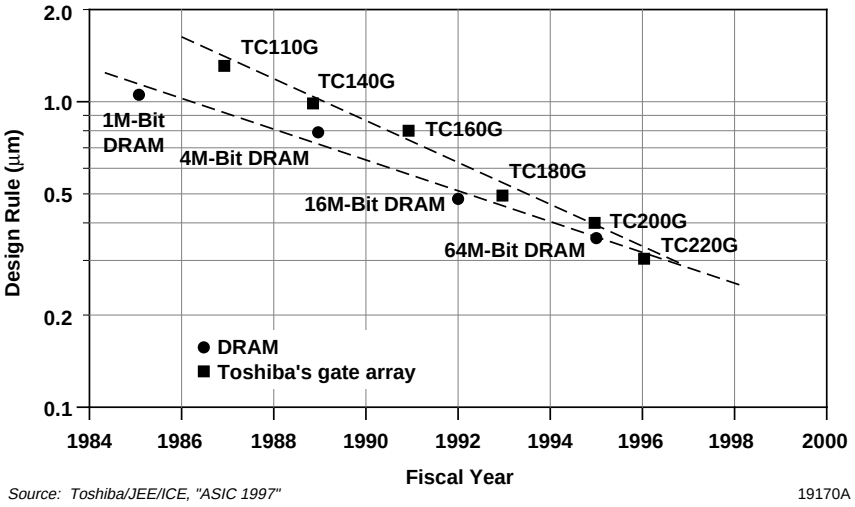
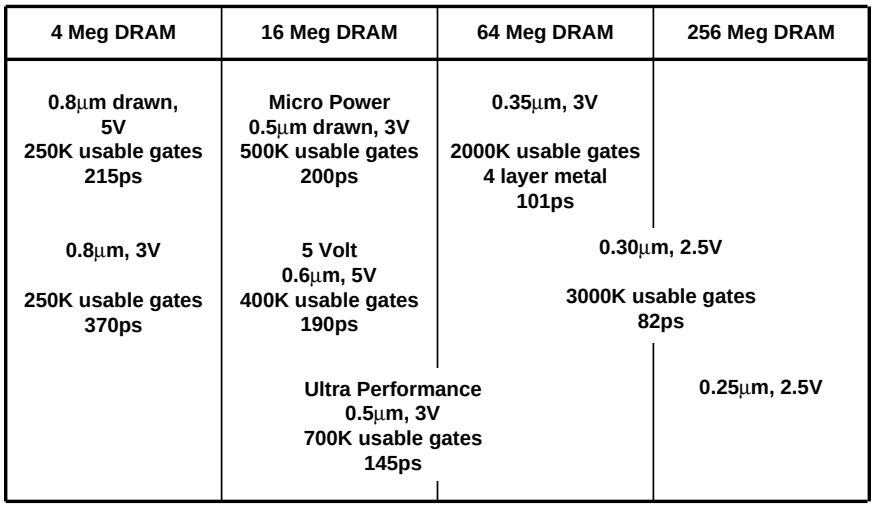
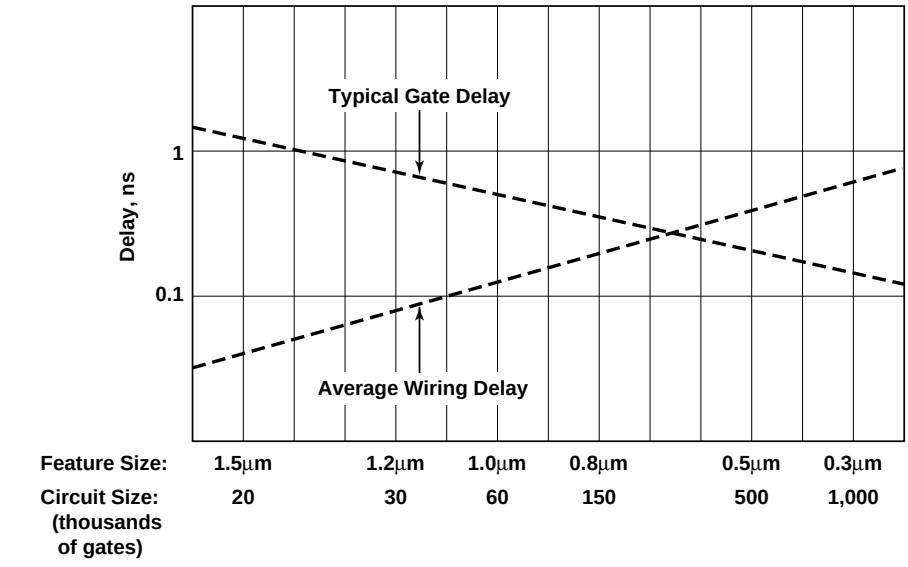


Figure 6-33. Transition of the DRAM and Toshiba's Gate Array Development



Source: Mitsubishi/ICE, "ASIC 1997" 21199

Figure 6-34. Mitsubishi's ASIC Roadmap



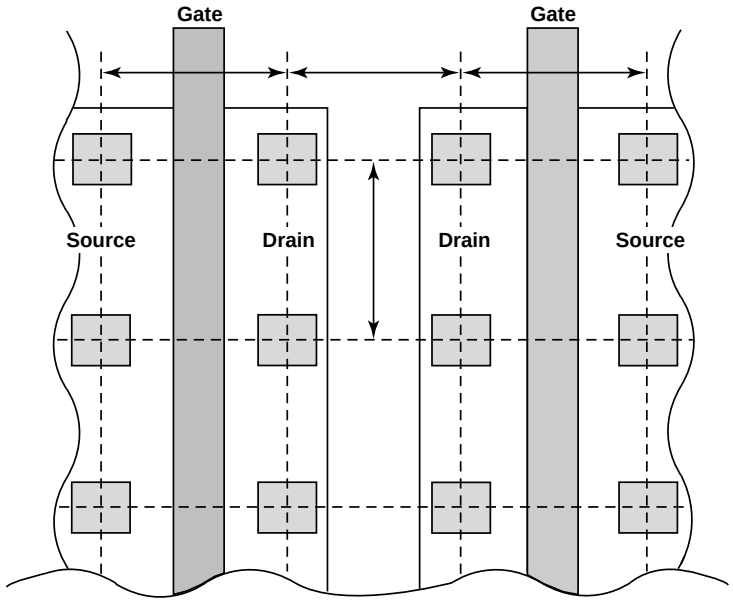
Source: OKI Semiconductor/ICE, "ASIC 1997" 20407A

Figure 6-35. Wiring (Interconnect) Delay Versus Gate Delay

In battling the effects of increased resistance and capacitance associated with increasingly thinner, narrower, and more closely spaced interconnects, ASIC designers are having to spend more and more design iterations identifying and solving timing errors; or else, settle for a design that doesn't use the full speed potential of the silicon to get a functional chip. Design issues are discussed later in this section.

Other challenges intensified by shrinking circuit geometries include limiting crosstalk between interlayer and adjacent wires, managing I/O issues like simultaneously switched outputs, and minimizing clock skews.

Deep-submicron technology has also decreased the significance of gate length when it comes to determining MOS circuit density. A more accurate indicator is metal pitch, which is defined as the sum of the metal line width at a via and the space between the via and an adjacent line. It is a measure of how closely the metal lines can be placed together. Thus, as shown in Figure 6-36, metal pitch sets the drain-to-source pitch in an individual transistor and the drain-to-drain pitch of isolated transistors.



Source: Computer Design/ VLSI Technology/ICE, "ASIC 1997" 21244

Figure 6-36. Influence of Metal Pitch on Deep-Submicron Device Layout

Furthermore, ASIC cell libraries are generally based on some fixed multiple of the metal pitch. That is to say, when library elements are placed and routed, the interconnect line lengths are multiples of the interconnect metal grid. Thus, metal pitch, not gate length, determines cell dimensions and library elements shrink proportionally to the pitch. Figure 6-37 provides a list of typical metal pitch measurements for several submicron technology generations.

Technology Generation (μm)	Metal Pitch (μm)	Number of Layers
0.6	3.0 - 2.4	3
0.5	2.4 - 1.8	3 - 4
0.35	1.8 - 1.2	3 - 5
0.25	1.2 - 0.8	3 - 5

Source: Computer Design/ VLSI Technology/ICE, "ASIC 1997" 21245

Figure 6-37. Typical Metal Pitch Measurements

The following bullets are summaries of several advanced ASIC process technologies that were discussed at the IEEE 1996 Custom Integrated Circuits Conference (CICC).

- Hitachi discussed the development of a 1.86-million-gate CMOS gate array with high-speed GTL I/O circuitry. Based on a 0.35μm process, the device is said to be capable of transmitting synchronous data through a 30cm line at a rate of 300MHz. The features of the channelless gate array are shown below.

  Raw Gates: 1.86M
  Usable Gates: 1.0M
  Metal Layers: 5
  Metal Pitch: 1.4μm (metal 1 to metal 3)
  Gate Oxide: 80Å
  Die Size: 14.75 x 14.75mm
  Power Supply: 3.3V
  Package: 400-pin PGA

- Lucent Technologies' Bell Laboratories presented a paper describing a manufacturable and high-performance 0.35μm CMOS ASIC technology optimized for 3.3V operation. The company claims the technology provides an improvement of 1.6X in circuit performance and 1.56X in packing density over Lucent's previous generation 0.5μm 3.3V CMOS technology. A comparison of the device parameters for the two technology generations is provided in Figure 6-38. Circuits that have been fabricated using the 0.35μm architecture include gate arrays, internal AT&T standard cell designs, a 256K SRAM development vehicle, and the company's ORCA FPGA.

Parameter	0.35μm CMOS	0.5μm CMOS
V_{DD}	3.3V	3.3V
t_{ox}	65Å	90Å
V_{th} (NMOS)	0.6V	0.6V
V_{th} (PMOS)	0.85V	0.9V
I_{ON} (NMOS)	600μA/μm	425μA/μm
I_{ON} (PMOS)	300μA/μm	180μA/μm
L_{poly} (NMOS)	0.36μm	0.5μm
L_{poly} (PMOS)	0.40μm	0.6μm
I_{off} at 125°C	< 1nA/μm	< 1nA/μm
Ring Oscillator	50ps	82ps
2–NAND FO = 2	94ps	144ps

Source: Lucent Technologies/ICE, "ASIC 1997" 21246

Figure 6-38. Comparison of Lucent's 0.35μm and 0.5μm Processes

- Motorola described a thin-film silicon-on-insulator (TFSOI) complementary BiCMOS technology for low-power RF mixed-mode applications, such as portable wireless communications equipment. The technology is based on a manufacturable, near-fully-depleted 0.5μm CMOS process with integrated lateral bipolar circuitry. Some of the device parameters are given below.

Bipolar Transistors	NPN	PNP
SOI Thickness:	0.1μm	0.1μm
Emitter Size:	0.72μm2	0.72μm2
Peak Current Gain:	65	40
Peak f_T:	14GHz	9GHz

CMOS Transistors	NMOS	PMOS
SOI Thickness:	0.1μm	0.1μm
Gate Oxide:	105Å	105Å
Gate Length (eff.):	0.44μm	0.45μm
Threshold Voltage:	0.51V	0.45V
Sat. Current (@3.0V):	310μA / μm	140μA / μm
Peak f_T:	16GHz	

- NTT LSI Laboratories, Kanagawa, Japan, described a 0.25μm SIMOX-CMOS gate array architecture with an LVTTL interface (2.0V-1.2V). Figure 6-39 shows that at low voltages, SIMOX (separation-by-implantation-of-oxygen) silicon substrates offer a speed advantage over bulk silicon substrates. Some of the device features are provided below.

Gate Length:	0.25µm
Threshold Voltage:	0.2V (NMOS), 0.3V (PMOS)
Gate Oxide:	50Å
Saturation Current:	359µA / µm (NMOS), 203µA / µm (PMOS)
Metal Pitch:	1.4µm (metal 1 to metal 4)
Die Size:	100mm2
Gate Count:	300K
I/O Count:	340 (105µm I/O pitch)
Power Supply:	3.3V, VDD (≤2.0V)

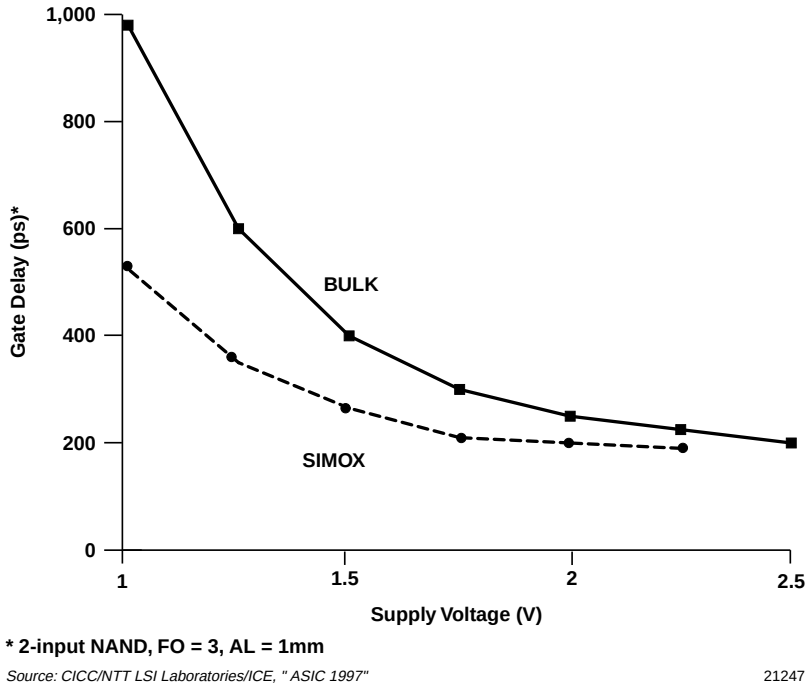


Figure 6-39. SIMOX Offers Speed Advantage at Low Voltage

ASIC DESIGN TOOLS

With the increase in complexity and density of ASICs has come the need for higher levels of abstraction in circuit simulation in order to meet time-to-market requirements. The use of hardware-description languages (HDLs)—Verilog and VHDL—and the synthesis of these languages, has significantly improved the productivity of ASIC designers. It has been estimated that the productivity of HDL users is 3 to 10 times that of users of schematic capture when measured in terms of the number of gates created in a given timeframe.

The three primary levels of abstraction in HDL simulators are the gate (or logic) level, the register-transfer level (RTL), and the most abstract—behavioral level (Figure 6-40). While HDL tools are being readily used at each of the three levels, most are focused on the RTL level of abstraction. Provided in Figure 6-41 is a listing of companies offering HDL and other types of circuit simulation tools.

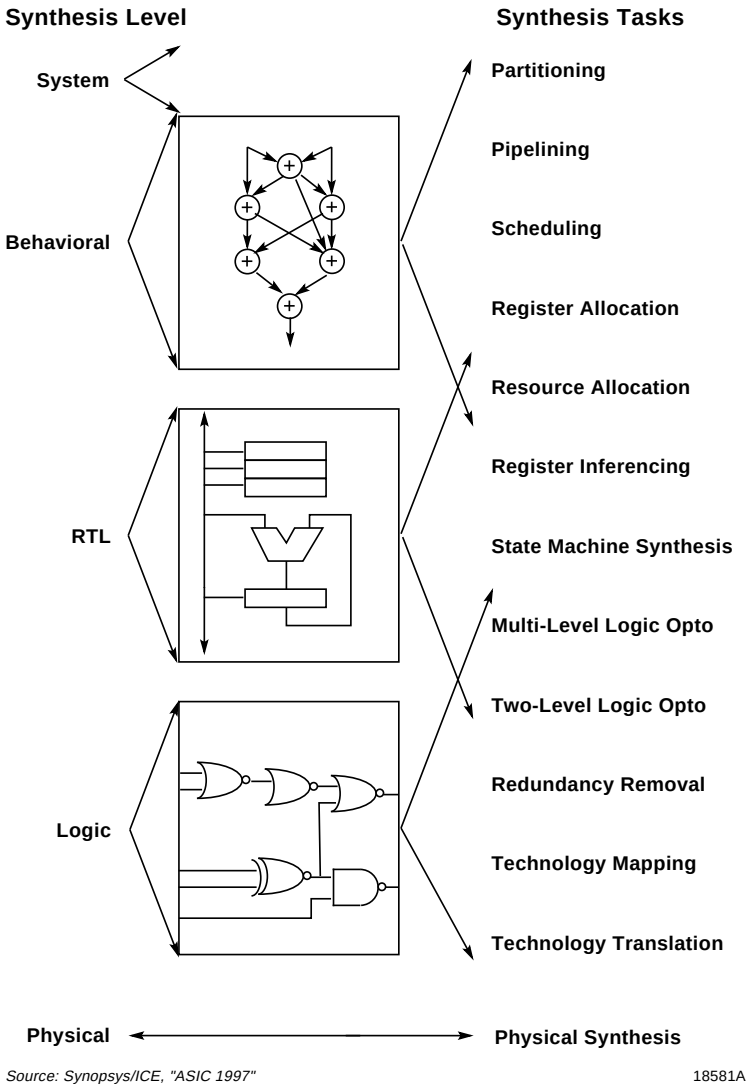


Figure 6-40. Levels of Abstraction

Company and Location	Product Name	Language	Functionality
Alta Group/ Cadence Design Automation Foster City, CA	**HDS (Hardware Design System)**	**Verilog, VHDL**	**HDS features a fast, data flow simulator that offers cycle-based simulation with a unified system-level design environment. Co-simulates with existing HDLs and generates HDL output for implementations. HDS also supports structural and behavioral design**
ANACAD Electrical Engineering Software Milpitas, CA	**ELdo**	**SPICE**	**The Eldo simulator uses an innovative Unix architecture which combines architecture which combines multiple solution algorithms for fast circuit-level simulation of mixed analog and digital designs**
	ELdoHDL	**SPICE, VHDL-A**	**The EldoHDL simulator combines the simulator with a VHDL-based analog behavioral language for fast analog simulation from circuit through system level**
	MixVHDL	**VHDL**	**The MixVHDL integrates EldoHDL with a complete VHDL simulator for fast circuit through system simulation in both analog and digital domains**
Analogy Beaverton, OR	**Saber Simulator**	**Mast**	**Saber can analyze complete systems from system through circuit-level implementations. This can include analog, digital, mixed-signal, mechanical, hydraulic, thermal or mechatronics**
	Saber/Verilog Mixed-Signal Simulation	**Mast, Verilog**	**Links Saber with Cadence Verilog for an all mixed-signal simulation system. Simulate mixed analog and digital systems using all the models of each simulator. Model and simulate behavioral, functional and primitive devices in both analog and digital domains**
	QVS	**MAST, VHDL**	**Links Saber to Mentor's QuickSim II for mixed-signal simulation system. Simulate mixed analog and digital systems using all the models of each simulator. Model and simulate behavioral, functional and primitive devices in both analog and digital domains**
	Saber/ViewSim Mixed-Signal Simulation	**MAST, VHDL, Verilog**	**Links Saber to Viewlogic's ViewSim for mixed-signal simulation system. Simulate mixed analog and digital systems using all the models of each simulator. Model and simulate behavioral, functional and primitive devices in both analog and digital domains**
Avista Design Systems Folsom, CA	**Spectre/XL**	**Spectre, SPICE Visual Basic for Applications**	**The first spreadsheet tool for analog design. Avista Spectre/XL's instant "what if" analysis gives you an accurate, flexible tool for evaluating, developing and optimizing circuit designs. Uses proven SPICE models. Requires Microsoft Excel for Windows v5.0**
Cadence Design Automation San Jose, CA	**Leapfrog**	**VHDL**	**Leapfrog is a native compiled code based VHDL simulator. It supports Verilog and Vital libraries and is integrated with Cadence products for IC/ASIC/FPGA/Board design solutions**
	Verilog-XL	**Verilog**	**High performance simulation tools integrated into full featured design environment. Supports multiple design methodologies for the design of IC/ASIC/FPGA/PLD and PCB's**
Chronologic Simulation Los Altos, CA	**VCS**	**Verilog**	**Fastest Verilog Simulator on the market VCS offers full capabilities for model development, interactive debugging, regression testing, and ASIC sign-off. OVI and IEEE compliant**
	VCSi	**Verilog**	**Easy to use interactive Verilog simulation**
	VMC	**Verilog**	**Modeling technology for secure, accurate, efficient simulation models. Protects model suppliers' intellectual property. Reduces model consumers' time-to-market**
Compass Design Automation San Jose, CA	**QSIM**	**Proprietary, Interfaces to VHDL, Verilog, EDIF**	**QSIM performs high-speed, full timing RC structural simulation of complex ASICs, utilizing ASIC vendor-specific delay models or the COMPASS input slope and RC tree delay models for accurate deep submicron gate and interconnect delays**

Source: Integrated System Design/ICE, "ASIC 1997" 21276

Figure 6-41. Circuit Simulation Tools

Company and Location	Product Name	Language	Functionality
Data I/O Corporation Redmond, CA	**Synario**	**VHDL, Verilog ABEL-HDL**	**Synario 2.1 is a Windows-based system for PLD, FPGA and board-level design. It provides mixed-entry (schematic and HDL descriptions) and HDL simulation support**
Exemplar Logic Alameda, CA	**Galileo V-System**	**VHDL**	**Fully integrated VHDL simulator with source level debugger, extensive design browsers, waveform trace, C language interface, VHDL '93 support and VITAL accelerated gate level simulation**
Frontline Design Automation San Jose, CA	**PureSpeed Developer**	**Verilog**	**The PureSpeed family of fully compliant in Verilog simulators incorporates three high-performance simulation engines–complied, interpreted and gate-level (XL) in a single kernel architecture**
	PureSpeed OverDrive	**Verilog**	**PureSpeed Developer and PureSpeed OverDrive provide complete support for PLI routines and SDF data and full command language support. All ASIC/FPGA libraries run unmodified in PureSpeed**
IKOS Systems Cupertino, CA	**Voyager**	**VHDL**	**High-performance mixed-level simulation in software and mixed-level accelerations. Includes a software solution for mixed-level fault simulation**
	Gemini	**Verilog**	**Mixed-level acceleration through a tight integration of the Cadence Verilog XL simulator with the IKOS NSIM hardware accelerator**
InterHDL Los Altos, CA	**Verilint**	**Verilog**	**Verilint is a semantics, synthesis, and coding-style checker for designs written in Verilog HDL**
	Viper	**Verilog**	**Viper is a Verilog HDL simulator which supports a powerful graphical debugging environment, and is compatible with the Verilog XL 1.6 and OVI**
	Verinet Toolkit	**Verilog**	**Verinet Toolkit is a front-end for the structural (gate-level) subset of the Verilog HDL**
	Veribase Toolkit	**Verilog**	**Veribase Toolkit is a Full Language Verilog front-end that is used to develop Electronic Design Automation applications for processing Verilog HDL designs**
	V to V	**Verilog, VHDL**	**V to V reads hierarchical designs and translates them into functionally equivalent designs covering the synthesizable Verilog**
Intusoft San Pedro, CA	**ICAP/4**	**XDL**	**Analog/mixed-signal circiut design, with IsSpice4 native mixed-mode simulator. Runs analog, digital, non-electrical, sampled-data and HDL models**
Mentor Graphics Wilsonville, OR	**Continuum**	**VHDL, HDL-A**	**Continuum, including QuickSim II and AccuSim II, is a mixed-signal simulator offering behavioral modeling for digital and analog devices and systems based on VHDL, and boundary model library for translation between analog and digital domain**
	AccuSim II	**HDL-A**	**Multi-level analog simulator to many different designs that require non-linear equation solving**
	QuickVHDL	**VHDL**	**Provides high-performance VHDL simulation, fully supporting VHDL '87 and 93 and VITAL 2.2b standards. Supports point tool and integrated design environments**
	QuickVHDL Pro System	**VHDL**	**Provides high-performance VHDL simulation, supports VHDL '87 and '93, VITAL 2.2b standards, point tool and integrated design environments. Provides co-simulation with QuickSim II**
	QuickSim II	**Proprietary**	**High-speed logic simulator permitting explortion of design functionality and performance**
	QuickHDL	**VHDL, Verilog**	**Provides mixed VHDL and Verilog simulation, supports VHDL '87 and '93, VITAL 2.2b and IEEE 1364 standards**
Meta Software Campbell, CA	**HSPICE**	**HSPICE**	**HSPICE is a cicuit simulation and analysis tool, which uses advanced transistor models to provide the optimum combination of accuracy, convergence and transistor modeling for IC designers. HSPICE is integrated into all commonly used design environments**

Source: Integrated System Design/ICE, "ASIC 1997" 21277

Figure 6-41. Circuit Simulation Tools (continued)

There has been much debate over whether VHDL (VHSIC [very high speed integrated circuit] HDL) or Verilog will become the dominant HDL tool in the industry. According to market statistics from the Electronic Design Automation Companies Association (EDAC), shipments of tools using Verilog HDL produced $73.4 million in revenue in 1995, up from $66.8 million in 1994. Meanwhile, VHDL revenues in 1995 were $52.5 million, down from 1994's $59.2 million. The decline in VHDL revenue has been attributed to steep price cuts. In terms of units, the EDAC statistics show that VHDL tools barely outshipped Verilog tools 4,235 to 4,188 in 1995.

Many view Verilog HDL as best at supporting logic simulation from the gate level to the RTL level and VHDL as more efficient operating at more abstract levels (Figure 6-42). More than likely, Verilog and VHDL will coexist for quite some time.

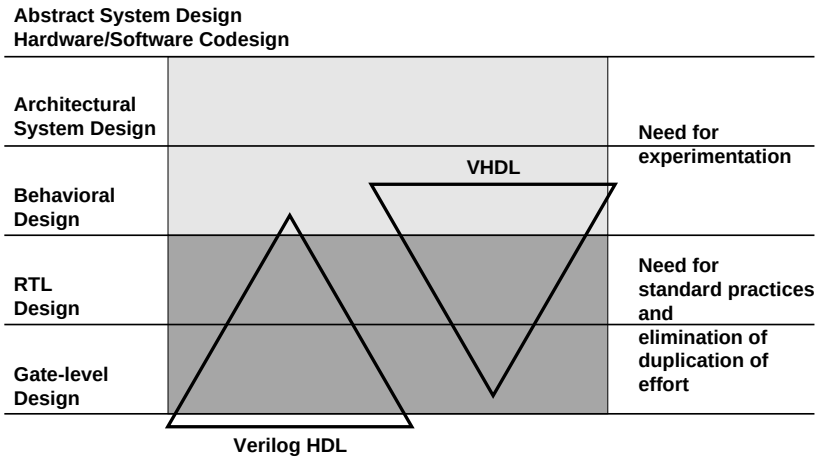


Figure 6-42. VHDL, Verilog Capabilities Overlap

Synthesis technology has had a profound impact on the ASIC industry. In less than ten years, it has grown from merely a research topic to an essential part of high-level ASIC design. Synthesis is quickly becoming essential for CPLD and FPGA designs as well. Synthesis tools translate abstract designs (generally starting from HDL descriptions) into actual logic that can be implemented in silicon, as well as optimize the logic given a set of circuit design constraints such as timing, power, loading, area, and testability. Figure 6-43 provides a listing of synthesis tool vendors.

Over the past few years, synthesis tools have struggled to keep pace with deep submicron design methodology shifts, especially in the case of timing. As discussed earlier, interconnect delay has become as much, or more, of a concern as gate delay in the design of advanced ICs. And, since actual interconnect delay is dependent upon the layout of the IC itself, physical layout information is needed very early in the design cycle in order to accurately estimate timing conditions. As a result, the traditional ASIC design flow has evolved into a more complex, "top-down" flow (Figure 6-44).

Company and Location	Product Name	Language	Functionality
Cadence Design Automation San Jose, CA	**Synergy Synthesis**	**Verilog, VHDL**	**Complete family of top-down design tools for the synthesis and optimization of RTL-level and gate-level designs for Verilog and VHDL**
Compass Design Automation San Jose, CA	**ASIC Synthesizer**	**Verilog, VHDL, EDIF**	**HDL based synthesis logic optimization. Timing/ area driven synthesis/logic optimization. State machines synthesis/optimization. Interfaces to physical tools**
Mentor Graphics Wilsonville, OR	**Mistral 1**	**DFL (in); VHDL & Verilog (output)**	**Behavioral synthesis tools for digital filters and low-throughput linear systems. Synthesizes a compete bit-serial architecture directly from a behavioral algorithmic description**
	Mistral 2	**DFL (in); VHDL & Verilog (output)**	**Behavioral synthesis tools for DSP design. Synthesizes a complete RTL design (datapath, memory, microcode) directly from a behavioral algorithmic description**
MINC Colorado Springs, CO	**PLDesigner-XL (and PLDesigner-XL for Windows)**	**VHDL, Design Synthesis Language**	**Universal tool offering a variety of device-independent input methods, optimization, automatic device selection, and automatic multiple-device partitioning**
Silerity Pasadena, CA	**PathBlazer**	**—**	**PathBlazer is a synthesis tool for complex, high-speed datapath design and optimization. It contains placement algorithms that ensure optimal timing of submicron ASICs and automatically explores architectural trade-offs and optimizes submicron placement**
Synopsys Mountain View, Calif.	**Design Compiler Family- DC Expert; DC Professional; FPGA Compiler**	**VHDL**	**Creates optimized, gate-level design based on IC design specifications and constraints to improve area and performance while reducing design time**
	Behavioral Compiler	**VHDL**	**Synthesizes datapath, memory, and control logic from a behavioral specification for a broad range of algorithmic applications**
Synplicity Mountain View, CA	**Synplify**	**Verilog, VHDL**	**Synplify is an extremely fast, easy-to-use FPGA and CPLD synthesis tool, that compiles, optimizes and technology maps Verilog and VHDL designs into small, high-performance device netlists**
	Synplify-Lite	**Verilog, VHDL**	**Same as above for one architecture of your choice**
Viewlogic Marlboro, MA	**PathBlazer**	**Verilog**	**Synthesizes and optimizes complex datapaths in minutes. Explores and displays all architectural trade-offs. Generates datapath floorplan for timing accuracy. 100x faster than other tools**
	ViewSynthesis	**VHDL**	**Logic synthesis and optimization for ASIC and FPGAs. Includes FPGA specific optimization including XBlock and LPM infrencing**

Source: Integrated System Design/ICE, "ASIC 1997" 21279

Figure 6-43. Architecture Synthesis Tools

The required tighter link between logic and physical chip design has put the pressure on design tool vendors to create more sophisticated tools that use “floorplanning” (or “design planning”) techniques to constrain variability in delay estimation and to manage the rapidly growing amount of functionality in silicon. The modern design flow involves an iteration between synthesis and floorplanning, with final routing performed only when the floorplanning netlist meets all requirements.

As previously discussed, the use of library elements (e.g., microprocessor cores) in ASIC design is on the rise. However, until recently, core libraries have tended to lock designers into a single foundry. There is now a trend to offer libraries that are crafted to support multiple foundries (i.e.,

portable). An early effort to accelerate and standardize the use of portable ASIC libraries was the introduction of the VHDL Initiative Towards ASIC Libraries (VITAL) by Cadence in 1992. VITAL was created to develop a VHDL-based "sign-off-quality" ASIC library standard. The result would be that ASIC vendors would not need to rerun simulations on each customer's design that involves a particular library. VITAL became an IEEE standard (1076.4) in September 1995. Shown in Figure 6-45 is a list of several ASIC and FPGA vendors with VITAL libraries*.

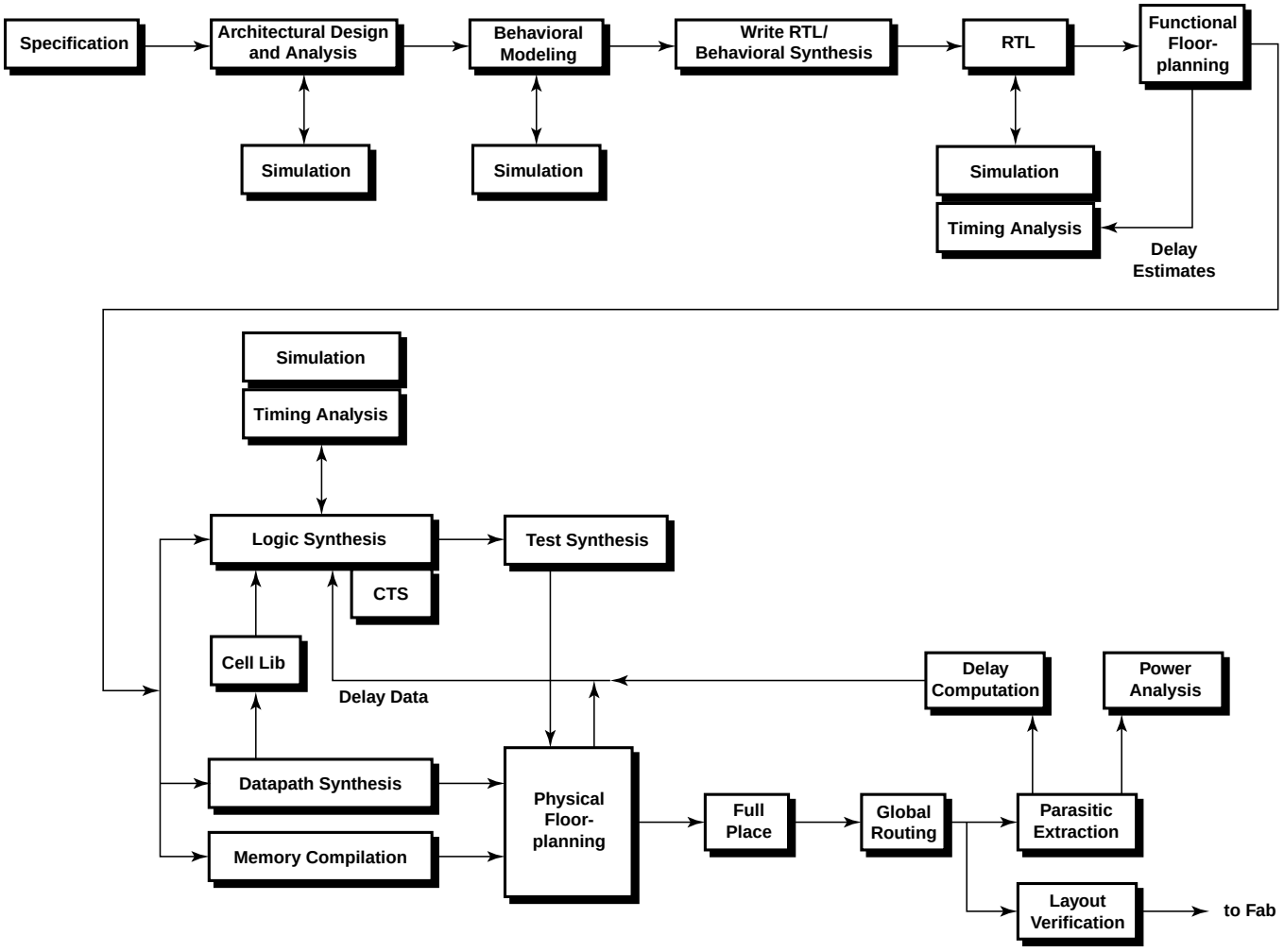


Figure 6-44. High-Level ASIC Design Flow

* As of the end of 1995, VITAL participants included more than 55 companies in the U.S., Europe, and Japan.

Company	Devices Supported
Actel	FPGAs
Altera	PLDs
AMI	Gate Arrays and Standard Cells
Honeywell SSEC	Gate Arrays
IBM Microelectronics	Gate Arrays and Standard Cells
LSI Logic	Standard Cells
Lucent Technologies	Standard Cells
Oki	Gate Arrays and Standard Cells
Orbit Semiconductor	Gate Arrays
Sharp	Standard Cells
Symbios Logic	Gate Arrays and Standard Cells
TI	Gate Arrays
Toshiba	Gate Arrays and Standard Cells
UTMC	Gate Arrays
VLSI Technology	Gate Arrays and Standard Cells
Xilinx	FPGAs and PLDs

Source: Computer Design/ICE, "ASIC 1997" 21281

Figure 6-45. Listing of ASIC Vendors with VITAL Libraries

The tools for analog and mixed-signal ASIC design are recognized to be several generations behind those for digital. So far, a way to synthesize analog circuits has not been developed. The precise control of voltage and current levels just doesn't easily lend itself to a structured design methodology. However, the industry's move toward mixed-signal "systems on a chip" is driving progress in efforts to develop standard analog HDLs (sometimes called AHDLs). Listed in Figure 6-46 are several vendors of analog / mixed-signal design tools.

The IEEE P1076.1 group has been working for several years on extending VHDL for both analog and mixed-signal modeling capability—referred to as VHDL-AMS. A language reference manual (LRM) for the VHDL-AMS tool is being prepared for IEEE balloting in December 1996. Meanwhile, the Open Verilog International (OVI) organization started working in 1995 on developing an analog-only Verilog tool (Verilog-A) based on Cadence's Spectre-HDL product. The Verilog-A effort was granted IEEE Study Group status in March 1996. A separate effort to address mixed-signal needs (Verilog-MS) has been proposed.

Some companies believe that working toward establishing an analog VHDL standard (VHDL-A) is not necessary since SPICE models and Analogy's proprietary MAST language* are already effective as analog HDLs. Figure 6-47 shows some of the differences between 1076.1 (VHDL-A) and Analogy's MAST HDL.

* Part of the Saber simulator package from Analogy.

Company and Location	Product Name; Simulation Fuctionality	Analysis Type	Output Format Supported
ANACAD Electrical Engineering Software Milpitas, CA	**Eldo; mixed analog/digital simulation**	**AC, DC, Monte Carlo, parametric, optimization, transient, noise, Fourier, transient noise, worst-case, safe-operating area, sensitivity, switched capacitor, pole/zero, accelerated transient DSP, transfer function**	**Graphical, SPICE, proprietary binary format**
	MixVHDL; mixed analog/digital simulation	**All ELDO functionality integrated with full 1076-93 VHDL and/or Verilog co-simulation capacity**	**Graphical, SPICE, proprietary binary format**
Analogy Beaverton, OR	**Saber Simulator; mixed analog/digital simulation**	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier, stress, sensitivity, model synthesis**	**Graphical, ASCII**
	QVS (Saber, QuickSim II – Mixed-Signal); mixed analog/digital simulation	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier, stress, sensitivity, model synthesis**	**Graphical, ASCII**
	Saber/Verilog; mixed analog/digital simulation	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier, stress, sensitivity, model synthesis**	**Graphical, ASCII**
	Saber/ViewSim; mixed analog/digital simulation	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier, stress, sensitivity, model synthesis**	**Graphical, ASCII**
Ansoft Pittsburgh, PA	**Maxwell SI Extractor, Maxwell SI Spicelink, Maxwell SI Eminence; analog simulation only**	**AC, DC, parametric, optimization, transient, Fourier, electromagnetic**	**EDIF, SPICE, IDL, MAST**
Cadence Design Systems San Jose, CA	**Analog Workbench/ Mixed-Signal; mixed analog/digital simulation**	**AC, DC, Monte Carlo, parametric, noise, transient, optimization, Fourier, sensitivity stress, worst-case, thermal**	**EDIF, SPICE, VHDL-A, VHDL, Verilog, Verilog-A**
	Spectre HDL; mixed analog/digital simulation	**AC, DC, transient, noise, Fourier, sensitivity,**	**SPICE, VHDL-A, Verilog-A, PSF**
	Analog Artist; mixed analog/digital simulation	**AC, DC, transient, noise, Fourier, sensitivity, optimization, Monte Carlo**	**SPICE, VHDL-A, Verilog-A PSF**
	Spectre RF	**Nonlinear RF, digital RF simulator; RF noise, RF AC, RF steady state**	**SPICE, VHDL-A, Verilog-A PSF**
Compass Design Automation San Jose, CA	**Mixed-Signal Design Option for Navigator; mixed analog/digital simulation**	**AC, DC, Monte Carlo, parametric, noise, transient, optimization, Fourier**	**Standard SPICE tabular, ELDO binary, Compass trace file**
CONTEC Microelectronics USA San Jose, CA	**ContecSPICE; mixed analog/digital simulation using logic devices built within ContecSPICE**	**AC, DC, transient, noise, Fourier, pole-zero, sensitivity**	**SPICE, ASCII, table, raw, graphs**
HP EEsof Westlake Village, CA	**Series IV, Microwave Design System**	**AC, DC, Monte Carlo, noise, transient, optimization, Fourier, high-frequency circuit, electromagnetic & systems simulation**	**Various**
IMP San Jose, CA	**Analog Magic**	**Hardware emulation of analog functions**	**Netlister to support SPICE, SABER, etc. (in dvlpmnt.)**
Intergraph Huntsville, AL	**Apex Analog Simulator; mixed analog/digital simulation**	**AC, DC, Monte Carlo, worst-case, parametric, transient, noise, Fourier, stability analysis, two-port analysis, stress analysis; spectrum analysis, mathematical analysis**	**SPICE, binary, EDIF, Verilog, graphical, VHDL, PADS, PCAD, CADSTAR, OrCAD, SCICARDS, PROTEL, Tango, Racal RINF, Mentor Boardstation V8**
Intusoft San Pedro, CA	**ICAP/4Windows Native Analog/Event-Driven; Simulation; mixed analog/ digital simulation C-Based AHDL**	**AC, DC, Monte Carlo, parametric, optimization, noise, transient, Fourier, distortion, pole-zero, temperature, sensitivity (AC & DC) Sampled-Data Systems, Array Processing, Hardware-Spice Interface**	**SPICE 2, SPICE 3, OLE2, Interactive waveform/ circuit data, hardware**
Lucent Technologies Design Automation Murray Hill, NJ	**ATTSIM; mixed analog/digital simulation**	**Transient, Fourier**	**Graphical Waveforms**
	ADVICE; analog simulation only	**AC, DC, Monte Carlo, parametric, optimization, transient, noise, Fourier**	**Graphical Waveforms**
Mentor Graphics Wilsonville, OR	**MS Analyzer: Mixed analog/ digital simulation switched digital**	**Transient, AC, DC, noise, parametric**	**SPICE, SCAP, Mentor SVDX, Lsim**
	Continuum QuickHDL: Mixed analog/digital simulation	**Transient, VHDL debugging**	**Mentor WDB, ATE EDIF netlist, all QuickHDL outputs**

Source: Integrated System Design/ICE, "ASIC 1997" 21283

Figure 6-46. Analog/Mixed-Signal Simulation Tools

Company and Location	Product Name; Simulation Fuctionality	Analysis Type	Output Format Supported
Meta-Software Campbell, CA	**HSPICE, GSI; analog only and mixed analog/digital simulation**	**AC, DC, Monte Carlo, parametric, optimization, transient, noise, Fourier**	**SPICE data, text waveforms**
MicroSim Irvine, CA	**MicroSim PSpice analog simulation only**	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier, worst-case, sensitivity, performance analysis**	**SPICE, EDIF, Probe graphical waveform analyzer**
	MicroSim PSpice A/D; mixed analog/digital simulation	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier, worst-case sensitivity, digital worst-case timing, performance analysis**	**SPICE, EDIF, Probe graphical waveform analyzer**
	MicroSim PSpice Basics analog simulation only for small circuits	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier, worst-case sensitivity, performance analysis**	**SPICE, EDIF, Probe graphical waveform analyzer**
	MicroSim PSpice Optimizer; analog simulation only	**Optimization for analog circuits**	**Probe graphical waveform analyzer**
	MicroSim Polaris, mixed analog/digital simulation signal integrity analysis	**Signal integrity analysis**	**Probe graphical waveform analyzer**
Quad Design Technology Camarillo, CA	**XTK (Crosstalk Tool Kit); and Crosstalk**	**Transmission Line**	**Quad propriety, Post Script**
Quantic Laboratories Winnipeg, Manitoba, Canada	**PCB Greenfield; mixed analog/digital simulation**	**Transient**	**SPICE**
	Compliance; mixed analog/digital simulation	**Transient**	**SPICE**
	BoardScan; mixed analog/digital simulation	**Transient**	**SPICE**
SANCAD San Diego, CA	**Mobius; mixed analog/digital simulation**	**DC, parametric, optimization, transient, Fourier, perturbation, timing, margin**	**SPICE + interactive X-Windows marching wave-form display w/selectable waveform compression**
	Cell Designer; mixed analog/digital simulation	**DC, parametic, optimization, transient, Fourier, timing, margin**	**SPICE + interactive X-Windows marching wave-form display w/selectable waveform compression**
Tanner Research Pasadena, CA	**T-Spice; mixed analog/digital simulation**	**AC, DC, transient, transfer**	**ASCII, W-edit waveform**
Tatum Labs Ann Arbor, MI	**ECA-2; analog simulation only**	**AC, DC, Monte Carlo, transient, Fourier, worst-case, temperature sweep, component sweep, AC & DC sensitivity**	**Tabular or on-line graphics**
	SpiceAge for Windows; mixed analog/digital simulation	**AC, DC, Monte Carlo, transient, Fourier, worst-case, temperature sweep, component sweep, noise**	**Tabular or on-line graphics**
	ALLTED; mixed analog/digital simulation, and mixed technologies (electronic, hydraulic, pneumatic, etc.)	**AC, DC, Monte Carlo, optimization, transient, Fourier, AC & DC sensitivity, optimal tolerance assignment, statistical, multivariant**	**Tabular or on-line graphics; real time or manipulated by post-processor**
TESOFT Roswell, GA	**TESLA Block Diagram Simulator; mixed analog/ digital simulation and RF**	**Monte Carlo, transient, noise, Fourier, distortion**	**Graphical waveforms, spectra & logic, binary and ASCII data formats**
Viewlogic Systems Marlboro, MA	**Saber – ViewSim VHDL, Chronologic Simulation's; VCS Verilog; mixed analog/ digital simulation**	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier**	**Saber, waveforms, EDIF, PWL, binary, ASCII**
	Mixed Signal Designer with ViewSpice; mixed analog/ digital simulation	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier, worst-case, distortion,**	**Streaming waveforms, SPICE, EDIF, PWL, binary, ASCII**
	Mixed Signal Designer with HSPICE; mixed analog/ digital simulation	**AC, DC, Monte Carlo, parametric, transient, noise, Fourier, distortion, optimization, pole-zero, sensitivity, small-signal transfer, sampling noise, small-signal network**	**Streaming waveforms, SPICE, EDIF, PWL, binary, ASCII**

Source: Integrated System Design/ICE, "ASIC 1997" 21284

Figure 6-46. Analog/Mixed-Signal Simulation Tools (continued)

	1076.1	MAST
Transient Analysis	Yes	Yes
Dc Operating Point Analysis	Yes	Yes
Dc Transfer Analysis	Yes	Yes
Ac Analysis	Yes*	Yes
Noise Analysis	No	Yes
Stress Analysis	No	Yes
Small-Signal Parameter Analysis	No	Yes
Sensitivity Analysis	Yes	Yes
Distortion Analysis	Yes	Yes
Monte Carlo	Limited**	Yes
Mixed Analog/Digital Model	Yes	Yes
Non-Electrical Modeling	Yes	Yes
Interaction With Simulator	Limited	Yes
Transfer Function Modeling	Limited	Yes
IEEE Standardization	Pending	No
Models Portable Between Vendors	Yes	No
Availability	1996	Now

*** While 1076.1 will support enough frequency-domain modeling to allow a simulator to run an ac small-signal analysis, support beyond simple ordinary differential equations is not clearly defined at present. 1076.1 will probably not support frequency-domain modeling based on distributed partial differential equations, or large-signal frequency simulation.**

**** 1076.1 offers the ability to specify a distribution on a parameter, but not to control when and how that distribution is evaluated.**

Source: Analogy Inc., EE Times/ICE, "ASIC 1997" 20063A

Figure 6-47. Analog VHDL 1076.1 (VHDL-A) Versus Analogy's "MAST"

Several ASIC design tool highlights from 1995 and 1996 are described below.

- Numerous alliances were announced between ASIC vendors and design tool suppliers, providing proof that the increasingly complex nature of ASIC design is requiring greater cooperation at both ends of the process. Pacts announced in 1996 include those between Toshiba and Cadence; LSI Logic and High Level Design Systems; Toshiba and Synopsys; LSI Logic and Viewlogic; IBM and Synopsys; and Symbios Logic and Compass.

- A new development group called Rapid—Reusable Application-Specific Intellectual Property Developers—was announced in June 1996. Members of Rapid (3Soft, Advance1 Logic, Integrated Silicon Systems, iReady, Object Oriented Hardware, Virtual Chips, the Design Reuse Group of Synopsys, and Mentor's ICTC group) joined together to bolster the visibility of companies who offer chips and circuit designs in the form of intellectual property.

- In an unprecedented agreement for the EDA industry, the two largest vendors Mentor Graphics and Cadence signed a pact providing reciprocal access to each other's tools. The move will facilitate tool interoperability and allow both firms to move ahead with their design consulting and "outsourcing" services.

- The Semiconductor Industry Association (SIA) is weighing a proposed "focus center" model for university / industry research in deep submicron design-automation issues. The proposed design center, which would receive an estimated funding of $5 million to $7 million, will be an attempt to address the widening gap between process technologies and design tools.

- In March 1996, Compass announced its Passport™ Foundry Program, a cooperative program aimed at verifying foundry process and characterizing physical libraries to ensure first-time silicon success. Charter members of the program include Chartered Semiconductor, ES2 (now owned by Atmel), LG Semicon, TSMC, and Tower Semiconductor.

- In early 1996, LSI Logic became one of the last ASIC vendors to embrace commercial EDA tools. With its new ToolKit environment, LSI Logic said it would replace its existing proprietary design kits with third-party tools. However, the company will continue to use its own layout tools.

- Lucent Technologies announced in February 1996, the creation of new software development forum for high-level PLD / FPGA design. The ORCA Alliance for Synthesis is designed to improve the integration between synthesis, simulation, timing analysis, and place-and-route tools from various suppliers.

ASIC TESTING

As the number of gates per pin has risen along with gate count (Figure 6-48), fully testing, debugging, and diagnosing an ASIC has become more difficult, yet increasingly important so as to ensure quality and reliability. The requirement for fully testing ASIC devices has become a top priority for many ASIC manufacturers and users.

USABLE GATES	750	2,000	5,000	10,000	30,000	150,000	1,300,000
PINS	50	90	150	220	300	528	936
GATES/PIN RATIO	15	22	33	45	100	284	1,389

Source:ICE, "ASIC 1997" 15578B

Figure 6-48. Gates Per Pin Trend

Similar to the movement toward the "top-down" design approach for ASICs, the ASIC industry is moving quickly toward incorporating DFT (design-for-test) methods early on in the design flow. At the 20,000-gate and greater densities, most ASIC vendors highly recommend that the users incorporate design-for-testability techniques into their design flow. Some high-density ASIC libraries are even making some DFT circuitry mandatory.

Design-for-test methods range from those that are simple, use no overhead (i.e., silicon area), and provide low effectivity to those that are complex and costly but provide thorough testability. Figure 6-49 shows a sampling of some of the DFT software tools available to the ASIC industry.

A factor driving greater use of DFT methods that move external testing functions on-chip (e.g., built-in self-scan [BIST] or boundary scan) is the soaring costs of the test equipment itself (Figure 6-50). In the early 1990's, the cost of systems needed to test ICs with 256 pins and clock rates of 40MHz was approximately $2 million. The SIA has expressed concern that if test technology continues to follow its current trends as chip speeds push 500MHz and pin counts climb to 4,000, the price of test systems could approach $50 million by the year 2010.

As is generally accepted, on-chip test structures typically cause a 5-20 percent overhead penalty. However, as shown in Figure 6-51, even a 20 percent silicon area penalty paid for a 30K usable-gate array with on-chip test capability is only about $2.60 per chip. The $2.60 penalty may be justified when compared to the possible $10 or more savings that can be realized at the system level (because of fewer very expensive field failures) if fault coverage* is significantly improved. Moreover, as ASIC densities continue to soar, die area penalty will eventually become insignificant compared to the benefits. This will become especially apparent for ASICs that have hundreds of thousands of gates!

The DFT method enjoying the most press coverage lately has been BIST. Though it is not a new, untried technology, BIST has only recently been commercialized for general use during the front-end, HDL-based design process. BIST supporters say the technique offers benefits such as the ability to run at intended chip operating speeds, the potential to significantly cut costs in test equipment hardware and software development, and the ability to carry test programs through to systems and field testing. In addition, the integration of a larger number of cores in ASICs in the future will require that BIST structures be designed into each core to prevent the need to add significant unwanted routing and logic overhead to the chip.

* Fault coverage is measured as a percentage of the possible defects a test program can detect. The defect rate is the percentage of devices passing a test. Thus, the higher the fault coverage, the lower the defect rate. A high level of fault coverage is very important for advanced ASIC devices.

Company Location	Name of Tool	Tool Function	Fault Simulator Included
Acugen Software Nashua, NH	**SHARPEYE**	**SHARPEYE software automatically analyzes digital logic designs and reports testability problems in an easy-to-read format.**	**No**
Alpine Image Systems Mountain View, CA	**AVLsim**	**Verifies 1149.1 testability during logic simulation. Uses simulator as an 1149.1 ATPG.**	**No**
	BSDL Verifier	**Verifies the accuracy of the BSDL file for an IC by comparing to hardware operation.**	**No**
Altium/IBM EDA Charlotte, NC	**Test Bench**	**DFT checking tools and ATPG.**	**Yes**
Attest Software Santa Clara, CA	**Tdx step**	**Testability analysis. Identifies controllability and observability problems by analyzing ATPG and fault simulation progress and difficulties.**	**Yes**
Cadence Design Systems Chelmsford, MA	**Test-intelligent design series**	**Integrated set of test synthesis, ATPG, and fault simulation tools. Test synthesizer opens a single-step approach to test synthesis, scan insertion. Test Generator is a high-performance ATPG tool, and Verifault is a concurrent fault simulator.**	**Yes**
Chronologic Simulation Los Altos, CA	**Verilog Compiled Simulator (VCS)**	**High-performance Verilog simulator.**	**No**
Compass Design Automation San Jose, CA	**Test Synthesis Solution**	**Synthesis and ATPG support of boundary scan, internal scan, built-in self-test, and core isolation. Integration of all architectures with standard or custom TAP controller.**	**No**
CrossCheck Technology San Jose, CA	**Aide II**	**Test pattern generation and fault simulation for stuck-at, IDDQ, and delay fault test including scan insertion, test rule checks, and vector post-processing.**	**Yes**
Flynn Systems Nashua, NH	**FS-ATG Version 3.0**	**Automatic test vector generation for PLDs, FPGAs, and EPLDs.**	**Yes**
Intellitech Meredith, NH	**BSDLMaker!**	**BSDLMaker! creates BSDL (boundary scan description language) files from silicon.**	**No**
Intergraph Electronics Huntsville, AL	**Concurrent Fault Simulator (CFS)**	**Mixed-level concurrent fault simulator with support for VHDL, LMG software and hardware models, and C models.**	**Yes**

Source: Integrated System Design/ICE, "ASIC 1997" 20275A /20276A

Figure 6-49. Design-For-Test Tools

Company Location	Name of Tool	Tool Function	Fault Simulator Included
LogicVision San Jose, CA	**ASICTEST**	**An integrated family of ESTA products with JTAGSYN for 1149.1 RTL synthesis; ICRAMBIST for RTL synthesis of BIST for embedded memories; and ISCANTEST for scan insertion, ATPG, and fault simulation.**	**Yes**
	JTAGSYN	**Performs high-level synthesis of RTL code (Verilog or VHDL) for a complete 1149.1-compliant top-level module containing I/O, boundary scan, and TAP. Also creates a BSDL file.**	**N/A**
	ICRAMBIST	**Performs high-level synthesis of RTL code (Verilog or VHDL) for an area-efficient memory BIST scheme. Generates controller and memory interfaces, plus stimulus for simulation.**	**N/A**
	ICSCANTEST	**Performs scan insertion, ATPG and fault simulation of Verilog netlists. Understands 1149.1 Boundary Scan and TAP. Includes PL/I interface for simulation and WGL for test data.**	**Yes**
LSI Logic Milpitas, CA	**TEST Builder**	**Full scan and optimized scan products insertion, and ATPG.**	**Yes**
	JTAG Builder	**JTAG insertion, test generation for JTAG logic, and BSDL generation**	**Yes**
	RAMBIST Builder	**Receives RAM description from memory. Compiles and automatically synthesizes built-in self-test circuit for RAM; single or multiple port, synchronous or asynchronous.**	**Yes**
Lucent Technologies Design Automation Allentown, PA	**ATTDTF/GENTEST**	**Sequential ATPG, fault simulator; partial and full scan, IDDQ, diagnostic (DFT).**	**Yes**
	ATTDFT/BCAD	**BSDL-Editor and conformance test generation for boundary scan implementation.**	**N/A**
	ATTDFT/BIST2	**Built-in self-test for random logic.**	**Yes**
Mentor Graphics Wilsonville, OR	**BSDArchitect**	**Behavioral test synthesis of boundary scan for ASIC and IC design. Auto generation of HDL test bench. Auto generation of BSDL model.**	**No**
	DFTAdvisor	**Structural test synthesis of internal scan for ASIC and IC design. Optimal scan selection for partial scan. Testability analysis. Rule checking.**	**No**

Source: Integrated System Design/ICE, "ASIC 1997" 20276A/20277A

Figure 6-49. Design-For-Test Tools (continued)

Company Location	Name of Tool	Tool Function	Fault Simulator Included
Mentor Graphics (continued) Wilsonville, OR	**FastScan**	**ATPG and fault simulation for full and partial scan designs, including IDDQ. BIST testability analysis and fault simulation.**	**Yes**
	FlexTest	**ATPG for full, partial, and no scan designs, including IDDQ.**	**Yes**
	QuickFault II	**Advanced fault simulation and graphical testability feedback for ASICs, boards, and MCMs.**	**Yes**
	QuickGrade II	**Probabilistic fault analysis and graphical testability feedback for ASICs, boards, and MCMs.**	**Yes**
	VTM:TOP	**Testpoint analysis for boards and MCMs with full or partial boundary scan. Automatically updates design with testpoint selection results.**	**No**
	Physical Test Manager (PTM): SITE	**DFT analysis of PCBs and MCMs. Merges physical access and test figure requirements with circuit design rules and clearances to automatically optimize testpoint locations.**	**No**
Simutest Sunnyvale, CA	**TASE**	**Generates test vectors for simulators; automatically creates test programs for testers from simulator/ATPG data.**	**No**
Summit Design Beaverton, OR	**TDS**	**Design to test links.**	**No**
Sunrise Test Systems Santa Clara, CA	**TestGen**	**DRCs, test logic synthesis, ATPG for sequential and combinational circuits.**	**Yes**
Synopsys Mountain View, CA	**Test Compiler**	**Combines synthesis, scan-based test, timing analysis and ATPG to automate design for test.**	**No**
	Test Compiler Plus	**Applies test synthesis techniques to automate the implementation of partial scan according to design constraints, and provides predictable ATPG results.**	**No**
	TestSim	**Fault simulator integrated with Synopsys test synthesis and test management and with Test Complier libraries. Incorporates functional vectors or other externally generated vectors by fault simulating them and using the results to seen ATPG in Test Complier or Test Complier Plus.**	**Yes**
Syntest Technologies Sunnyvale, CA	**Pioneer** **Picasso** **Pyramid**	**Testability analyzer.** **Sequential/partial-scan, full-scan ATPG.** **Scan synthesizer.**	**Yes**

Source: Integrated System Design/ICE, "ASIC 1997" 20277A/20278A

Figure 6-49. Design-For-Test Tools (continued)

Company Location	Name of Tool	Tool Function	Fault Simulator Included
Teradyne Boston, MA	**Test Architect**	**Tool set integrated into Mentor Graphics QuickSim design simulator; provides direct link to Teradyne board testers.**	**No**
Texas Instruments Dallas, TX	**ASSET Diagnostic System**	**Supports interactive debug and test of IEEE 1149.1-compatible designs. Interactively controls and observes scannable signals at the bit, register, pin or bus level.**	**No**
VEDA Design Automation Santa Clara, CA	**Hifault**	**Fault simulation with deterministic and statistical fault simulation, fault diagnosis, IDDQ test support and toggle counter with built-in observability.**	**—**
Viewlogic Systems Marlboro, MA	**ViewTest**	**Generates manufacturing test programs for new and existing designs. Tools available within ViewTest include: testability analysis and design rule checking, sequential automatic test pattern generator (ATPG), fault simulation, test synthesis, current testing, 1149.1 JTAG Boundary Scan, BSDL support, path delay testing, and vector compaction.**	**—**

Source: Integrated System Design/ICE, "ASIC 1997" 20278A

Figure 6-49. Design-For-Test Tools (continued)

	Hewlett-Packard	LTX	Advantest	Schlumberger	Megatest
Specification	**8000 F330T**	**Delta 100**	**T6681**	**IT S9000GX**	**Vega 400**
Architecture	**Processor/Pin**	**Segmented Resource**	**Resource/Pin**	**Sequence/Pin**	**Resource/Pin**
Base Rate Data (MHz)	**160**	**100**	**200**	**200**	**200**
Maximum Data Rate (MHz)	**330**	**200**	**400**	**400**	**300**
Maximum Clock Rate (MHz)	**330**	**250**	**400**	**800**	**500**
Maximum I/O Pins	**512**	**512**	**1,024**	**512**	**512**
Maximum Number Test Heads	**1**	**2**	**2**	**2**	**2**
Overall Accuracy (ps)	**±300**	**±150**	**±300**	**±240**	**±300**
Cost/Pin (typical, $)	**6,000**	**6,000 to 7,000**	**8,000 to 9,000**	**12,000 to 14,000**	**8,000 to 12,000**

Source: Solid State Technology/ICE, "ASIC 1997" 21282

Figure 6-50. High Performance IC Test Equipment

Other on-chip test architectures include internal scan and boundary scan. For the internal scan method, circuitry is designed into the chip for scan test data and control lines, which are then chained together to allow serial access for shifting in test patterns and shifting out test results. Internal scan may either be implemented as full scan or partial scan. Partial scan has the benefit of reducing area and performance impact, but reduces fault coverage.

Cost Factors	Without Silicon Test Area Penalty	With 20% Silicon Test Area Penalty
Wafer size	150mm	150mm
Tested wafer cost	$700	$700
Die size (sq. mils)	124K	149K
Total dice available	180	148
Probe yield (0.35d/cm^2)	82%	78%
Number of good dice	148	115
Cost per good die	$4.74	$6.06
Packaging cost (plastic)	$2.47	$2.47
Assembly yield	97%	97%
Yielded assembly cost	$7.44	$8.80
Final test cost	$0.75	$0.75
Final test yield	90%	90%
Factory cost	$9.10	$10.61
Gross margin	41%	41%
Selling price (5,000)	$15.42	$17.99

Source: ICE, "ASIC 1997" 17737C

Figure 6-51. 30K Usable Gate Array Cost Comparison (With and Without On-Chip Test)

Boundary scan has become a popular test method due to the increased usage of high-density surface mount ASICs. It provides a way to directly access the inputs and outputs of a chip where physical contact with the device pins is impossible. The die area penalty paid by implementing the IEEE 1149.1 boundary scan architecture depends on the density of ASIC being designed. The TAP (test access port) controller and registers require about 500 gates of circuitry while the gates needed for the I/O cells are dependent upon the number of I/Os. For example, a 3,000-gate device with 44 pins would suffer a hefty 60 percent die area increase, whereas a 10,000-gate, 100-pin ASIC would incur only a 12 to 15 percent die area penalty. Moreover, a pad limited die could incur no extra die area, and thus a negligible increase in cost.

Another test method that has gained popularity over the past couple of years is called IDDQ (i.e., quiescent supply current) testing. CrossCheck describes the rational behind IDDQ testing as follows.

"Under normal conditions, IDDQ is typically within pre-determined limits in defect-free CMOS VLSI circuits. A defect that causes current drain in excess of those limits is considered a leakage or IDDQ fault. By monitoring the power supply of a circuit directly, IDDQ detects manufacturing defects such as transistor-level shorts and metal bridging. Many defect types are only detectable by IDDQ tests and, as such, users of IDDQ testing have reported lower levels of defective parts shipped to customers when IDDQ testing is used a supplement to their existing test techniques, including functional or scan tests."

As even CrossCheck recommends when discussing IDDQ testing, it is most beneficial when used as a supplement to other test procedures. It has been suggested that a combination of test strategies are necessary for obtaining the best results. For example, using full scan on random logic portions of the IC, partial scan elsewhere, boundary scan on I/O lines, BIST (built-in self-test) on regular structures (e.g., memory), as well as IDDQ and delay fault tests, may be appropriate.

As one can see, those looking for an easy "cure-all" ASIC test solution will quickly be disappointed. Not only do different system applications require individualized test program strategies (Figure 6-52), but each IC may also need to implement numerous external and on-chip test methodologies in order to attain a high-level (99-100 percent) of fault coverage (Figure 6-53).

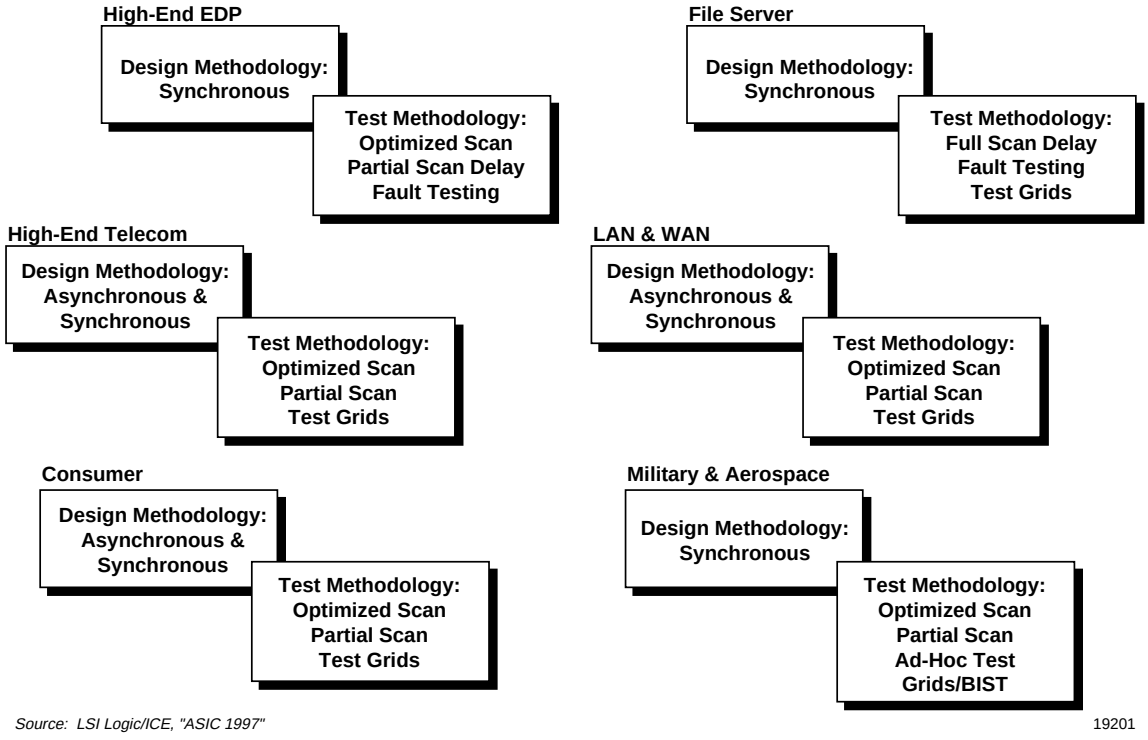


Figure 6-52. Providing Test Strategies for Different Target Markets

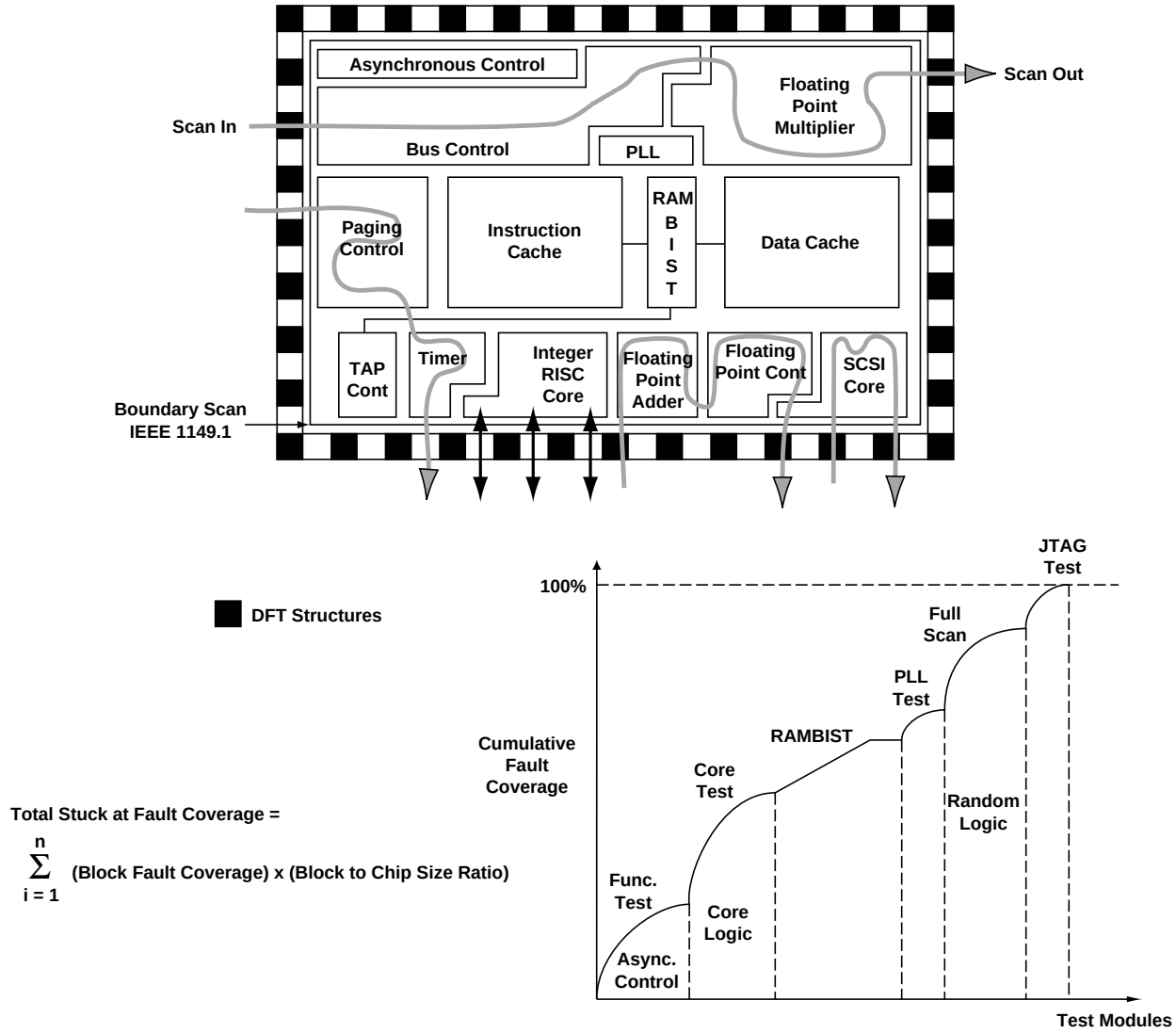


Figure 6-53. Integration of Multi-Style Design-for-Test Methodologies