INTRODUCTION

When making decisions, there are numerous pros and cons that must be weighed in order to make an intelligent choice. This is especially true when an IC user considers the advantages and disadvantages of ASIC devices (Figure 5-1).

<table>
<thead>
<tr>
<th>STANDARD ICs</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pros</td>
<td>Cons</td>
</tr>
<tr>
<td>Low cost</td>
<td>Not optimized for each system</td>
</tr>
<tr>
<td>Off-the-shelf availability</td>
<td>Difficult to obtain system product differentiation</td>
</tr>
<tr>
<td>Proven reliability (fully tested)</td>
<td>Inefficient use of board space</td>
</tr>
<tr>
<td>Multiple sources (usually)</td>
<td></td>
</tr>
</tbody>
</table>

| ASICs | | |
| Pros | Cons |
| Efficiency of the ASIC for optimizing system performance | High unit cost of ASIC |
| Efficient use of board space | User pays for ASIC design |
| Performance (speed) enhanced (usually by replacing numerous standard ICs with a single ASIC) | Potential for design failure and reliability problems |
| | Most vendors single-source ASICs |
| | System house needs internal ASIC design and test expertise |
| | Long leadtimes (not including PLDs/FPGAs) |

Source: ICE

Figure 5-1. Pros and Cons of Standard ICs and ASICs

In comparison to ASICs, the advantages of standard devices can be summed up in one phrase — ease-of-use. For standard ICs the cost structures are easily identified and the IC manufacturer can supply the standard IC user with fairly specific availability and reliability information. Moreover, in most cases, if the standard IC user does not like the way a vendor is treating him, it takes little effort to patronize other companies that make identical parts and who will better serve the user’s needs.

The major problem with standard ICs that helped begin the move to using ASIC devices was that standard parts were not optimized for each individual system’s specifications. The most important “pro” for ASIC devices has always been the “efficiency of the ASIC for optimizing system performance.”
The major negatives of using ASICs have almost always dealt with cost. The obvious costs are the typically higher ASIC unit costs and NREs (non-recurring engineering) costs. One example is the added effort to design and partition the system for an ASIC application. But there are other “costs” involved with using ASICs that are not so readily apparent to the potential ASIC user.

By definition, the decision to use ASICs instead of standard ICs will carry increased risks. These risks can lead to high costs incurred by the ASIC user. For example, if the ASIC design fails to work properly in the system, a new design (and possibly another NRE charge) will have to be created. Besides a cash outlay, the ASIC user will need to devote expensive in-house engineering and management resources to fix the problem. In addition there is a risk of “time-to-market” delays.

Testing can also create some significant costs to the ASIC user. In some cases the NRE charges do not include test program development and these costs must be added to the program later. Moreover, with advanced ASICs averaging only 95 percent to 99 percent fault coverage during testing, problem-susceptible ASICs that make it into systems may increase field service and warranty costs.

Problems occurring at the vendor’s manufacturing facility could lead to long delays for a user to receive its ASICs, and thus lead to delays in shipping the system itself. The costs to a small company of not shipping its systems on-time could be and has been catastrophic.

For the most part, IC vendors and users have worked hard to minimize the total “costs” of using ASICs. The growth of the ASIC industry is one indication that for most IC users the risks and associated costs of using ASICs are well worth the effort.

While it is true that each IC customer will have its own specific system requirements, some basic criteria can and should be explored by the ASIC user. This section will analyze the significant trade-offs and essential considerations necessary in choosing from among PLD, gate array, and standard cell approaches.

THE DESIGN CYCLE

As was previously mentioned, one of the primary distinguishing attributes of a gate array or standard cell approach is the cooperation that must exist between the vendor and user. In every cell-based design there are three major steps: design (including designing for test), layout and verification, and manufacturing.

As shown in Figure 5-2, the user typically handles most of the design work, while the layout and verification responsibilities are usually shared. Actual manufacturing of the device is, of course, handled entirely by the vendor.
It should be noted that the above description assumes that the user has at least a medium level of ASIC sophistication. Typically a user with little design experience will require more “hand holding” by the vendor or may choose to use a third-party design house (a list of third-party design houses is given in the Appendix). Figure 5-3 shows a typical ASIC schedule when using a third-party design house and foundry.

Both of these approaches are effective but result in a more costly ASIC device. It behooves a large system house (or heavy user of ASICs) to perform internally as much of the design work as possible.

Not only are systems companies performing more of the design work of ASICs in-house, they are also becoming much more productive. Figure 5-4 shows one example (Silicon Graphics) of the increasing productivity from using advanced CAD tools and the increasing ASIC design productivity as measured in gates designed over a period (day or month) of time. As will be discussed further in Section 6, much of this increase is due to better CAD tools. However, it should be noted that some of the productivity gain is attributed to the increasing experience of ASIC designers within the system company.

**Figure 5-3. Typical Design Cycle**

<table>
<thead>
<tr>
<th>MAJOR PHASES</th>
<th>ACTIVITY WITHIN EACH PHASE</th>
<th>DIVISION OF RESPONSIBILITIES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design</td>
<td>Pre-design start</td>
<td>Vendor/Customer</td>
</tr>
<tr>
<td></td>
<td>Design review</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Cell selection</td>
<td>Customer</td>
</tr>
<tr>
<td></td>
<td>Schematic capture</td>
<td>Customer</td>
</tr>
<tr>
<td></td>
<td>Simulation (functional)</td>
<td>Customer</td>
</tr>
<tr>
<td>Layout and verification</td>
<td>Simulation (timing)</td>
<td>Vendor/Customer</td>
</tr>
<tr>
<td></td>
<td>Pre-layout design review</td>
<td>Vendor/Customer</td>
</tr>
<tr>
<td></td>
<td>Test vector generation</td>
<td>Vendor/Customer</td>
</tr>
<tr>
<td></td>
<td>Auto-layout</td>
<td>Vendor</td>
</tr>
<tr>
<td></td>
<td>Post-layout simulation</td>
<td>Vendor/Customer</td>
</tr>
<tr>
<td>Prototype manufacturing</td>
<td>Post-layout approval</td>
<td>Vendor/Customer</td>
</tr>
<tr>
<td></td>
<td>Mask generation</td>
<td>Vendor</td>
</tr>
<tr>
<td></td>
<td>Wafer fab</td>
<td>Vendor</td>
</tr>
<tr>
<td></td>
<td>Assembly/test</td>
<td>Vendor</td>
</tr>
<tr>
<td></td>
<td>Prototype approval</td>
<td>Customer</td>
</tr>
</tbody>
</table>

Source: Intel
Figure 5-3. Typical Design House/Foundry ASIC Schedule

Figure 5-4. Increasing Design Productivity
Although great strides have been made in ASIC software design tools, the improvements in design approaches have not been able to keep pace with the increases in gate density (Figure 5-5). Figure 5-6 shows how far design productivity has lagged IC density increases since 1981. As will be discussed in Section 6, CAD tools are going to be a key issue in producing high-density sub-0.35µm ASICs.

Among the most critical areas for the ultimate success of an ASIC program are the simulation and verification steps. As was shown in Figure 5-2, most of the steps are a combined effort of the ASIC manufacturer and customer. As CAD tools become more sophisticated, some ASIC vendors are allowing the user to do all of the simulation and design-rule verification, when using the ASIC vendors’ software programs.
NRE COST TRENDS

The costs that are passed on to the user by the vendor (or third-party design house) are known as NREs or non-recurring engineering expenses. NREs usually cover everything from circuit design through prototype approval. The other major cost passed on to the user is the component charge, which is the cost of manufacturing and assembling the device, plus a profit.

Since the early 1980’s, the ASIC vendor’s revenue split between component charges and NREs has dramatically shifted. One example is the revenue data from LSI Logic (the leading U.S.-based ASIC house) which shows how rapidly the NRE portion has shrunk (Figure 5-7). The increasing capability of the system companies’ in-house design resources as well as the increasing number of ASIC designs moving into volume production are driving this evolution.

Figure 5-8 shows that since 1987 and until 1994, LSI Logic’s design and technology service revenue stayed at about $100 million per year. With standard cell NRE’s higher than those for gate arrays and LSI Logic’s quickly growing standard cell business, one would expect LSI’s NRE revenues to surge. However, the number of standard cell designs performed is usually less than that for gate arrays, leading to the declining design revenue for LSI Logic in 1995 and 1996.

Another factor in the shift in the NRE contribution is the overall shift in the market categories for ASICS. The portion of ASIC sales to high NRE content applications has dropped. The major ASIC market are shifting to high volume consumer and communication designs were the NRE content will continue decline (See Figure 5-9 from LSI data). ICE expects the NRE percentage of total ASIC sales to continue to decline for LSI Logic as well as for the other ASIC suppliers as a result of these market shifts.
Figure 5-7. LSI Logic’s Changing Revenue Make-Up (1985-1996)

Figure 5-8. LSI Logic’s Design and Technology Service Revenues (1985-1996)
Technology Factors

The major factors in setting NRE costs are the type of technology used, the number of competitors in the market, and the complexity level (number of gates or macrocells). In general, the higher the gate count the higher the NRE. This is especially true for technologies like ECL and CMOS.

Below 10,000 usable gates, CMOS gate array NREs tend to reside in the $10,000-$20,000 range. At the 20,000-100,000 gate and greater density levels, CMOS gate array NREs are approximately $0.75-$1.00 per gate. Beyond 150,000 gates, NREs come down to about 30-50¢ per gate. Embedded functions like MCUs, MPUs, and blocks of high-speed SRAM can sometimes increase the NREs by up to 50 percent. Thus, a user should expect to pay an NRE of at least $75,000-$100,000 for a CMOS array with 100,000 usable gates. For BiCMOS devices, $1.50-$3.00 per gate is a typical range for NRE charges (Figure 5-10).

<table>
<thead>
<tr>
<th>Technology</th>
<th>Usable Gates</th>
<th>NRE/Gate ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>≤10K</td>
<td>4.00 - 10.00</td>
</tr>
<tr>
<td></td>
<td>&gt;10K</td>
<td>1.00 - 2.00</td>
</tr>
<tr>
<td>BiCMOS</td>
<td>All</td>
<td>1.50 - 3.00</td>
</tr>
<tr>
<td>CMOS</td>
<td>≤3K</td>
<td>6.00</td>
</tr>
<tr>
<td></td>
<td>&gt;3K - ≤10K</td>
<td>1.55 - 3.00</td>
</tr>
<tr>
<td></td>
<td>&gt;10k - ≤20k</td>
<td>1.50</td>
</tr>
<tr>
<td></td>
<td>&gt;20K - ≤150K</td>
<td>0.75 - 1.00</td>
</tr>
<tr>
<td></td>
<td>&gt;150K</td>
<td>0.30 - 0.50</td>
</tr>
<tr>
<td>ECL</td>
<td>≤2K</td>
<td>25.00</td>
</tr>
<tr>
<td></td>
<td>&gt;2K - ≤10K</td>
<td>5.00 - 10.00</td>
</tr>
<tr>
<td></td>
<td>&gt;10K</td>
<td>1.00 - 2.00</td>
</tr>
</tbody>
</table>

Source: ICE

Figure 5-10. Typical Gate Array NRE Charges
Compared to low-end gate arrays, the NRE charges for advanced CMOS gate arrays and CMOS standard cell devices have remained fairly high due to the complexities of the technologies and the fewer number of vendors (Figure 5-11).

One thing that should be remembered about ASIC NREs is that they are almost always negotiable. If an ASIC manufacturer needs to better utilize its fab or the ASIC customer’s future business prospects look promising, the ASIC NRE charge to the customer may be lowered or even waived. However there have been cases were the low NRE was offset by a much higher unit cost. Thus the customer must consider the total price per part used.

As less and less of the ASIC producers total revenue is realized from NRE, ASIC manufacturing efficiency and costs become critical. Typically the ASIC fab will be less efficient than a high volume memory facility, because of the added infrastructure needed for the ASIC fab to handle many mask sets, part types, and process variations.

An ASIC manufacturer must now operate IC facilities that are competitive in process technology and utilize a high percentage of available capacity. Anything less than this is going to make profitability a very difficult result for the ASIC vendor to attain.

**PLD OVERVIEW**

PLDs resemble gate arrays and standard cells in that a part is made unique by (or for) each individual user and can correctly be called an Application Specific Integrated Circuit. Moreover, NRE expense is incurred by the user. This cost covers the onetime purchase of programming software and a programming station. This cost can be significant.

An example is a case study presented by Silicon Graphics, Inc. which showed the cost elements (Figure 5-12) of performing PLD programming in-house. However Silicon Graphics stated that the costs for the in-house PLD programming facility were normally recouped within the first three quarters of operation assuming a continuous requirement.
The traditional TTL-based fuse-programmable PLD, originally marketed by Signetics and MMI, has been replaced by CMOS PLDs. In general, these devices have surpassed the capabilities of the bipolar PLDs by offering lower power requirements, enhanced functionality, and higher gate densities. PLDs with up to twenty thousand usable gates are now a viable option for the low-end gate array user.

### PLDs VERSUS GATE ARRAYS

The following case history is a specific comparison of plastic-packaged PLD and gate array costs. For this example, a CMOS 0.7 micron 60-90MHz gate array with 10,000 usable gates was compared to a 0.5 micron (three-layer metal) field-programmable gate array (FPGA) with a similar gate count that supports system performance of up to 50MHz. Higher performance PLDs are available but can cost twice as much or more per gate.

Cost can be divided into two categories, fixed and variable, that when added together give the total cost (Figure 5-13). Gate arrays have significantly higher fixed costs than PLDs, which tends to make PLDs more cost effective at low volume levels.
The breakdown of fixed costs for the gate array and PLD is shown in Figure 5-14. An explanation of the various terms is given below.

<table>
<thead>
<tr>
<th>COST SEGMENT</th>
<th>GATE ARRAY ($)</th>
<th>PLD ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NRE</td>
<td>20,000</td>
<td></td>
</tr>
<tr>
<td>SIMULATION</td>
<td>5,000</td>
<td></td>
</tr>
<tr>
<td>TIME TO DESIGN FOR TESTABILITY</td>
<td>(2 man weeks) 4,000</td>
<td></td>
</tr>
<tr>
<td>DESIGN ITERATIONS*</td>
<td>11,250</td>
<td></td>
</tr>
<tr>
<td>TEST PROGRAM (4 man weeks)**</td>
<td>8,000</td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td>48,250</td>
<td></td>
</tr>
<tr>
<td>SIMULATION</td>
<td>(1 man week) 2,000</td>
<td></td>
</tr>
<tr>
<td>SOFTWARE AND PROGRAMMER***</td>
<td>1,200</td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td>3,200</td>
<td></td>
</tr>
</tbody>
</table>

* Design iterations = 1/2 (NRE) + 1/4 (simulation)
** 1 man week = $2,000
*** $1,200 = $60,000 total software and hardware cost ÷ 5-year life ÷ 10 designs/year

Gate Array Terms

NRE - Includes on-line vendor interface, design verification, mask charges, prototype samples, and a nominal simulation (pre- and post-layout) time.

Simulation - Additional simulation costs cover use of the vendor’s computer (typically a mainframe).

Time to Design - This covers extra design time.

Testability - To insure the device can be tested. Estimated engineering time is two weeks for a 10,000 usable gate array. One man-week is assumed to cost $2,000.
Design Iterations - This cost covers modifying the design, device prototyping, and initial customer evaluation. Cost is calculated by taking 1/2 of the total NRE plus 1/4 of the simulation time (charge). This cost assumes the ASIC customer wants to change the design. Vendor-caused design iterations are rare and the customer is usually not charged when they occur. Currently, design iterations for gate array and standard cell designs are needed much less frequently than in the mid to late 1980’s.

Test Program Development - The engineering time necessary to create test vectors, estimated at four weeks for a 10,000 usable-gate array. Once again, one man-week is assumed to cost $2,000.

PLD Terms

Simulation - PLDs do not need the extensive simulations that gate arrays require. However, high-density PLDs should be simulated. This model assumes 1 week for a 10,000 usable gate PLD with one man-week costing $2,000.

Software and Programmer - These are the programming tools and system that users purchase to program PLDs. The tools cost $60,000 with an estimated life (usefulness) of five years. Assuming there are 10 designs per year, the software cost per device is only $1,200.

Variable Costs

Variable costs are those that fluctuate in direct proportion to changes in output. The variable portion of the cost to the user is calculated by taking the product of three values: price-per-gate, total gates, and units (Figure 5-15). As shown, the price-per-gate for the PLD device is only four times the price of a similar density CMOS gate array. In 1993, the PLD was 15 times the cost of a similar density CMOS gate array.

Using the total cost formulas (Figure 5-15), the break-even point for the gate array and PLD can be derived. At the 10,000 usable gate level, the PLD solution is more cost effective at unit volumes below 2,500 (Figure 5-16).
As shown, it does not take a large number of units for the gate array approach to amortize its large fixed cost to the point where it becomes more cost effective than the PLD. The $24 PLD unit price versus the $6.00 gate array device price assures a fairly low-volume crossover point given almost any reasonable gate array NRE charge. Note that this is just one example. The user can perform the same set of calculations based on actual quoted prices for a specific application.

Because the NRE charge is such a small part of the total cost make-up of an FPGA, the total unit price of 10,000 usable gate device decreases only 37 percent when going from using 200 units to using 3,000 units. However, because such a large portion of the gate array total cost is NRE, the amortization of the NRE causes the 10,000 usable gate array total unit price to decrease about 91 percent when going from using 200 units to 3,000 units.

Figure 5-17 shows that whether at 200 or 3,000 units, a very high percentage of the gate array’s cost is due to fixed (i.e., NRE) costs. When the IC industry was slumping and heavily discounted NRE charges were the norm, the choice to use a gate array was very clear from the beginning. However, now that NRE charges have firmed, the PLD choice looks more attractive, especially at low unit volumes.

As shown, 96 percent of the cost of using PLDs at 3,000 units is from variable costs (i.e., the unit price). This is the reason it is so critical for the PLD producer to reduce device costs by using advanced processes (0.6µm or less) and interconnect (3-layers of metal or more) schemes, both of which result in reduced die sizes and lower unit costs.
If the FPGA and gate array price trends continue as mentioned in the previous paragraph, the relative FPGA/gate array price ratio by the end of the decade could be less than 2:1 (Figure 5-18). Given the time-to-market benefits of FPGAs, and less than a 2x price difference, it would be safe to assume that FPGAs would serve the vast majority of low gate count (≤40,000 gates) needs at that time. However as shown, the potential ASIC prices can still drop significantly and shift this crossover point.

As was discussed in the ASIC Technology Trends section, PLDs will continue to increase in density to compete with “low-end” gate arrays. The current definition of low-end for the gate array market are devices with less than 20,000 gates and speeds of less than 40MHz.

ICE estimates that about 20 percent of the total dollar volume of the CMOS gate array market could be defined as “low-end”. Thus, advanced PLD producers are attempting to use their 3-layer metal ≤0.6µm PLDs to target this multi-billion dollar low-end business of the CMOS gate array supplier.

Figure 5-17. 10K-Gate PLD Versus Gate Array Cost Make-Up
It is interesting to note that in most cases the CMOS gate array supplier is not fighting the PLDs attack on the low-end market. Most CMOS gate array suppliers are concentrating on the high-density, high-performance, and high unit volume segment of the gate array market.

What this now means as far as the trend lines shown in Figure 5-18 is that the low-end CMOS gate array price per gate may stay relatively flat in the future. With little competitive pressure, the low-end CMOS gate array price per gate could even increase in the late 1990’s. Low gate-count arrays could even be at a higher price per gate than PLDs after the year 2000!

Figure 5-19 shows how steeply MOS PLD prices are dropping. This example is the pricing pattern of Xilinx, who plans to continue the trend.

While the 30 percent or greater decline in the PLD price per gate may be difficult to sustain into the late 1990’s, there is little doubt that PLDs will become more competitive in price compared to low-end gate arrays. This is one reason that ICE is bullish about the future of the PLD/FPGA business (discussed in Section 4).
Time to Market

There is no doubt that when comparing specific unit costs of gate arrays (even including NREs) and PLDs, gate array devices look favorable at all but the lowest volume levels. Why then has there been a surge in the PLD market over the past few years? The answer is the increasing importance of the “time to market” factor. For example, in today’s high-end disk-drive market, lifecycles of six-months to a year are fairly common.

Time to market costs refer to lost margins incurred by the delay of the introduction of the system product into the marketplace. According to a McKinsey and Company study, one-third of the potential profit dollars are lost when the system is six months late to market (Figure 5-20). Thus, the off-the-shelf aspect of using PLDs instead of gate arrays becomes very attractive to conservative systems companies and those with very short market windows (the number of these systems houses is rapidly increasing). However, Hewlett-Packard offers an interesting philosophy on time-to-market by saying, “Time to market is a very high priority, but is not at the expense of technological innovation. There are times when we say we may not be the first with this, but we will be the best.”

Figure 5-19. Xilinx’s FPGA Price Reductions
A simple model that illustrates the concept of the importance of avoiding delays into the market is shown in Figure 5-21. The model was created by Logic Automation. It assumes that the market peak is in the middle of the total lifecycle timeframe, the revenue stream from a delayed entry parallels the on-time entry, and both the delayed and on-time market peaks are at the same point in time.

The percent of potential revenue lost by a delayed entry is expressed as \( \left( \frac{D (3W-D)}{2W^2} \right) \times 100 \). Thus, a product that is three months late in a market that will last 24 months would lose 34 percent of its possible potential market revenue \( \left( \frac{3(3x12-3)}{2x12^2} \right) \times 100 \). Some lost revenue dollar examples are also given in Figure 5-21. Although one can argue the assumptions of the model, the conclusion that time to market is of critical importance to most companies is irrefutable.

As is probably obvious by now, the choice between gate arrays and PLDs is getting more complex. Figure 5-22 summarizes some of the trade-offs of using PLDs versus gate arrays. In the near future, it appears that PLDs must be content to primarily service low unit volume, low density (compared to gate arrays), medium-performance designs, and/or those systems with short market windows. However, as has already been discussed, this will be a significant marketplace. Moreover, in the long run, PLDs may dominate the less than 40,000 gate marketplace based upon attractive price per gate costs!

There are a few companies (e.g., Orbit Semiconductor) that have developed programs to quickly convert a PLD design into a gate array when the unit volume of the PLD device rises. In these cases the user can have the best of both worlds — quick time to market with the PLD and low cost volume production of the gate array if system volume shipments take off. This is especially true for high density PLD devices where unit costs are extremely high. Obviously time-to-market will be the primary selling point for these high-density PLDs/FPGAs.
STANDARD CELLS VERSUS GATE ARRAYS

Similar to the on-going debate of when to use PLDs versus gate arrays, standard cell-based ASICs and gate arrays are oftentimes compared to each other and compete for many of the same applications. A good analysis on the topic of cells versus arrays, and the basis for this sub-section, is by R. Walker, J. Rau, and R. Brossart of LSI Logic.

In this analysis, LSI’s double-layer metal LMA9000 series gate array family was compared to its LCBV15 cell-based ASICs (both of which had 0.9 micron effective channel lengths). Although LSI has updated these ASIC families with much more advanced array- and cell-based ASIC technologies, the basic trade-offs between cells and arrays presented hereafter still hold true in today’s marketplace.
Given the same gate-limited design implemented in comparable cell and array technologies, cell-based designs will always yield a smaller die size. Three main reasons for this situation include:

1. Because of the ability to optimize transistor size and gate usage, random logic in cell-based designs requires about 15 percent less die area than in arrays.
2. ASIC memory (e.g., RAM or ROM) is implemented much more efficiently in cell-based designs as compared to array-based designs (not including embedded megacells).
3. With gate array masterslices typically coming in 30 percent increments in density (Figure 5-23), the odds are that an array-based design will result in some wasted die area as compared to standard cell designs.

The result of the manufacturing differences between cell and array wafers is that early in the production cycle, the array-based devices will typically cost less to produce than any specific cell-based device. This is in spite of the cell-based ASICs’ typically smaller die size and does not include or consider the lower NRE costs associated with array-based designs.

Figure 5-24 shows a 15,000 gate logic design implemented in array- and cell-based technologies. As shown, it takes 25,000 units before the smaller size of the cell technology die has enough of an effect on manufacturing cost to offset the cheaper array wafer (and thus die) production costs. At only 15,000 logic gate array densities, however, PLDs are now a competing ASIC alternative.

Figure 5-25 shows what happens when a logic design is mismatched to the array masterslice. In this example, only 37 percent (13K) of the logic gates were used (out of a possible 35K gates) as opposed to the typical 45 percent usage for double-layer metal arrays. As shown, the crossover point moves rapidly down to 10,000 units as the highly efficient cell-based die size competes very
well with this inefficient large gate array. The use of triple-layer metal has helped boost the usable gate percentage into the 60-70 percent range*. Of course the triple-layer metal arrays add complexity and cost to the manufacturing process.

<table>
<thead>
<tr>
<th>Part # (µPD659xx)</th>
<th>Raw Gates (K)</th>
<th>Usable Gates (K)</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>26</td>
<td>190</td>
<td>114</td>
<td>388</td>
</tr>
<tr>
<td>27</td>
<td>250</td>
<td>150</td>
<td>444</td>
</tr>
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<td>318</td>
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<td>500</td>
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<td>29</td>
<td>377</td>
<td>226</td>
<td>540</td>
</tr>
<tr>
<td>30</td>
<td>462</td>
<td>277</td>
<td>596</td>
</tr>
<tr>
<td>31</td>
<td>630</td>
<td>378</td>
<td>692</td>
</tr>
<tr>
<td>33</td>
<td>806</td>
<td>483</td>
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<td>1,076</td>
<td>646</td>
<td>892</td>
</tr>
<tr>
<td>37</td>
<td>1,545</td>
<td>927</td>
<td>1,060</td>
</tr>
<tr>
<td>39</td>
<td>1,990</td>
<td>1,194</td>
<td>1,204</td>
</tr>
</tbody>
</table>

*84-pin plastic DIP

*Source: NEC

Figure 5-23. NEC’s 0.35µm Gate Arrays (CMOS Family, 3-Layer Metal)

Figure 5-24. 15K Gate Random Logic Example*
The cell-based devices are very competitive with array technology when implementing memory. Figure 5-26 shows how the crossover point gets down to only 5,000 units for a 4,500 gate design with 4K of SRAM.

It should be remembered that in all of the previous examples, the amortization of NRE charges was not included. If NRE costs were included, the more expensive charges associated with cell-based ASICs would put the crossover points at slightly higher unit volume levels.

As was stated in the gate array versus PLD sub-section, the decision to use one ASIC method as opposed to another is multi-faceted. The same situation is very true when looking at using cells or arrays. The decision ultimately must be based on each application’s requirements.
Figure 5-27 shows some of the basic trade-offs between cell- and array-based ASICs. NEC states that about one-third of its cell-based customers desire analog functions on-chip. When implementing analog circuitry the cell-based design will almost always win versus the gate array.

One point that was not touched upon in the previous models was the packaging flexibility associated with cell-based designs. Because cell-based technology allows both smaller die size and the flexibility to make a longer and narrower die than arrays, the cell-based device can sometimes be housed in a less expensive or more readily available package type.

Whether it is cells versus arrays or arrays versus PLDs, it is imperative that potential ASIC users (or the manufacturers they trust) be aware of their technology options and intimately knowledgeable about their designs (and the systems in which their ASICs will be implemented).

OTHER ASIC COST CONSIDERATIONS

Price Per Gate

In the ASIC industry there is always a lot of discussion concerning price per gate. As has already been covered, the importance of price-per-gate figures is sometimes overestimated by the customer when choosing an ASIC methodology. However, when ASIC vendors, especially gate array suppliers, begin vying for a potential customer’s attention, price-per-gate figures are often the main topic of discussion.

Figure 5-28 shows a survey of some published ECL, BiCMOS, GaAs, and CMOS price-per-usable-gate figures. As shown, there is usually a wide range of prices, even for similar density devices.
For the CMOS gate arrays, the lower pricing points (0.02-0.04 cent per gate) in the lower curve on the chart, are typically 100,000 piece prices. The higher pricing points (0.06 cent per gate) are for low-density CMOS arrays with unit volume shipments of 1K to 10K.

In many cases for a given complexity and factory cost, there is a strong relation between the quoted market price and the quantity ordered. A typical curve of the ratio of price to cost (markup) by volume is shown in Figure 5-29. Note at low quantities the markup is in the range of 2 to 3, while at 100K to 1 million units the value tends to flatten out in the range of 1.5. These ratios are typical of the industry and are used to account for the fixed administrative costs for each new order.

Figure 5-28. Gate Array Price-Per-Gate

Notes:
- GaAs arrays in unit volumes of 20K.
- ECL arrays packaged in ceramic, and unit volumes of 1K.
- CMOS and BiCMOS arrays packaged in plastic QFP, feature size 0.35µ - 0.8µ, and unit volumes 5K to 10K.

Key
- ECL
- GaAs
- BiCMOS
- CMOS
- CMOS 100K+

Source: ICE

16725F
I/O Cost Factors

Because many users are demanding increased I/O capabilities from their ASICs (as many as two I/O pins for each 100 usable gates), some companies have begun pricing gate array families by pin. One reason for this is the cost of high pin count ceramic packages. In some cases the cost of the package can be 10X the cost of the die. An example of this type of pricing is shown in Figure 5-30.

Even with low cost plastic packages the chip I/O can determine the cost and price. With high pad/pin counts the die area and cost is determined not by the number of logic gates but by the area required for the bonding pads and the input protection networks. In addition to the added die cost the package cost will also increase. An example is shown in Figure 5-31 where by decreasing the pin requirement from 352 down to 144 pins, the final market price per gate was reduced by almost a factor of 4.

Note that the above comparison was based on a fixed bond pad pitch. Some companies achieve a fairly low area but high I/O design by using staggered bonding pads (shown in Section 6). Thus, by using staggered bonding pads and/or reducing the pitch between the pads, the die size can oftentimes be shrunk (especially in the frequently encountered “pad-limited” designs) and subsequently the die cost can be reduced. Another method to reduce the cost is to use a technique like the IBM “C4” process, where the I/O pads (bumps) are scattered over the die area. Techniques such as this can result in a significant cost advantage.
Performance

One formula that does hold true to form is that the customer must pay for performance. As shown, the price per gate escalates as one moves from the lower performance CMOS arrays to the high-speed ECL arrays (with a 100 to 1 price per gate ratio not uncommon).

According to ICE’s survey, the price per gate for BiCMOS versus CMOS gate arrays is from three to six times greater. Unisys, a large user of ASICs, showed a comparison (Figure 5-32) it had made when examining BiCMOS ASIC offerings. While the cost/performance ratio of the high-end...
BiCMOS versus CMOS ASICs does not look attractive, more than likely the high-end BiCMOS devices are competing against ECL and GaAs rather than CMOS. The cost/performance ratio for high-end BiCMOS versus ECL or GaAs puts the high-end BiCMOS technology in a more favorable competitive position.

![CMOS Versus BiCMOS ASIC Comparison](image)

**Figure 5-32. CMOS Versus BiCMOS ASIC Comparison**

**Standard Cells**

In general, the price-per-gate figures for standard cell devices average about the same as gate arrays. Although standard cell die sizes are typically smaller than similar density gate arrays, the more complex functions incorporated with standard cells (e.g., analog, MCUs, etc.) ultimately lead to fairly close price-per-gate figures. This, of course, does not include the amortization of the higher NRE charged for the standard cell parts. Because of the increasing use of analog, MPU, MCU, etc., functions on standard cell and gate array ASICs, direct price-per-gate comparisons are becoming more difficult and less applicable.

**Time Considerations**

The old phrase “time is money” is directly applicable to the ASIC industry. As mentioned earlier in this section, one of the primary benefits of using PLDs is off-the-shelf availability. As is exemplified by the sharply increasing PLD market, this benefit is worth the relatively high PLD unit price to many ASIC users.
Figure 5-33 shows the typical ASIC (not including PLDs) prototype and production lead-times. As shown, the typical time from a signed-off gate array design to the first available production quantities is nine weeks. For standard cells another five weeks is usually added.

As manufacturers have gotten better at producing ASICs, factory cycle times have improved (Figure 5-34). Moreover, ASIC manufacturers have also implemented specialized programs (e.g., wafer banking) in an attempt to further speed up delivery times to customers.

One of the more unique programs to speed up delivery of ASIC prototypes is offered by Chip Express (Santa Clara, CA). The company uses a laser-based trimmer to make up to 6,000 cuts per second with 0.2 micron tolerance to customize gate arrays having from 2,000 to 100,000 usable gates. A 40,000 usable gate device requires about 15 million cuts and can be customized in about two hours.

The average fee for two 20K gate prototype chips delivered in one week is about $12,500. Specialized one-day turnaround is also available at about double this price. Chip Express can deliver production volumes (50-1,000 pieces) of its gate arrays in two weeks using photomask technology (there is a one time $18K charge). Because of the special design of the base wafer, one photomask customizes two layers of metal (Figure 5-35).

**Figure 5-33. Typical ASIC Leadtimes**

![Bar chart showing typical ASIC leadtimes for prototypes and production.

Source: ICE]
Figure 5-34. Factory Cycle Time (Customer Order-to-Ship)

Figure 5-35. SEM View Illustrating Programmable Array Technology
For very high volumes (e.g., tens of thousands) of parts, Chip Express began offering what it calls its HARD (High Area Reduction Die) array. The HARD arrays are produced at IC foundries (e.g., Seiko Epson and Tower Semiconductor) using normal gate array photomask technology. As shown in Figure 5-36, the HARD array option now gives Chip Express prototype to production capability.

With the increasing customer demand for faster turnaround times we now have PLD vendors competing with gate array vendors as well as a few specialty gate array vendors attempting to match PLD availability characteristics. As always, the customer must weigh the benefit of fast turnaround versus its inevitable and sometimes significant price premium.

**Packaging Trends**

One significant cost trend is the increasing requirement for higher pin counts. As indicated there is typically a direct relation between package cost and pin count.

Historically, designers have been estimating the required number of I/O’s by applying “Rents Rule”. This is simply an empirical relation where the I/O’s are a function of the square of the gate count. A more accurate fit for present trends is the use of a “1/3 power” rule as shown below.

\[
I/O's = Gates^{0.33} \times 8
\]

The plot of this is shown in Figure 5-37
New sea-of-gates arrays are offering products with up to 1.3M usable gates. This is a major challenge to the packaging industry. As shown in Figure 5-37, ASICs with 100K-150K usable gates require packages with 300-500 pins. Even some 12,000 usable-gate devices are specifying packages with more than 200 pins. Figure 5-38 shows the numerous package types LSI Logic offers and the pin-count ranges of these packages.

Figure 5-39 shows some of the most commonly used plastic and ceramic packages and their average costs. It should be noted that all ceramic package types are hermetic, whereas plastic packages are non-hermetic.

For the high lead count ceramic packages, $0.08 per pin is typical. In some cases the package will cost more than the ASIC die! For the extremely high pin count devices (i.e., greater than 300 pins), TAB (tape automated bonding) or flip-chip bonding methods are displacing the typical wire-bonding techniques.

The packaging cost figures shown are only for the raw material. Typically, an additional $0.005 per package pin can be added for labor and overhead associated with the packaging operation. North American and European companies’ IC packaging is usually performed in areas such as the Philippines or Malaysia rather than in North America or Europe where labor rates are much lower (Figure 5-40). However, for quick turnaround, low-volume, or high ASP ASIC needs, local assembly is still sometimes a good alternative.
The issue of thermal management for high power IC devices is an additional cost factor. Ceramic heat spreader and lids, thermally enhanced epoxies, and many other solutions are used in combinations to achieve more effective thermal management solutions for these IC package types. IC thermal management will continue to become a more significant challenge to overall IC package costs, as the gate counts per device and IC junction temperatures dramatically increase.

**Test Concerns**

As ASIC devices have routinely begun to incorporate tens of thousands of usable gates, the testability issue has come to the forefront of ASIC user concerns (Figure 5-41). Most ASIC producers believe that ASIC users “should” be very concerned with testability when gate counts exceed 25K.

Test vector generation typically consumes about 40 percent of an ASIC’s design time (Figure 5-42). This is especially true for high-density ASICs. Figure 5-43 shows the typical development costs of a mixed-signal ASIC. As shown, almost one-third of the development cost was directly attributed to test engineering. Thus, considering the large amount of time and money spent addressing ASIC test, it is easy to see why it is such a hot topic.
An IC with several thousand transistors will have several thousand nodes that will switch between one and zero in the course of operation. If one of the nodes is frozen at either of the logic levels, it’s called a “stuck at” node, or a “fault.” This defect must be caught by the production test program. As the IC becomes more complex (more transistors), it becomes more difficult to test all nodes and catch all the “faults.” Hence, the phrase “fault coverage.”
Figure 5-41. Critical Issues for System Designers

Figure 5-42. Design Time by Task
It is estimated that more than 60 percent of the ASIC market requires better than 95 percent fault coverage with 50 percent of the market requiring 99 percent fault coverage.

Figure 5-44 shows how important high fault coverage is, especially for high-density ASICs. As shown, if you have only 95 percent fault coverage for a 100K gate array, about 80 defects per 1,000 parts will get through test undetected (not a very comforting thought for the ASIC user).

![Figure 5-44. Defect Rate Versus Fault Coverage](source)

![Figure 5-43. Mixed-Signal ASIC Development Cost Breakdown](source)
Currently, ASIC customers using gate arrays of less than 100,000 gate densities are still more interested in keeping the unit costs low by avoiding the use of on-chip test structures. Figure 5-45 shows some of the “costs” (i.e., overhead) of various testing options.

Figure 5-46 shows the added cost of applying some of these on-chip test approaches. With the larger gate counts, techniques such as boundary scan do not significantly increase the cost per bit and overall will reduce the test costs and thus the total device cost. Beyond the 100,000 gate level, some type or types of on-chip test is essential.

### MANUFACTURING COST EXAMPLES

Figure 5-47 shows an analysis of present and future CMOS gate arrays cost/price trends. In addition to the listed assumptions the following conditions are also assumed.

- A world class wafer fabrication facility running at 80% capacity
- Market prices based on committed quantities of 10,000 units
- Gate utilization of 70% for all examples
Note that the values assumed are not the maximum available for the period but represent the upper level of performance and complexity that is typical of the period. Figure 5-48 is a plot of the overall price trends through the year 2002.

**Defect Densities**

A key factor in future cost trends is the resultant defect densities in the new facilities. The defect density figures used in the gate array cost model are based on total fatal defects per square cm and are assumed to be randomly distributed. The wafer probe yield is based on an average of Murphy’s and Seeds yield equations and the global defect densities listed. (See ICE’s publication COST EFFECTIVE IC MANUFACTURING 1998-1999 for details.)

With the varied circuitry (e.g., SRAM, I/O, logic gates, etc.) on some of the advanced ASICs, yield models that account for the different defect densities have been developed.

One such model was described by Motorola at the 1994 Custom Integrated Circuits Conference. This model empirically derived “sensitivity” levels to describe how sensitive physical areas of the chip are to defects.
Defect sensitivity using an ASIC example is shown below.

I/O: 0.25
CMOS Logic Gates: 0.50
SRAM: 0.80

Thus, 25 percent of the I/O area, 50 percent of the logic area, and 80 percent of the SRAM area would be “fatal” to a defect. As would be expected, the “non-critical” feature sizes of the I/O as well as liberally spaced circuitry, only marginally expose the I/O area to fatal defects. However, tightly packed SRAM cells are highly susceptible to fatal defects with the logic gate figure falling somewhere between I/O and SRAM.

Overall, as ASICs begin to further incorporate large blocks of MPUs, memory, and other functions, formulas that account for area defect sensitivity will become more useful for estimating probe yield.

**Complexity**

Typically the ASIC manufacturer’s gross margin improves as gate density increases. This is the key reason that many gate array vendors are concentrating on high-density devices. As was discussed earlier, PLD vendors are targeting the low-end gate array market that many ASIC vendors are now de-emphasizing.
As shown in Figure 5-49, high-density gate arrays are among the largest devices produced in the IC industry. With only 112 total dice available for a 0.5-micron 125,000 usable gate array on a 150mm wafer, the high-density gate array will be a driving factor pushing the industry toward using 200mm and even 300mm wafers. Notice how large the die size is for the 0.8µm and 0.7µm 2-layer metal PLDs compared to gate arrays of similar density. No wonder the relative cost was so high for the PLDs. However, as was shown earlier, new architectures, sub-0.6µm feature sizes, and a move to 3-layer, and eventually 4-layer, metal is helping reduce die sizes and close the gate array/PLD pricing gap.