9 ROM, EPROM, & EEPROM TECHNOLOGY

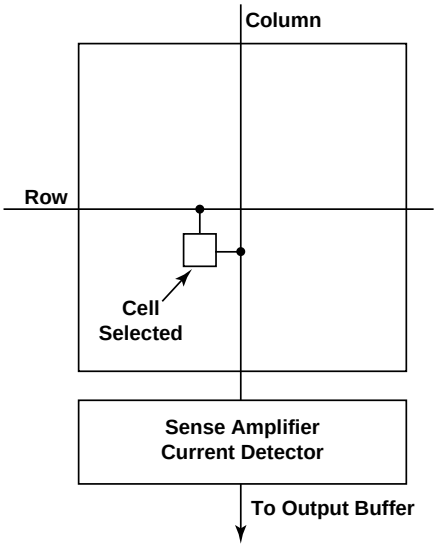
Overview

Read only memory devices are a special case of memory where, in normal system operation, the memory is read but not changed. Read only memories are non-volatile, that is, stored information is retained when the power is removed. The main read only memory devices are listed below:

ROM (Mask Programmable ROM —also called “MROMs”)
EPROM (UV Erasable and Electrically Programmable ROM)
OTP (One Time Programmable EPROM)
EEPROM (Electrically Erasable and Programmable ROM)
Flash Memory - These devices are covered in Section 10.

How the Device Works

The read only memory cell usually consists of a single transistor (ROM and EPROM cells consist of one transistor, EEPROM cells consists of two transistors). The gate threshold voltage of the transistor determines whether it is a “1” or “0”. During the read cycle, a voltage is placed on the gate of the cell. Depending on the programmed threshold voltage, the transistor will or will not drive a current. The sense amplifier will transform this current, or lack of current, into a “1” or “0”. Figure 9-1 shows how a read only memory works.



Source: ICE, "Memory 1996" 19956

Figure 9-1. Read Only Memory Schematic

Mask Programmable ROMs

Mask programmable ROMs (ROMs) are the least expensive type of solid state memory. They are primarily used for storing video game software and fixed data storage for electronic equipment, such as fonts for laser printers, dictionary data in word processors, and sound data in electronic musical instruments.

ROM programming is performed during IC fabrication. Several process alternatives can be used to program a ROM. These are:

- Metal contact to connect (or not to connect) a transistor to the bit line.
- Channel implant to create either an enhancement-mode transistor or a depletion-mode transistor.
- Thin or thick gate oxide, which creates either a standard transistor or a high threshold transistor, respectively.

The choice of these is a trade-off between process complexity, chip size, and manufacturing cycle time. A ROM programmed at the metal contact level will have the shortest manufacturing cycle time, as metallization is one of the last process steps. However, the size of the cell will be larger.

Figure 9-2 shows a ROM array programmed by channel implant. The transistor cell will have either a normal threshold (enhancement-mode device) or a very high threshold (higher than Vcc to assure the transistor will always be off). The cell array architecture is NOR. The different types of ROM architectures (NOR, NAND, ...) are detailed in the flash memory section.

Figure 9-3 shows an array of storage cells (NAND architecture) that consists of single transistors illustrated as devices 1 through 10 and 11 through 20 that is programmed with either a normal threshold (enhancement-mode device) or a negative threshold (depletion-mode device). The devices are read sequentially within the small groups. Two groups are shown in the drawing.

In 1995, a handful of manufacturers offered 64Mbit ROM devices. Power supplies ranged between 2.7V and 5.5V with access times in the range of 150ns. Hitachi announced a 3.3V 16Mbit ROM with a x32bit or x16bit organization and a burst mode (40ns access time). Random access time on the device was 120ns.

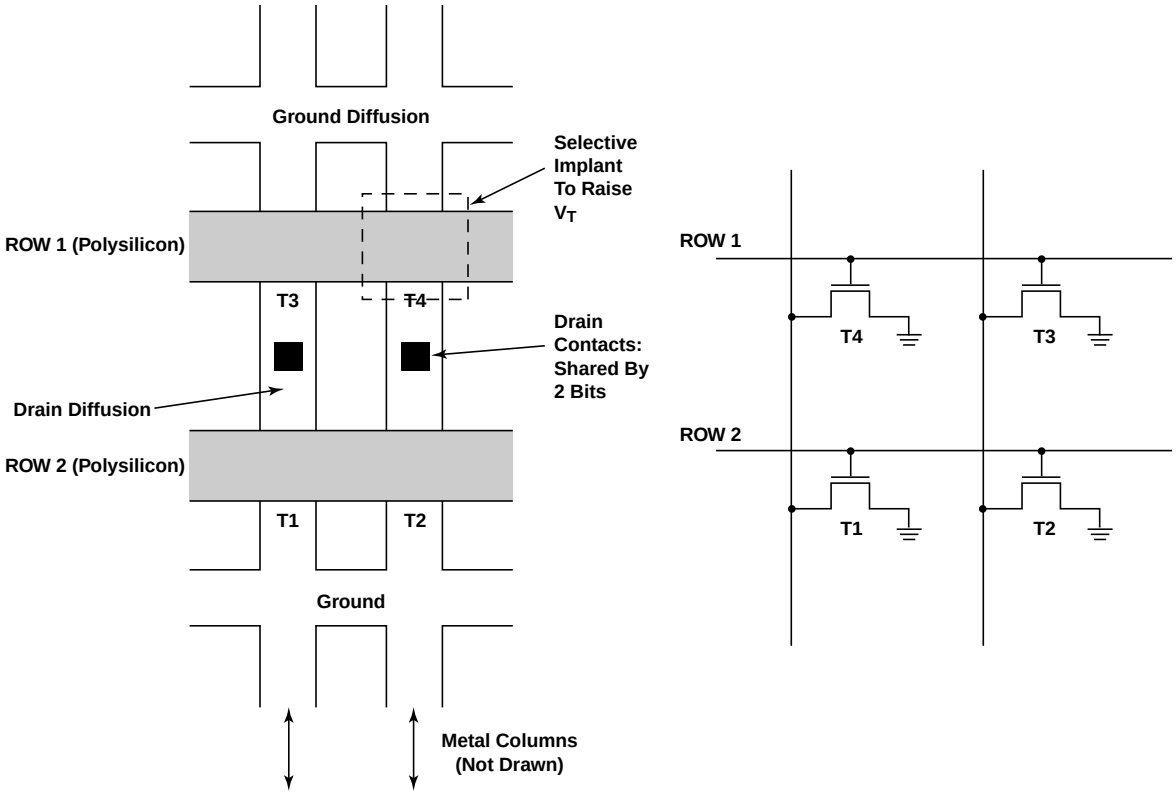


Figure 9-2. ROM Programmed by Channel Implant

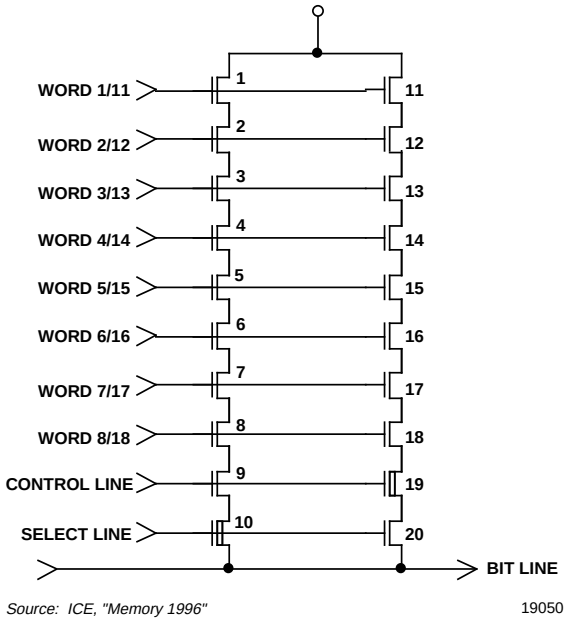


Figure 9-3. Memory Cell Schematic

Sharp integrated on a single chip a ROM and a Pseudo SRAM (PSRAM). Sharp called its 8Mbit device a ROM/RAM. The chip, configured 512Kbit x 16, contains 8Mbit of RAM and 2Kbit of ROM. This device:

- Allows RAM and ROM to be accessed at the same system speed to simplify address management and ease software development.

- Saves board space by combining functions that otherwise require multiple chips.

The ROM/RAM device has an access time of 80ns (170ns cycle time) and the power supply is 3V. The proposed application for DOS systems is shown in Figure 9-4.

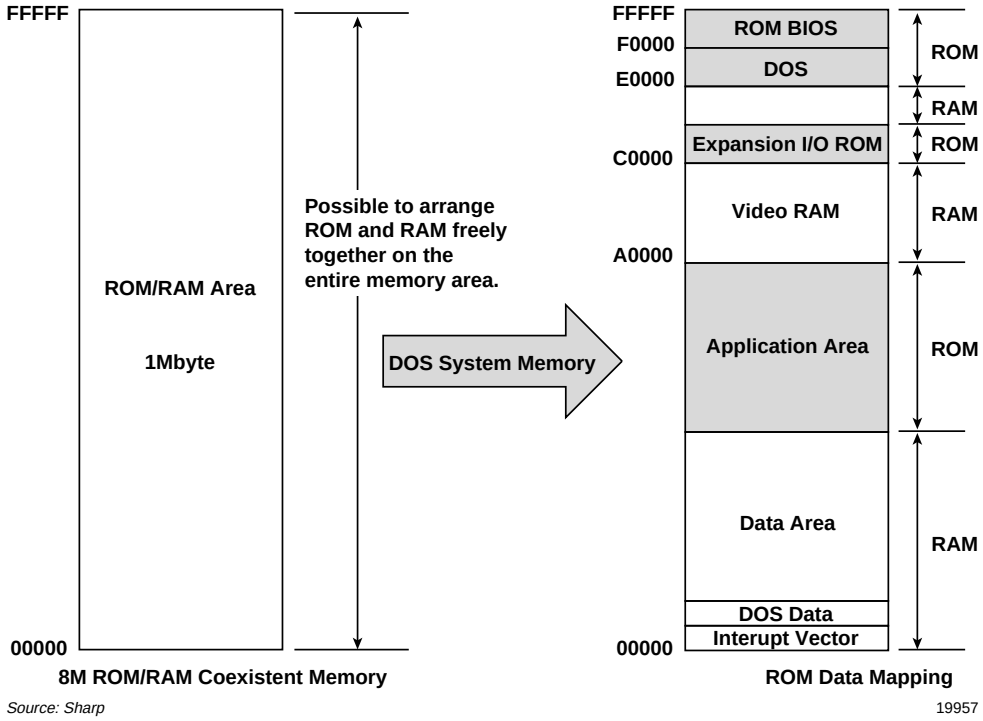


Figure 9-4. Sharp ROM/RAM Configuration Proposal

EPROM

EPROM (UV Erasable Programmable Read Only Memory) is a special type of ROM that is programmed in finished form (after device packaging), usually by the end user or system manufacturer.

The EPROM device is programmed by forcing an electrical charge on a small piece of polysilicon material (called a floating storage gate) located in the memory cell. When this charge is present on this gate, the cell is "programmed," usually a logic "0," and when it is not present, it is a logic "1." Figure 9-5 shows the cell used in a typical EPROM. The floating gate is where the electrical charge is stored.

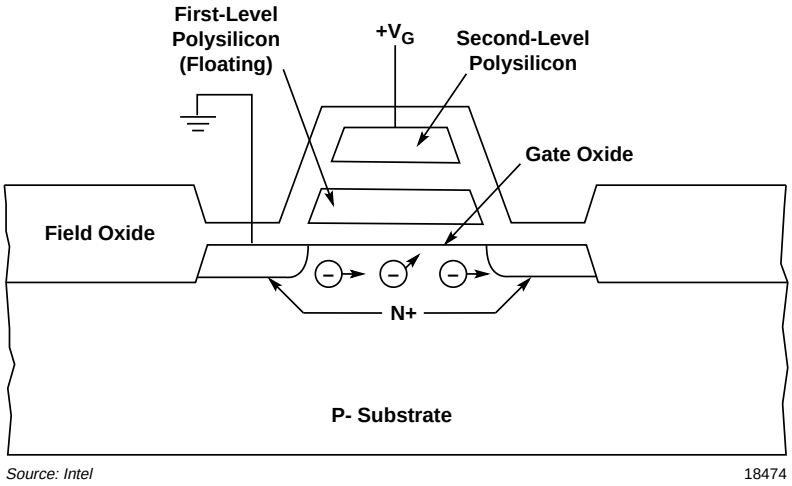


Figure 9-5. Double-Poly Structure (EPROM/Flash Memory Cell)

Prior to being programmed, an EPROM has to be erased. The EPROM is exposed to an ultraviolet light for approximately 20 minutes through a quartz window in its ceramic package. After erasure, new information can be programmed to the EPROM. After writing the data to the EPROM, an opaque label is placed over the quartz window to prevent accidental erasure.

Programming is accomplished through a phenomenon called hot electron injection. High voltages are applied to the select gate and drain connections of the cell transistor. The select gate of the transistor is pulsed "on" causing a large drain current to flow. The large bias voltage on the gate connection attracts electrons that penetrate the thin gate oxide and are stored on the floating gate.

EPROM Floating Gate Transistor Characteristic Theory

The following explanation is also true for EEPROM and flash devices.

Figure 9-6 (a) and (b) shows the cross section of a conventional MOS transistor and a floating gate transistor, respectively. The upper gate in Figure 9-6 (b) is the control gate and the lower gate, completely isolated within the gate oxide, is the floating gate. C_{FG}

and C_{FS} are the capacitances between the floating gate and the control gate and substrate, respectively. V_G and V_F are the voltages of the control gate and the floating gate, respectively. $-Q_F$ is the charge in the floating gate. (As electrons have a negative charge, we added a negative sign). In an equilibrium state, the sum of the charges equals zero.

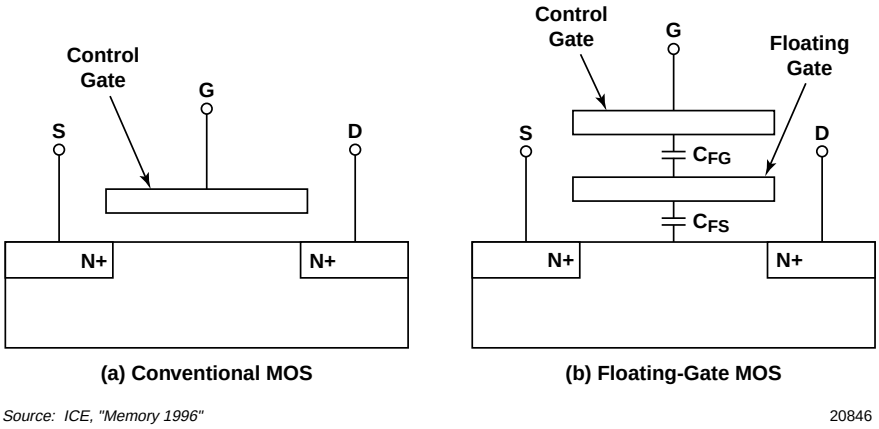


Figure 9-6. Cross Section of a Conventional MOS Transistor and a Floating-Gate MOS Transistor

$$(V_G - V_F)\, C_{FG} + (0 - V_F)\, C_{FS} - Q_F = 0$$

$$V_F = \left(\frac{C_{FG}}{C_{FG} + C_{FS}}\right) V_G - \frac{Q_F}{C_{FG} + C_{FS}}$$

V_{TC} is the threshold voltage of the conventional transistor, and V_{TCG} is the threshold voltage of the floating gate transistor:

$$V_{TCG} = \left(\frac{C_{FG}}{C_{FG} + C_{FS}}\right) V_{TC} - \frac{Q_F}{C_{FG} + C_{FS}}$$

$$V_{TCG} = V_{TO} - \frac{Q_F}{C_G}$$

$$\text{Where } V_{TO} = \left(\frac{C_{FG}}{C_{FG} + C_{FS}}\right) V_{TC} \quad \text{and} \quad C_G = C_{FG} + C_{FS}$$

The threshold voltage of the floating gate transistor (V_{TCG}) will be V_{TO} (around 1V) plus a term depending on the charge trapped in the floating gate. If no electrons are in the floating gate, then $V_{TCG} = V_{TO}$ (around 1V). If electrons have been trapped in the floating gate, then $V_{TCG} = V_{TO} - Q_F/C_G$ (around 8V for a 5V part). This voltage is process and design dependent. Figure 9-7 shows the threshold voltage shift of an EPROM cell.

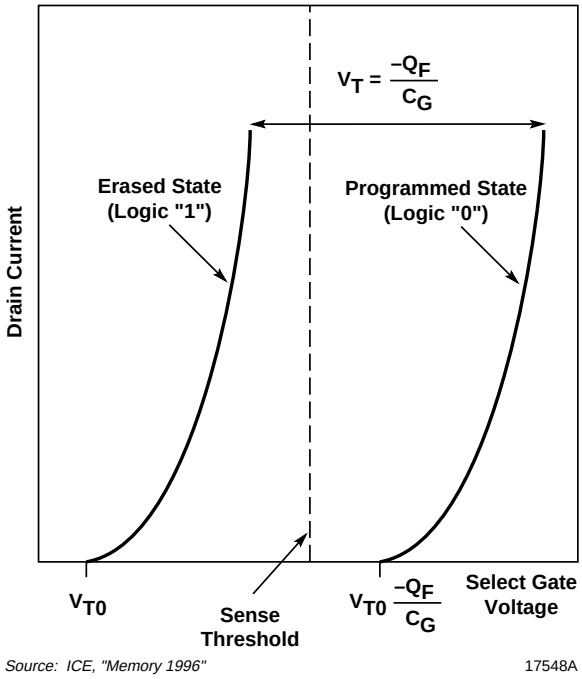


Figure 9-7. Electrical Characteristics of an EPROM

The programming (write cycle) of an EPROM takes several hundred milliseconds. Usually a byte — eight bits — is addressed with each write cycle. The read time is comparable to that of fast ROMs and DRAMs (i.e., several tens of nanoseconds). In those applications where programs are stored in EPROMs, the CPU can run at normal speeds.

Field programmability is the EPROM's main advantage over the ROM. It allows the user to buy mass-produced devices and program each device for a specific need. This characteristic also makes the EPROM ideal for small-volume applications, as the devices are programmed in very small quantities. Also, the systems supplier can program any last minute upgrades to the program placed on the chip just before shipment.

EPROM cells may be configured in the NAND structure shown previously, or, more commonly, in the NOR configuration shown in Figure 9-8.

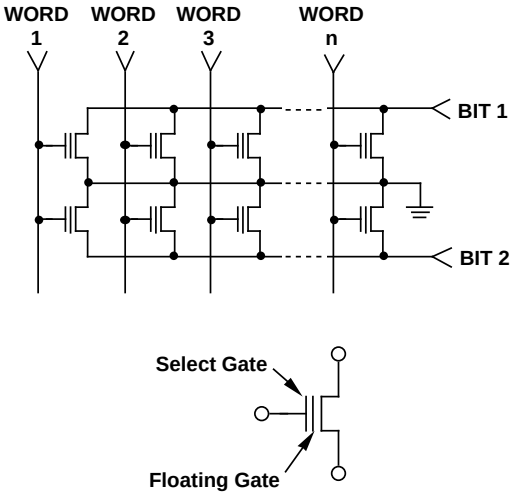


Figure 9-8. EPROM NOR Configuration

Figure 9-9 shows a Transmission Electron Microscope (TEM) cross section of an EPROM cell. The oxide between the substrate and the floating polysilicon gate is approximately 150Å thick.

Figure 9-9. EPROM Cell Cross Section

EPROMs were created in the 1970's and have long been the cornerstone of the non-volatile memory market. But the development of flash memory devices (see Section 10) will lead to a loss of EPROM marketshare. For this reason few suppliers are developing higher density parts but are focusing on niche applications.

OTP (One Time Programmable)

The standard ceramic package of an EPROM is expensive. In most applications, EPROMs are programmed one time and will never have to be erased. To reduce the cost for these applications, EPROMs may be manufactured in opaque plastic packages, and are then referred to as One Time Programmable (OTP) devices. These cannot be erased.

EEPROM

EEPROM (Electrically Erasable Programmable ROM) offer users excellent capabilities and performance. A single power supply is required. Write and erase operations are performed on a byte per byte basis.

The EEPROM cell is composed of two transistors. The storage transistor has a floating gate (similar to the EPROM storage transistor) that will trap electrons. In addition, there is an access transistor, which is required for the erase operation.

Figure 9-10 shows a comparison table of different non-volatile memory cells. Figure 9-11 shows the EEPROM cell schematic. Figure 9-12 shows the voltages applied on the memory cell to program / erase a cell. Note that an EPROM cell is erased when electrons are removed from the floating gate and that the EEPROM cell is erased when the electrons are trapped in the floating cell. To have products electrically compatible, the logic path of both types of product will give a "1" for erase state and a "0" for a programmed state. Figure 9-13 and Figure 9-14 show the electrical differences between EPROM and EEPROM cells.

Multi-Level Analog Storage EEPROM

Some companies, in particular Intel, have initiated work on 4-level non-volatile memories for digital application. These devices are currently in the development stage.

However, Information Storage Devices (ISD) has proposed a 256-level non-volatile cell for analog storage. ISD presented a 480Kbit EEPROM at the 1996 ISSCC conference. The multilevel storage cell is able to store 256 different levels between 0V and 2V. This means the cell needs to have a 7.5mV resolution. The 256 different levels in one cell corresponds

to 8 bits of information. A comparable digital implementation requires 3.84Mbit memory elements to store the same amount of information. The information stored will not be 100 percent accurate but is good enough for audio applications that allows some errors.

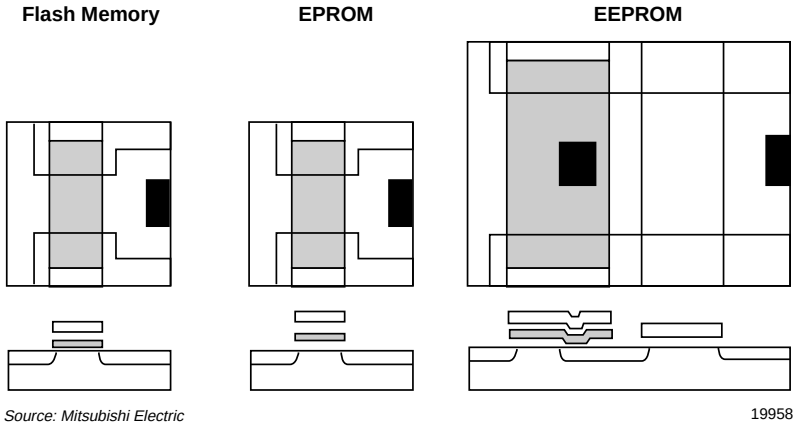


Figure 9-10. Comparison of Non-Volatile Memory Cell Sizes

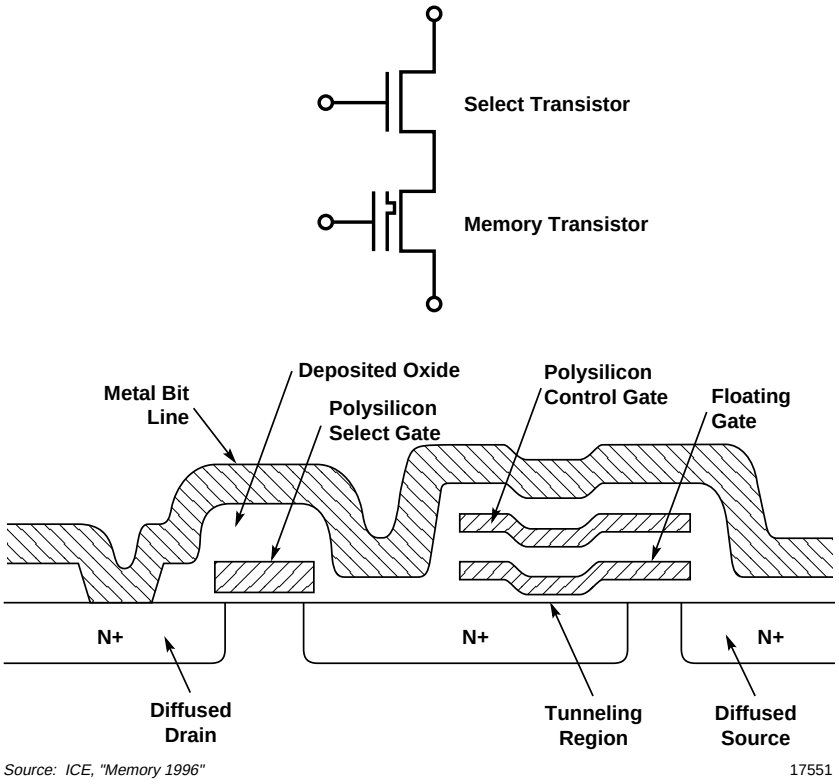
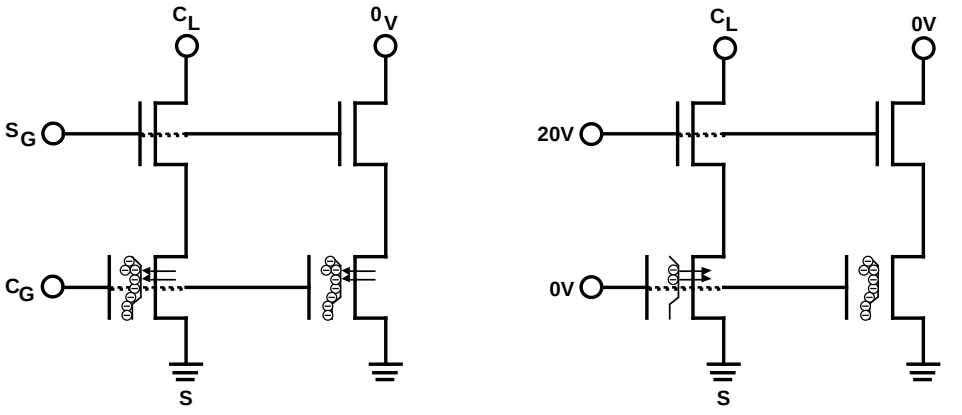
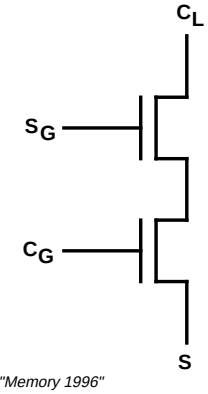


Figure 9-11. EEPROM Cell





	S_G	C_L	C_G	S
Erase	V_{PP}	0	V_{PP}	0
Program	V_{PP}	V_{PP}	0	0
Read	V_{CC}	1	V_{CC}	0
Unselected	0	X	0	0

Source: ICE, "Memory 1996" 17554A

Figure 9-12. EEPROM Cell Program/Erase

EPROM	versus	EEPROM
Hot electron injection		Fowler Nordeim tunneling
1 transistor cell		2 transistor cell
Oxide ≈ 150Å		Oxide ≈ 80Å
↓		↓
I_{PP} current		No I_{PP} current
↓		↓
External V_{PP}		Internal V_{PP}

Source: ICE, "Memory 1996" 17555

Figure 9-13. Electrical Differences Between EPROM and EEPROM

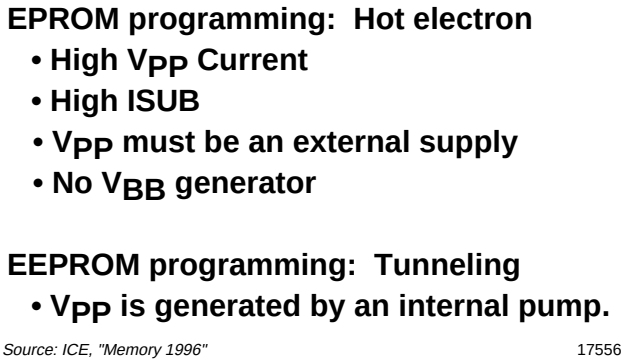


Figure 9-14. V_{PP} EPROM Versus V_{PP} EEPROM

Reliability Concerns

ROMs are actually arrays of transistors, and therefore demonstrate no special reliability problems.

The EPROM device has the potential for system reliability problems due to leakage of charge off the storage gate. Over the years this has been determined not to be a problem.

The weakness comes from the use of "higher than normal" voltages on the cell transistors. These high voltages can exaggerate defects in oxide films that are less than perfect. The screening procedures overstress the devices so that weak transistors fail before final test.

EEPROM and flash devices use two types of basic processes — single poly and double poly. Serial EEPROMs and some of the parallel EEPROMs and flash devices use the single poly. This technology offers better reliability in terms of program / erase cycles, about ten times the double poly process. Some single poly devices guarantee one million cycles.

Thin tunneling oxide is a critical manufacturing step for EEPROMs. During programming and erase cycles, high voltage is applied across the thin oxide. The reliability problem with the thin tunnel oxide comes from the fact that in order to cause cold electron tunneling, the voltage across the dielectric must be very close to the rupture voltage.

Performance

The read cycles of read only memories are dependent on the design goals rather than inherent device limitations. The NAND structure is slower than the NOR structure, but offers greater packing densities. The NOR structures can be designed to operate faster

than DRAMs of similar feature size, but are usually designed for density and cost rather than speed. Fast devices have access times between 20ns and 50ns and slower devices are generally over 100ns (both in NOR structures).

Cell Size and Die Size

The cell size for the ROM is potentially the smallest of any type of memory device, as it is a single transistor. A typical 8Mbit ROM would have a cell size of about 4.5μm^2 for a 0.7μm feature size process, and a chip area of about 76mm^2. An announced 64Mbit ROM, manufactured with a 0.6μm feature size, has a 1.23μm^2 cell on a 200mm^2 die. The device is wired in the NOR configuration, which improves system performance.

The ROM process is the simplest of all memory processes, usually requiring only one layer of polysilicon and one layer of metal. There are no special film deposition or etch requirements, so yields are the highest of all memory chips of the same density.

The cell size of the EPROM is also relatively small. The EPROM requires one additional polysilicon layer, and will usually have slightly lower yields due to the requirement for nearly perfect (and thin) gate oxides.

These factors, plus the fact that an EPROM is encased in a ceramic package with a quartz window, make the EPROM average selling price three to five times the price of the mask ROM.

There are two distinct EEPROM families: serial and parallel access. The serial access represents 90 percent of the overall EEPROM market.

Serial access EEPROMs feature low pin count. Typically they are packaged in an 8-pin package:

- 2 pins for power voltage,
- 1 pin for Read / Write control,
- 1 pin for the clock,
- 1 pin for Input / Output,
- 3 pins for Chip Enable.

Serial EEPROMs are readily available in low densities (typically from 256 bit to 256Kbit). Parallel EEPROMs typically start at the 256Kbit level and increase to bigger densities.

The EEPROM requires much more silicon area per bit because of the access transistor required for each cell. However, the EEPROM structure will continue to be used in those ROM applications where erasure on a bit level is needed.

Figure 9-15 shows the physical geometries of EPROMs and EEPROMs analyzed by the ICE laboratory in 1995.

	XICOR XC28C010 1Mbit 9443	HITACHI HN58C1001P-12 1Mbit 1994 - 1995	ATMEL AT27C010-45 1Mbit 9428	ISSI IS27HC010 1Mbit 1994 - 1995
Technology	**EEPROM**	**EEPROM**	**EPROM**	**EPROM**
Die Size	**5.7 x 8.9mm ($51mm^2$)**	**6.1 x 8.2mm ($50mm^2$)**	**3.4 x 4.3mm ($14.6mm^2$)**	**4 x 4.5mm ($18mm^2$)**
Min Gate - (N)	**1.3μm**	**0.6μm**	**0.6μm**	**0.7μm**
Cell Pitch	**2.6 x 8.1μm**	**4.25 x 5.3μm**	**2.1 x 2.1μm**	**2.5 x 2.7μm**
Cell Area	**$21\mu m^2$**	**$22.5\mu m^2$**	**$4.4\mu m^2$**	**$6.8\mu m^2$**

Source: ICE, "Memory 1996" 20847

Figure 9-15. Physical Geometries of EPROMs and EEPROMs