Acceptor
An impurity that can make a semiconductor P-type by causing the absence of electrons in the conduction band (called “holes”). These holes are carriers of positive charge.

Access Time
Time needed by the device to present the data out after the address has been validated.

Active Component
A (non-mechanical) circuit component that has gain or switches current flow, such as a diode, transistor, etc.

Alignment
The arranging of a mask and wafer in correct positions with respect to each other. After alignment, radiation-sensitive photoresist on the wafer is exposed by radiation passing through the non-opaque areas of the mask.

Amplifier
A device that uses an active component to increase the voltage or power of a signal without distorting its waveshape.

Analog
A continuous, non-digital representation of phenomena. An analog voltage, for example, may take any value.

AND Gate
A gate whose output is ON only if all input signals are ON.

Angstrom
A unit of length measuring 1/10,000 of a micrometer (10⁻⁴µm).

Array
A group of items arranged in rows and columns. Termed cell array for memory devices. See Core.
Arse nic
An N-type dopant used as an implant source/drain for NMOS type transistors.

ASIC
Application specific integrated circuit. An IC designed to meet a specific customer requirement.

ASM
Application-specific memory.

ASP
Average selling price.

Assembly
The final stage of semiconductor manufacturing where the active device is encased in a plastic, ceramic, or metal package. Referred to as “back-end” processing.

Asynchronous
When outputs change states in time with an address change.

ATA Card
AT-Attachment interface standard used for miniature flash cards.

ATD
Address Transition Detection. Circuit added in some static memories (SRAM, ROM, EPROM ...), to generate an internal clock each time a new address is presented.

ARAM
Audio RAM. DRAM used for audio applications.

Avalanche Injection
Hot electron or avalanche injection is a mechanism used to charge the floating gate with electrons.

Bandwidth
The measure of an amount of data that can be transferred in a given time. Typically described in megabytes per second.

BiCMOS
Bipolar-CMOS. A technology made by combining bipolar and CMOS technologies on the same chip.
Binary
A system of numbers using 2 as a base, in contrast to the decimal system which uses 10 as a base. The binary system requires only two symbols: 0 and 1.

BIOS
Basic Input and Output System. PC code storage used when turning on a PC.

BIST
Built In Self Test. Method of testing an IC that uses special circuits designed into the device.

Bit
A binary digit. A bit is the smallest unit of storage in a digital component.

Bit-line
Also called column.

Block Diagram
Drawing representing the main functional blocks of a device.

Boron
An P-type dopant used as an implant source/drain for PMOS type transistors.

BRAM
Battery RAM. SRAM with a small battery inserted in the package to hold the stored information during power off.

Breakdown Voltage
A high voltage resulting from an electrical field being sufficient to cause a high level of conductance. The breakdown voltage of a junction is generally non-destructive.

Burst
Read or write cycles, generally in bursts of four, that are automatically sequenced by the memory chip. To accomplish this, a special pipeline stage and a two-bit counter are added.

Bus
Group of several signals. For example the address bus.

Byte
Information of 8 bits. Also called word.
Cache
High-speed SRAM memories used between the microprocessor and the main memory (DRAM) to increase the bandwidth and reduce the latency. See L1 and L2 caches.

CAGR
Cumulative Average Annual Growth Rate.

CAM
Content Addressable Memory.

Capacitance (C)
The capability of storing electrical charge. Unit of measure is the Farad (F).

CAS
Column Address Strobe. Clock used in DRAM to validate the column addresses.

CD-ROM
Compact-Disk ROM.

CDRAM
Cache DRAM. Memory integrating DRAM plus some L2 cache SRAM.

CE, CS
Chip enable or chip select. This signal active or inactive (power down) the device. When inactive, the device cannot be addressed, but keeps its information.

Cell
Also called memory cell. Elementary structure on which on bit of information is stored. With the development of multi-level cell, there will be more than one bit of information per cell.

Channel Length
Path between the source and the drain of the MOS transistor. Major element the of transistor, the channel length is used to define the technology level.

Chip
An integrated circuit or discrete device. Also called a die.

Circuit Design
Techniques used to connect devices (transistors, capacitors, resistors, etc.) to perform a function.
Circuit Layout
See Layout.

Cleanroom Class
Government specification FED-STD-209 that defines the number of particles of a given size and distribution per cubic volume of space for each class.

Clock Frequency
The master frequency of the periodic pulses that synchronizes operations of a logic circuit.

CMOS
Complementary metal-oxide semiconductor. A technology made by combining NMOS and PMOS transistors.

Cold-Electron Tunneling
See Fowler-Nordheim tunneling.

Core
Part of the memory device where the cells are located. Also called memory array.

CPU
Central Processing Unit. The CPU is the brain of the computer.

Critical Dimensions (CD)
The width or space of critical circuit elements in an integrated circuit.

Current (I)
The flow of electrons. Usually measured in Amperes (A).

Data
Any information stored or retrieved from a memory device.

Data Sheet
Technical paper giving the complete characteristics of a memory device.

Date Code
Manufacturing date usually indicated on the package.

DC Test
A sequence of direct current measurements performed in IC pads to determine probe contact, leakage currents, voltages levels on inputs and outputs, power supply currents, etc.
DDR
(Double Data Rate). Information transferred on both edge of a clock.

Defect
Physical abnormality in an IC. A defect may or may not result in a fault in the logical functioning of a chip.

Density (memory)
Number of cells (or bits) stored in a memory. 1Mbit, 4Mbit, 16Mbit, etc.

Depletion Transistor
An NMOS transistor with a negative threshold voltage.

Depletion Region
That area at a P-N junction which, when reverse biased, is swept clear of free charges.

Design Rules
Rules that state the allowable dimensions of features used in the design and layouts of an IC. Rules unique to a specific process technology, including minimum width, minimum separation, layer to layer overlap, etc.

Die
A single square or rectangular piece of semiconductor material into which a specific circuit has been fabricated. Plural is dice.

Digital
A method of representing information in an electrical circuit by switching the current ON or OFF. Only two states are possible, usually represented by “0” and “1”.

Digital Circuit
A circuit that operates like a switch and can perform logical functions. Used in computers or similar logic-based equipment.

DINOR
Internal cell core architecture used mainly for flash.

Diode
A two-terminal device that allows current to flow in one direction but not the other. A diode is present at the intersection (junction) of a P-type and an N-type semiconductor.
Direct Current
The flow of electrons that only goes in one direction. Abbreviated DC.

Doping
The introduction of a dopant into a semiconductor to modify its electrical properties by creating a concentration of N or P carriers. Doping is normally accomplished through diffusion or ion implantation processes.

Drain
The working current terminal (at one end of the channel in a MOS transistor) that is a drain for holes or free electrons exiting from channel.

DRAM
Dynamic Random Access Memory. Device used for main memory in subsystems. The elementary cells must be periodically refreshed.

Driver
An element that is coupled to the output stage of a circuit in order to increase its power, current handling capability, or fanout. For example, an address driver is used to supply the current necessary for an address line.

Dual-Port DRAM
See Video DRAM.

Dummy Cell
Mainly used in DRAMs, the dummy cells are additional cells used as reference by the sense amplifier during read cycle.

DUT
Device Under Test.

EDO
Extended Data Out DRAM. Also called Hyper Page Mode DRAM. Improvement of the Fast Page Mode by latching the old output data while new data is addressed.

EDRAM
Enhanced DRAM. DRAM taking advantage of the internal architecture of a standard Fast Page Mode by using the sense amplifiers as an internal Level 2 Cache SRAM.
EEPROM
(Electrically-Erasable PROM). Similar to ROM, but with the capacity of selective erasure and programming through electrical stimulus.

Electron
An elementary, negatively charged atomic particle.

Enhancement Transistor
NMOS transistor with a positive threshold voltage ($V_t$) or PMOS transistor with negative $V_t$.

Epi
Short for epitaxy, the controlled growth of a layer of crystalline semiconductor material on a suitable substrate.

EPROM
Erasable Programmable ROM. Also called UV-EPROM. The information is written (programmed) electrically by hot electrons and erased using an Ultra Violet source. The package is in ceramic with a quartz window to allow the UV light to reach the die.

Erasure
The action of removing the information of a non-volatile memory. Erasure is in bulk, for the whole chip, or in blocks or sectors.

ESD
Electrostatic discharge.

Fab
Wafer manufacturing fabrication facility.

Fabless
A semiconductor company that does not have its own wafer manufacturing facility, but subcontracts the wafer manufacturing.

Fabrication
In semiconductor manufacturing, fabrication usually refers to the (front-end) process of making devices in semiconductor wafers, but usually does not include the packaging, assembly, and test (back-end) stages.

Failure Analysis
An orderly procedure for determining the reason that an IC device has failed. The results are frequently useful for enhancing the reliability of subsequent products.
Failure in Time
One failure in $10^9$ device hours.

Failure Rate
A rate of failure per unit time. Semiconductors are usually measured in failures per 1,000 hours.

Feature Size
See Minimum Geometry.

Femto
A prefix meaning one quadrillionth ($10^{-15}$). Symbol is f.

Field Oxide
A thick layer of dielectric, generally silicon dioxide, that covers the inactive portion of the semiconductor surface.

FIFO
First In First Out.

Final Test
The electrical evaluation of the packaged device.

FIT
See Failure in Time.

Flash
Non-volatile memory with characteristics like an EPROM or EEPROM.

Flip-Flop
An electrical circuit having two stable states: ON and OFF. The main element of an SRAM cell.

Floating Gate
Piece of polysilicon in the EEPROM, EPROM and flash memory cells where the data is stored.

Fowler-Nordheim Tunneling
Cold electron or Fowler-Nordheim tunneling is used for program/erase of EEPROM and flash memory devices. It is a quantum-mechanical effect that allows electrons to pass through a gate oxide and to be trapped in the floating gate.
**Glossary of Terms**

**FPM**
Fast Page Mode. See Page Mode.

**FRAM**
Ferroelectric RAM. The cell is similar to an DRAM cell, but the cell capacitor dielectric is made of ferroelectric material, which keeps the information when the power supply is off.

**Frequency**
The number of times per second an alternating signal goes through a complete cycle. Expressed in Hertz (Hz).

**Functional Test**
Tests to determine whether the logic and analog behavior of a circuit is correct.

**Fuse**
A circuit element used in MOS memory circuits as programmable connection in the redundancy circuitry.

**Gate**
The primary control terminal of a MOS transistor.

**Gate Oxide**
The thin layer of thermal oxide separating the gate electrode (terminal) from the semiconductor substrate.

**Giga**
Prefix meaning one billion ($10^9$). Symbol is G.

**Glassivation**
Passivation using silicon dioxide (glass).

**Granularity**
Granularity quantifies the smallest memory increment available to expand a memory system.

**Hi-Z**
High-Impedance. Used for an output in Hi-Z state.

**Hole**
The absence of a valence electron in a semiconductor crystal. The movement of a hole is equivalent to the movement of a positive charge.
Hot Electrons
   See avalanche injection.

IC
   Integrated circuit. A semiconductor die containing multiple elements that act together to form the complete device circuit.

Interconnect
   A conductive connection between two or more circuit elements. The conductors among elements (transistors, resistors, etc.) on an integrated circuit or between components on a printed board circuit.

Ion
   An atom that has either gained or lost electrons making it a charged particle (either negative or positive, respectively).

Ion Implantation
   A means for adding dopants to a semiconductor material. Ions are accelerated in an electrical field into the semiconductor material. It is especially useful for thin doped areas. This process is much more precise than the diffusion method of doping.

I/O
   Input/Output.

ISSCC

Junction (P-N)
   The line of demarcation where the number of P- and N-type carriers are exactly equal with a surplus of P-type on one side and N-type on the other.

KGD
   Known Good Die. Die tested to be sold as bare die.

Kilo
   A prefix meaning a multiple of 1,000 ($10^3$).
L1/ L2 Cache
L1 (Level 1) cache memories are incorporated in silicon directly on the microprocessor. L2 (Level 2) cache memories are a separate chip located between the microprocessor and the main memory. Also see Cache.

LAN
Local Area Network.

Latch-Up
Condition that occurs when a parasitic PNPN structure in a CMOS device triggers due to silicon controlled rectified (SCR) action.

Latency
Refers to the delay needed to access the first memory byte. Subsequent byte access times will be defined by the bandwidth.

Layout
The physical arrangement of all the circuit elements on the surface of the device.

Leakage Current
Parasitic small current due to non-perfect device isolation. The leakage current in DRAM cells requires a DRAM refresh.

Lifecycle
The different steps of a device, from its market introduction, through growth maturity, saturation, decline to its obsolete stage.

Lithography
The transfer of a pattern or image from one medium to another, as from a mask to a wafer. If light is used to effect the transfer, the term, “photolithography” applies.

Mask
A transparent (glass or quartz) plate covered with an array of patterns used in making ICs. Each pattern consists of opaque areas that prevent light passage. The mask is used to expose photoresist that defines areas that will later be etched on a wafer.

MLC
Multi Level Cell. A cell that is able to store more than one bit of information. Still in development for digital applications.
MPU
Microprocessor Unit.

NAND Configuration
Internal cell configuration used mainly for flash memory.

NMOS
N channel transistor. The source and drain of the transistor is N doped. The transistor is on when the gate voltage is increased.

Node
Area in an integrated circuit not separated by an active of passive device; interconnect area.

Non-Volatile Memory
Memory that does not lose its content after power-off. Essentially ROM, EPROM, EEPROM, and flash memory.

NOVRAM
Non-volatile RAM. See NVRAM.

NVRAM
Non-volatile RAM. SRAM with an EEPROM back-up to store the data during power-off.

OE
Output Enable. Signal that controls the high impedance of valid states on the data out.

OEM
Original Equipment Manufacturer.

OTP
One Time Programmable EPROM. EPROM packaged in a plastic or ceramic windowless package. The device cannot be erased as the package is hermetic to UV light.

Package
The protective container for an electronic component, with terminals to provide electrical access to the components inside.

Page Mode
A feature mainly used for DRAMs but which can also but used on other memory types that addresses data from a same row to increase the bandwidth.
Parallel Access
A feature of a memory by which all the bits of a byte are entered or retrieved simultaneously.

PC
Personal computer.

PCMCIA Card
Personal Computer Memory Card International Association card.

PDA
Personal Digital Assistant.

Pipeline
Register added between the memory array and the output.

PMOS
P-channel transistor. The source and drain of the transistor are P doped. The transistor is on when the gate voltage is decreased.

Power-Down
A mode of a memory during which the device is operating in a low-power or standby mode.

Process
A series of manufacturing steps and a set of conditions which together produce the integrated circuit.

Program Enable
An input signal, which, when true, puts a programmable memory into a program mode.

Programming
Writing new information to memory. Term normally used for non-volatile memories (EPROM, EEPROM, Flash). For volatile memories (RAM), the term “writing” is used in place of “programming.”

PSRAM
Pseudo Static DRAM. A DRAM with internal refresh circuitry that performs like an SRAM.

Quartz Window
Quartz included in a ceramic package of EPROMs to allow the UV light to reach the silicon during erase step.
RAS
Row Address Strobe. Clock used in DRAM to validate the row addresses.

R&D
Research and Development.

RDRAM
Rambus DRAM.

Read Cycle
A memory operation whereby data is output from a desired address location.

Redundancy
Additional circuitry (typically rows and columns) that replaces non-functional cells. The replacement is done by the manufacturer during wafer probe test by blowing fuses.

Refresh
Operation needed in DRAMs to regenerate information in the memory cells that leaks over the time.

ROM
Read Only Memory. The memory is programmed during fabrication of the device.

ROW
Rest Of the World (excludes Japan, North America, and Europe).

Sense Amplifier
Internal circuitry of the memory that recognizes the information stored in the memory cell and transforms it into a “1” or “0” logic.

SAM
Serial Access Memory.

Serial Access
Feature of a memory by which all the bits are entered or retrieved sequentially at a single input.

SDRAM
Synchronous DRAM. DRAM controlled by a clock.
Glossary of Terms

SIA
Semiconductor Industry Association.

SGRAM
Synchronous Graphic DRAM. The SGRAM adds special features on SDRAM to address video applications.

SIMM
Single In-Line Memory Module.

SRAM
Static RAM. A type of semiconductor memory in which a flip-flop stores the information. The information is stored as long as the power voltage is applied.

SSRAM
Synchronous SRAM.

Stack Capacitor
One method of reducing the cell size of a DRAM by stacking the capacitor over the bit line above the surface of the silicon.

Standby Current
Current consumed by the memory when de-selected by Chip Enable or Chip Select clocks.

Storage Capacitance
Ability for a node to store a charge. Used for DRAM cells that are composed of one access transistor plus a storage capacitance.

Substrate
The material on which a microelectronic device is built.

Subthreshold Current
MOS transistor channel leakage current that flows between source and drain when the transistor is off.

Supply Voltage
Power supply provided to the memory. Acronyms: V\text{CC} and V\text{DD}.

Synchronous
When outputs change states in time with a clock.
Technology
See Process.

TFT Cell
Thin Film Transistor Cell. The TFT cell is a type of SRAM cell that consists of a poly load acting as a PMOS transistor.

Three State Output
High Impedance state (see Hi-Z).

Threshold Voltage ($V_t$)
The voltage at which a transistor turns on or off.

Transistor
An active semiconductor device with three electrodes that is mainly used as a switch.

Trench Capacitor
One method of reducing the cell size of a DRAM by folding the capacitor vertically into the surface of the silicon in the form of a trench.

ULSI
(Ultra Large Scale Integration). IC containing 10 million or more transistors.

UMA
Unified Memory Architecture. PC architecture providing logic and graphic memory sharing for memory saving.

UV-EPROM
See EPROM.

VESA
Video Electronics Standard Architecture.

Video RAM
This device is also called Dual-Port DRAM. A VRAM has separate parallel and serial interfaces for video applications.

VLSI
Very Large Scale Integration. ICs that contain 100,000 or more transistors, but less than 10 million transistors.
Volatile Memory
Device that loses its content when powered off. DRAMs and SRAMs are volatile memory devices.

$V_t$
See Threshold Voltage.

Wafer
A thin disk of semiconductor material (usually silicon) on which many separate chips can be fabricated.

Wafer Sort
The electrical testing of each die on the wafer while still in wafer form.

WRAM
(Window DRAM). DRAM used for graphic applications.

Word-line
Also called row.

Write Cycle
A memory operation whereby data is written in a desired address location.

Yield
The yield is the ratio of the number of acceptable units to the maximum number possible.

4T Cell
SRAM cell made of four NMOS transistors plus two poly loads.

6T Cell
SRAM cell made of six transistors (four NMOS and two PMOS).