“Even if you’re on the right track, you’ll get run over if you just sit there.”
— Will Rogers

A very efficient design and manufacturing strategy has evolved in the past 50 years upon which virtually all electronic products are based. There may be significant differences in the outer form factors and other weighing factors of electronics-based products, but all such systems are based on integrated circuit chips, interconnected in a hierarchy of modules up to the complete system.

Though there is often more than one “right” way to design a system that results in a particular form factor and performance level, a well defined strategy has evolved over the years that standardizes many aspects of the technology to reduce manufacturing costs and time to market.

The various levels in this interconnection scheme are diagrammed in Figure 8-1. They consist of the following stages:

level 1: from the die, typically into a single chip package

level 1.5: from the die to a substrate that could be part of an MCM or wire bonded to a substrate as chip on board (COB) or flip chip attached to a substrate as direct chip attach (DCA)

level 2: from the package to the substrate, or MCM to the substrate

level 3: from the board to the backplane or from the daughter card to the motherboard

level 4: from the backplane to other backplanes in a cabinet

level 5: from one cabinet to others with cabling

Every electrical system can be broken up into these interconnect levels with a distinct interface between each. By standardizing on interfaces, there is tremendous flexibility to pick and choose the design within each level to arrive at the optimum cost-performance and time to market metrics. The infrastructure consists of the standards, a body of widely accepted practices, and multiple material suppliers and contract assemblers to enable the various interface choices.
THE CONVENTIONAL STRATEGY

A typical product creation cycle from concept to final product is diagrammed in Figure 8-2. How much of the complete path is supported within a single company is a measure of how vertically integrated it is. The partitioning of the packaging and interconnect levels into modules with clean, well defined interfaces between them is what has enabled non-vertically integrated companies to offer final products. This partitioning process also created a very large cottage electronics industry to support the details of each level independently.

The term “conventional” technology is defined by its availability in the open market. This is an indication of the presence of an infrastructure to support it. Figure 8-3 is a photograph of a typical, conventional assembly line for printed circuit boards.

The barriers to low-cost manufacturing and shorter time to market are minimized if a new product can be implemented using the conventional approach, which is summarized as:

- The system is designed with standard, semi-custom, or full custom chips.
- The chips are packaged in packages for through-hole or surface mount assembly, with or without heatsinks attached, and are delivered fully tested.
• The circuit boards are designed and fabricated with through-hole, buried, and/or blind vias using mechanical drilling, print, etch, and laminating methods.
• The various components are assembled with through-hole or surface mount pick and place assembly and wave solder or reflow.
• The system is cooled with air, using either convection or a central blower.
• The system is integrated using standard mechanical engineering practices.

If a system can be manufactured using these methods, the infrastructure is in place to deal with it. Partitioning has allowed companies to specialize in producing only chips, or only boards, or only packages, or software, or only assembly services. The tremendous infrastructure that is in place allows some “system houses” to concentrate on product design, integration, and marketing, as long as their products can take advantage of the established, conventional technologies.

These conventional approaches are constantly evolving and improving, with more sophisticated options becoming available in the open market. The driving forces on the introduction of new packaging choices are as much related to how they fit into the existing infrastructure, as to the
cost/performance they offer. Also, there is far less technical risk in moving along an evolutionary path of steady improvement than there is in jumping to a new, revolutionary path, even though the performance advantage may be great.

The Role Of The U.S. Packaging Industry

In general, it is the vertically integrated system houses, such as IBM, AT&T, Motorola, Rockwell, HP, and DEC, that have pursued and introduced new technologies, which then filter down and become established in the industry. Twenty years ago, surface mount technology was viewed as something special, done only in large system houses. Today, 65% of all package components are surface mounted and this percentage is increasing. Surface mount technology is fully integrated in the infrastructure of conventional technology.

Likewise, chip-on-board (COB) is a conventional technology, though not widely practiced. It is an essential feature of hybrid technology, and has been enabled on epoxy-glass substrates primarily because of “glob top” epoxy encapsulants. With these encapsulants, bare die mounted on circuit boards can be protected from the environment with a reliability level matching packaged die.
We are currently in the early stages of four new technologies, oriented toward enabling a higher packaging efficiency and hence denser designs running at higher speeds. All of these technologies result in a smaller footprint for the die on the substrate.

These four new technologies, discussed in detail in later chapters, are:

- Direct Chip Attach Flip Chip Assembly (DCA-FC)
- Ball Grid Array (BGA) packages
- Chip Scale Packages (CPS)
- MultiChip Modules (MCMs),

Each of these technologies had their start within large vertically integrated companies where the infrastructure was created and implemented for specialized applications. After the successful product introductions, the concept was adopted by the merchant semiconductor manufacturers. Champions and visionaries then began the process of creating a commercial infrastructure.

Some of the infrastructure in place for hybrids, a long time conventional technology, is being applied to MCMs, and much new infrastructure, not currently available, will have to be developed and proved to be viable.

The hurdle of introducing a new IC to non-vertically integrated customers is drastically reduced if it can be fit into a single-chip package for which assembly technologies are readily available and for which substrates can be fabricated. The trends in IC technology toward higher pin count, higher power dissipation, higher signal bandwidths, and higher sensitivity to noise are pushing the evolution of this conventional strategy, in order to handle the newest chips.

The packaging strategy that is most appropriate for a company to meet their product goals is based just as much on the technologies available in-house and outside, as it is the potential performance.

Adapting new technologies, especially in the U.S. is often a painful and slow process. This reluctance to change acts as a filtering process to increase the odds that those approaches that evolve to widespread use are well tested and offer significant cost-performance benefits. There are a number of reasons this process is slow:

1. The “chicken or the egg” problem. Vendors are reluctant to take a risk and invest in developing a new technology unless customers are demanding it. However, customers will not demand it until all the pieces are available and they are committing product designs to the new technology. This attitude leads to “development in response to crisis,” brought on, for
example, by products that cannot compete with other new technologies. This also puts the large, vertically integrated companies in the lead role in the development of new technologies. In a vertically integrated company, when a new infrastructure is required, all the pieces are developed in parallel, motivated by corporate commitment and edict.

2. In the U.S. there is a larger gap between the technologies available inside vertically integrated companies and what is available in the merchant market, in contrast with the Japanese electronics industry. In Japan, many of the vertically integrated companies are also large merchant vendors. This is only recently becoming the trend in the U.S. Many of the leading edge package and interconnect technologies from IBM, HP, AT&T, Motorola and DEC, are now being offered under license or on a contract basis. As an example, the same MCM technology that enabled IBM’s mainframes is available for anyone’s PC.

3. There is a reluctance for companies to take unnecessary technical risks. Therefore, in adopting a new technology, the hurdle is very high because the first application is usually extremely challenging. The new technology usually requires rapid implementation, rather than having had a chance to move up the learning curve gradually.

4. Manufacturing engineering is not given the cultural value that it deserves. There is a tendency in schools, and some companies, to view the hard part of a new product development to be the conceptual stage. Manufacturing is perceived to be as easy as “turning the crank.” In fact, it is manufacturing that usually requires far more effort, skill, and attention to detail than developing the concept, as shown in Figure 8-4.

5. The U.S. has been very slow to integrate science and engineering into manufacturing. Statistical Process Control (SPC) is still in its early stage of being integrated into production facilities. There is a common attitude in IC fabs that if a process is “working,” one should not change it, for fear that it then will not work.

6. The business and corporate management climate fosters attention to short-term profits, rather than encouraging investments in the future. The time to market for a new product based on a technology with an existing infrastructure to support it is 12-18 months. To introduce a new product based on a new technology may take 5 years, as with the substrate technology that DEC introduced in the VAX 9000.

7. All manufacturing that results in an efficient operation, consistently high-quality product, with well documented and understood processes takes a lot of work. There is a tendency to seek solutions that are superficial and “easy” in the short term, but do not contribute to moving up the learning curve for future growth.
These issues challenge the U.S. packaging industry. Unless they are addressed, U.S. electronics, with a few exceptions, will continue to lag further and further behind the technology available in the off-shore marketplace.

Even in just the last five years, there has been significant progress in the packaging, interconnect and assembly infrastructure. Some of this progress is attributed to the strengthening or initiation and success of industrial consortia, some privately created, some government sponsored, such as:

- SEMATECH (Semiconductor Manufacturing Technology Consortium Inc.)
- MCC (Microelectronic Computer Corp.)
- IPC (Institute for Packaging and Interconnect Technology)
- NEMI (National Electronics Manufacturing Initiative)
- ITRI (Industrial Technology Research Institute)
- Universal Instruments BGA and Flip Chip Consortia

One of the end results of these efforts has been the drafting of three technology roadmaps sponsored by the IPC, NEMI and the SIA.
SINGLE-CHIP PACKAGES

The first level of interconnect or packaging is the interface with the IC. From the IC’s perspective, the level one package must accomplish four tasks:

1. protect the die from the environment
2. transport heat from the die to the ambient
3. transport electrical power to the die
4. transport signals between the die and to the outside world

This is diagrammed in Figure 8-5.

To the rest of the system, the first level package has two critical functions. First is to provide a mechanical transformer from the pitch of the landing pads on a die to the pitch of the landing pads on a PWB. This later function defines the physical size of the package. The drive to handle more I/O off the die, without increasing the footprint of the package, is pushing the acceptance of finer pitch peripheral and finer pitch area arrays of connections, both for through-hole and surface mount assembly.
The other prime role for the first level package is to provide a clean and well defined interface between a chip supplier and an end user. A packaged chip can be fully tested in the same format as it will be used. It can be robustly shipped and easily handled at the receiving end by conventional assembly equipment. The drive for faster, smaller, cheaper, NOW, is pushing single-chip packages into form factors that are beginning to challenge these aspects of the traditional single-chip package.

Some examples of these packages are shown in Figure 8-6.

![Increasingly Complex Packages That Tax Conventional Assembly Technology](image)

**Figure 8-6. Increasingly Complex Packages That Tax Conventional Assembly Technology**

**Historical Perspective**

The first single-chip packages, in the early 1950’s, not surprisingly, looked a lot like miniature vacuum tubes. They were small hermetically sealed metal cans with a header base of feedthroughs having 2 to 10 small legs. The legs, or pins, were mounted into holes in a printed wiring board. These cans typically had only a maximum of 8-10 leads, in a circular pattern out the bottom, as shown in Figure 8-7. They were used to package single transistors which were the only types of chips then in use. Pin count was not a concern.

It was the introduction of Integrated Circuits, in the early 1960’s that created the need for higher pin count packages, and started the thirst for higher pin count, which has not been quenched even today.
A brief perspective on the evolution in complexity and pin count of integrated circuits is shown in Figure 8-8. In 1961, the first monolithic IC required 6 pins. In 1964, the Fairchild M-S Flip Flop required 11 pins. In 1966, the J-K flip flop required 16 pins. In 1967, a typical Arithmetic Logic Unit (ALU), required 36 pins. The IC quickly outgrew the ability of metal cans to accommodate leads.

The dual in-line package (DIP) was created to provide more pins than a metal can, while allowing through hole assembly in conventional circuit boards. The DIP has leads on two sides (hence the name) and dual rows of leads, in line. In 1995, 32% of all packages used, or 15 billion units were DIPs. This style package has recently evolved to include surface mount versions, but still with leads on only two sides.

In the early packages, the center-to-center spacing was 100mils, limited by the minimum pitch of conventionally drilled holes in circuit boards. The largest pin count practical in the early DIP was 64 pins. This package has a body size of over 3.2 inches long. Examples of DIPs are shown in Figure 8-9.

As IC pin count needs rose, the limits of the DIP were quickly reached. The pin grid array (PGA) was the next through hole package to be introduced, with pins on an area array pattern. Pin counts of even 132 were easily accommodated. This was typically accomplished by using an array of 14 x 14 pins, and removing the center 8 x 8 array. In 1995, over 200 million PGAs were assembled into products. Examples of PGAs are shown in Figure 8-10.

The transition to surface mounting of package leads to solder pads, rather than inserting pins into holes started in the mid 70’s. This has been viewed as a major advance to more densely pack components on boards and minimize the cost of the boards. Early surface mount packages were DIPs with their leads cut short and butt attached to the boards. Leads that bent under, or J leads, and leads that bent out, or gull wing, soon followed.
Packaging technology quickly evolved to the peripherally leaded package. The term “flat pack” was introduced in the 70’s to describe a new generation of packages designed to be mounted to the surface of the board, with leads on all four sides. In the 80’s, the term “chip carrier” was introduced. Chip carriers are typically square packages, leaded or leadless, with attach points around the periphery. Early surface mount packages tended to have a much smaller footprint than comparable pin count DIPs or PGAs. This was due to the tighter pitch possible, typically 50mil centers, and using all four sides. A comparison of a 40-pin DIP and a 40-pin chip carrier is shown in Figure 8-11.

The history of packages and the desire to satisfy ever higher pin count, from the can to the chip carrier is summarized in Figure 8-12. This trend continues today and into the future.
Evolutionary Advances in Conventional Packaging Technologies

Figure 8-9. Ceramic DIP Packages

Figure 8-10. A Variety of PGA Packages
MODERN TECHNOLOGY CHOICES FOR SINGLE-CHIP PACKAGES

There are today a myriad of single-chip packages to choose from, each with their own acronym, such as DIP, PGA, SOP, SOJ, TSOP, VTSOP, CC, PLCC, CPGA, BGA, TBGA, etc. Several of these types are shown in Figure 8-13. The habit for packaging engineers to create a new name and acronym for a slight variation on an existing package is pointed out by Scott Adams, shown in Figure 8-14.
However, all of these package types can be categorized into just three general classes, based on their lead form factor:

- **Dual In-line Packages: DIPs**, rectangular packages with two rows of leads on two sides of the package, can be through hole or SMT
- **Chip Carriers**: square packages, with leads on all four sides, strictly for SMT
- **Grid Arrays**: leads on an area array. For through hole, called PGA, for SMT, called LGA or BGA.

These three families are diagrammed in Figure 8-15.

Each package type or package style can be categorized by a lead pitch, a body size, the total number of pins, the package thickness, and special enhancements.
Board-Attach Footprints

The most important quality of a package is the number of external pins it can support. Each package style has a body size and footprint area which scales with pin count, when the package is pin limited rather than IC size limited. This is illustrated in Figure 8-16, for each of the three styles. When the driving force is the smallest size package for a required number of leads, the selection process is clear from this figure.

For most low pin count memory devices, because of their rectangular shape, a DIP is preferred. As pin count increases, the optimum style is a QFP. At about 80 pins, a 50mil center BGA offers a smaller footprint. At about 230 pins, a 100mil center PGA is more optimum over a QFP. For the highest pin counts, the BGA offers the most efficient package size.

As will be illustrated in later chapters, the grid array form factor is the most efficient style. There is a continuum in pitches in use from 100mil centers in a PGA to 8mil centers for a flip chip. As the pitch decreases, the assembly and substrate requirements (costs) increase, but the packaging efficiency increases. For lower pin counts, the DIP and QFP have an established place.
DIPs

DIPs are used almost exclusively for low pin count devices, typically less than 64 leads, for through hole or surface mount. By far the biggest usage is for memory packaging. The die are rectangular, with typically a 2:1 aspect ratio, closely matching the natural body size of most DIPs. When DIPs are used for surface mount, and the pitch is reduced to 25mils, the package style is often referred to as Small Outline Package (SOP), or Small Outline Integrated Circuit (SOIC). When the leads are bent under in a J lead, rather than straight out as in gull wing, the package style is termed SOJ. Some examples are shown in Figure 8-17.

The current driving force on DIPs, especially for memory packaging, is to reduce the thickness or profile of the package. This will enable portable applications where size and weight are important constraints. Figure 8-18 illustrates this trend in reduced thickness DIPs for memory packaging. As the package gets thinner, the name reflects this, as in Thin SOP, or TSOP, and Very Thin SOP or VT SOP.
Peripheral Leaded Packages

The peripheral leaded packages are exclusively designed for surface mount. The pitch has steadily been shrinking, as assembly capability advances. Years ago, 50mil centers were a challenge to assembly operations. In 1996, 25mil center lead pitch assembly was a standard process with 20mil centers ramping up. The advantage in going with finer pitch is in a smaller footprint on the board.

### Table: Peripheral Lead Packages

<table>
<thead>
<tr>
<th>Drawing</th>
<th>Nomenclature</th>
<th>Body Width</th>
<th>Lead Type</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="SO" /> 8-16 Pin</td>
<td>SO = Small Outline</td>
<td>156mil</td>
<td>Gull Wing 50mil</td>
</tr>
<tr>
<td><img src="image" alt="SOM" /> 8-16 Pin</td>
<td>SOM = Medium Outline</td>
<td>220mil</td>
<td></td>
</tr>
<tr>
<td><img src="image" alt="SOL" /> 16-32 Pin</td>
<td>SOL = &quot;Large&quot; Outline SOP = &quot;Small&quot; Outline Package</td>
<td>300mil*</td>
<td></td>
</tr>
<tr>
<td><img src="image" alt="SOJ" /> 16-40 Pin</td>
<td>SOJ or SOL-J = &quot;J&quot; - Lead Large Outline</td>
<td>300mil*</td>
<td>J- Lead 50mil</td>
</tr>
<tr>
<td><img src="image" alt="VSOP" /> 32-56 Pin</td>
<td>VSOP = Very Small Outline Package</td>
<td>300mil</td>
<td>Gull Wing 25mil</td>
</tr>
<tr>
<td><img src="image" alt="SSOP" /> 8-30 Pin</td>
<td>SSOP = Shrink Small Outline Package</td>
<td>208mil</td>
<td>Gull Wing 25mil</td>
</tr>
<tr>
<td><img src="image" alt="TSOP" /> 20-56 Pin</td>
<td>TSOP = Thin Small Outline Package</td>
<td>230mil to 550mil Including Leads</td>
<td>Gull Wing Type 1 19.7mil</td>
</tr>
</tbody>
</table>

* Up to 440mils

Source: Topline/ICE, "Roadmaps of Packaging Technology" 22489

Figure 8-17. SOIC Small Outline Integrated Circuit

Peripheral Leaded Packages

The peripheral leaded packages are exclusively designed for surface mount. The pitch has steadily been shrinking, as assembly capability advances. Years ago, 50mil centers were a challenge to assembly operations. In 1996, 25mil center lead pitch assembly was a standard process with 20mil centers ramping up. The advantage in going with finer pitch is in a smaller footprint on the board.
TAB (tape automated bonding) is a type of package with peripheral leads on a very fine pitch, typically 10-12mil centers. A close up of the outer leads of a TAB package with 0.14mm (5.6mils) pitch is shown in Figure 8-19. This illustrates the possible direction for very fine pitch leads. TAB has been used in volume production for the Sun Microsystems MicroSparc processors, the VAX 9000 and for Pentium processors for use in notebook applications. An example of a system using a TAB component is shown in Figure 8-20.
The advantage of ultra fine pitch surface mount is in the much smaller package footprint. For example, a 350 lead package in 25mil pitch chip carrier format takes up almost 5sq. inches of board real estate. With 10mil pitch, as in TAB, the area is closer to 1sq. inch, a dramatic reduction in size.

However, the smaller footprint with ultra fine pitch peripheral leads is more costly to assemble. As the leads decrease in pitch, the handling issues become more important. The leads on a 20mil center package are less than 10mils wide and very fragile. Problems of lead damage or lack of coplanarity add to the cost of handling and pick and place. Finer pitch also adds cost to the board. There is a bigger risk of solder bridging and shorting on the board. For TAB, each component is typically individually placed and reflowed with a hot bar, adding assembly time and capital equipment cost.

Chip carriers are offered in many types. When the leads are folded under in a J lead, and plastic molded, they are called PLCC (Plastic Leaded Chip Carriers). The generic chip carrier is termed QFP (quad flat pack). A molded plastic QFP is referred to as a Plastic QFP or PQFP. When the QFP is made from cofired ceramic, it is a CQFP. When it is made with a metal base, it is termed MQFP. Olin Interconnect has commercialized a version of a QFP with a metal clam shell top and bottom, with enhanced thermal and electrical performance. It is trade named the MQUAD. The MQUAD is diagrammed in Figure 8-21. Examples of other QFPs are shown in Figure 8-22.
Evolutionary Advances in Conventional Packaging Technologies

Figure 8-21. Cavity Down MQUAD® Package

Figure 8-22. Quad Flat Packs (QFP)
Surface mount chip carriers can be leaded or leadless. Leadless chip carriers are lower cost, easier to handle, and use a smaller assembly alley than leaded chip carriers. However, they have special reliability concerns. A potential failure mode of leadless surface mount components is solder joint cracking from thermal cycling due to the mismatch in the thermal coefficients of expansion (TCEs) of the chip carrier and substrate. For this reason, leadless chip carriers are mostly used with ceramic substrates, or for very small packages. Raychem’s Chip Carrier Mounting Device™ (CCMD) can be used to turn a leadless chip carrier into a leaded chip carrier, as shown in Figure 8-23. These compliant leads increase the thermal cycling lifetime for ceramic chip carriers on FR4 boards by a factor of 100.

Figure 8-23. Chip Carrier Mounting Device, Solder Pillars for Surface Mount of Leadless Packages

Not all assembly houses can handle fine-pitch, leaded chip carriers of 25mil pitch. To convert fine pitch surface mount packages for through-hole assembly, surface mount to through-hole transformers are available, as shown in Figure 8-24.

Grid Array Packages

The most efficient scheme for increasing the I/O density of a package is to place the I/O in an area array. The first area array packages were designed for through hole insertion. These were pin grid area (PGA) packages. The typical lead pitch is 100mils. The use of pin grid array packages can tax the layer count and feature size of the circuit board.
If there are 18 rows of pins, for example in a 324 pin, full array, 9 tracks of traces will be needed to get a signal trace from the inside row to the outer routing channels. If the board is designed for one track technology between holes, 9 signal layers will be required just to route the pin escapes. This is one disadvantage to using PGAs for high pin count devices, it can sometimes require a more costly board.

One solution is to use a partially filled array. For example, using a 22 x 22 pin array results in 484 pins. If the center 12 rows are removed, the total package pin count is 340 and the maximum pin depth is only 6 pins. This trades off a larger package, 4.8in², compared with 3.4in², but may result in a lower cost system, due to a reduced number of layers in the final board.

PGA packages with over 500 pins have been fabricated. Figure 8-25 is an example of a 500 pin PGA that is over 2.7 inches on a side or over 7.5in². This is a very large package. The package size can be reduced by adding an additional pin in the interstitials. Addition of this interstitial pin effectively doubles the I/O density. The effective pitch is roughly 70mils. Figure 8-26 is an example of a pin grid array package with interstitial pins.
Figure 8-25. 500-Pin Cavity Down PGA

Figure 8-26. Cavity Down PGA With Interstitial Pins on 100mil Centers
Figure 8-27 compares the package footprint area of a 0.025 inch pitch QFP and a 0.1 inch pitch PGA and interstitial PGA. For pin counts greater than about 230, a 0.1 inch pitch PGA offers a smaller footprint. For pin counts greater than 100, an interstitial PGA offers a smaller footprint than a QFP. This is why there are few applications for QFPs of greater than 208 pins. Interstitial PGAs are popular for the higher pin count PGAs. For example, the Pentium is packaged in a 324 pin interstitial PGA.

It is difficult to use a PGA with pin pitch finer than an interstitial PGA, assembled as a through hole component. This taxes the circuit board too much, and would require a very small pin, subject to easy misalignment.

To get higher pin I/O densities, the surface mount grid array is the only other practical approach. Surface mount pin grid arrays with 50mil centers are in use for high end applications in Japan. An example of a surface mount 50mil center PGA is shown in Figure 8-28. Even finer pitch grid arrays have been introduced, but based on surface pads or bumps. An example of a 25mil center pad array is shown in Figure 8-29.

The concept of surface mount area array packages, offering a high density I/O package, has caught on and driven the introduction of the ball grid array (BGA) explosion. An example of a BGA package is shown in Figure 8-30. The primary advantage of a BGA package over a PGA is a tighter pitch of the I/O and, being a surface mount package, does not required large through-hole vias in the circuit board. The board can be less complex.
Evolutionary Advances in Conventional Packaging Technologies

Figure 8-28. 1,000 Lead Surface Mount Pin Grid Array on 50mil Centers for Surface Mount

Figure 8-29. Cavity Up Pad Grid Array Package on 25mil Centers
Figure 8-31 compares the footprint size of the QFP, PGA and BGA package footprint areas. It is clear that 50mil center area array of connections results in a much smaller footprint package. The introduction of area array interconnection moves packaging efficiency onto a new evolutionary track of much more efficient packaging density. It offers a practical footprint to achieve I/O counts into the 600 and above range. Even a 700 pin BGA has a smaller footprint than a conventional 208 PQFP. BGAs are discussed in more detail in a later chapter.

As the pin count of ICs has increased there has been a natural evolution that roadmap package options have taken. This is illustrated in Figure 8-32.

ENHANCED PACKAGES

Leadframe Versus Circuit Board

The manufacturing path for DIPs and peripheral leaded chip carriers has traditionally been by stamping a leadframe, performing a die attach and wirebond to the leadframe, and transfer molding the package body around the chip. This is a very efficient, high yielding and low cost assembly process. Figure 8-33 illustrates this process flow.
Evolutionary Advances in Conventional Packaging Technologies

Figure 8-31. Package Footprint for High Pin Count Packages

Figure 8-32. Evolution of Electronic Packaging

Source: ICE, "Roadmaps of Packaging Technology"
An alternative process is to use an interconnect substrate as the mechanical transformer from the die to the leads. Both cofired ceramic and printed circuit board substrates are commonly used. These substrates have been used to fabricate QFPs, PGAs and BGAs. An example of a QFP leadframe fabricated from an FR4 substrate is shown in Figure 8-34. If this package were mounted on a copper block this plastic package would offer better thermal performance than the best ceramic packages.

The advantage of using a substrate is the ability to provide enhanced electrical and thermal performance, while keeping the costs reasonable. The only way to implement a grid array package is by using a substrate.

Figure 8-33. Transfer Molding Procedure
The term plastic package refers to either a plastic molded package or a printed circuit board substrate package, typically FR4 or BT resin based. Low cost plastic packages can be single sided, with basically just the fan out traces on one side. Double sided boards can be used with the chip on one side and the pins or solder balls on the other side. Electrical performance can be enhanced by adding power and ground planes and decoupling capacitors on the package. For example, a PQFP package with an internal lead frame, may have a lead inductance of 10nH. When a 4 layer substrate with an internal ground plane is used, the ground inductance can be as low as 3nH.

By using standard circuit board technology, plastic packages can ride the price and feature curve of the circuit board industry, taking advantage of cost and performance advances. The substrate technology used to fabricate plastic packages is described in a later chapter.

### Thermally Enhanced Packages

Virtually all single-chip packages are designed for air cooling, either free convection or forced air. As the power handling capability of a package increases, various features, each costing more, are implemented:

- Cavity up (typical)
- Cavity down
- Thick planes in the package substrate
- Internal heat spreader: copper tungsten, copper, alumina or aluminum nitride
- Heatsink attached
- Thick power and ground planes in the motherboard substrate
The thermal path from the base of the die to the case is typically lower than the thermal path from the top of the die. The wirebonds off the top of the die create a natural standoff preventing close thermal contact. A cavity down orientation allows the back of the package to be available for heatsink attach or coupling to the air and provides a lower thermal resistance for the package.

Increasing the surface area for heat to flow also decreases the thermal resistance. A thick slab of high thermal conductivity material, directly underneath the die, will spread the heat to a larger area and decrease the thermal resistance of the package.

Aluminum nitride provides an electrically insulating, but thermally conductive, chip-attach substrate. An example of a quad flat pack with an aluminum-nitride base is shown in Figure 8-35. The thermal performance of a QFP with an aluminum nitride base, compared with conventional materials is shown in Figure 8-36. The thermal resistance can be decreased to 50% of a conventional ceramic QFP and almost 35% of a plastic QFP. Aluminum, copper and copper-tungsten bases are also commonly used heat spreaders.

![Quad Flat Pack With Aluminum-Nitride Substrate](source: Narumi/ICE, “Roadmaps of Packaging Technology”)

In packages with a laminated substrate, such as FR4, polyimide or BT, the use of thick power and ground planes acts as a thermal spreader. Internal planes can more than double the power handling ability of a package.

For the lowest thermal resistance, all materials in the thermal path should be kept either very thin or of high thermal conductivity. New die attach materials, loaded with fine ceramic powders can have thermal conductivities higher by a factor of 5 to 10 over the unfilled resin.
It is often erroneously said that plastic packages can’t handle much power. In fact, with an embedded heat spreader, the power handling of a plastic package can be excellent. The MCAIII gate array, at 35 watts, is packaged in a plastic PGA. A cross section of a PGA with heatsink is shown in Figure 8-37.

With the use of a heat spreader and thermally conductive epoxy, the greatest source of thermal resistance is in the interface to the air. This is why the nature of the heatsink plays such an important role in determining the power handling ability of a package.

For example, with the heatsink used in the MCAIII, 1.75 inches on a side, the case-to-ambient thermal resistance is about 2°C/W, at 4 cubic feet per minute air flow rate. If the maximum temperature rise allowed is 70°C above ambient, then a total power dissipation of 35 watts could be handled. This is about the maximum power dissipation of this chip.

Over the 3in² of heatsink area, the power density extraction of this heatsink is roughly 12W/in². By comparison, the pinned heatsink used in the VAX 9000 module has a power extraction ability of up to 18W/in². The relatively large air flow of 31ft³/min is required to reach these levels.

Figure 8-36. Plastic, Ceramic and Aluminum Nitride QFP160 Pin Thermal Resistance
Electrically Enhanced Packages

As pointed out in Chapter 7, the electrical performance of a package is improved when:

- Leads are kept short.
- Low dielectric constant insulators and high conductivity conductors are used.
- Ground reference planes are used and controlled impedance traces of at least 50ohms.
- Power planes are used with on-board decoupling capacitors.
- Chip bonding lengths are kept short.

Each of these features means added cost for the package. The lowest cost packages are typically single conductor layer and provide just a geometrical fanout and hermetic protection for ceramic versions. However, they often are not rated for operation with clock frequencies above about 100MHz, or rise times shorter than 1nsec.

PGAs made with FR4, BT or polyimide-glass printed wiring board material are good examples of implementations of features for higher performance, balanced with acceptable cost. These materials can provide power and ground planes, on-board decoupling capacitors, controlled impedance traces and low dielectric constant. By customizing the inner bonding shelf, and using multiple shelves, the wirebonds can be kept short-less than 50mils. An example of an FR4 PCB based PGA is shown in Figure 8-38.
Traditional cofired packages suffer from a number of electrical deficiencies, especially at higher pin counts. The dielectric constant is typically 10. The trace widths and dielectric thickness typically offer only a 30 to 40ohm characteristic impedance, which loads down the drivers. Usually, the trace width increases toward the periphery, so the characteristic impedance is not constant. To gold-plate the inner bonding shelf and the pads for pin attach, tie bars to every trace are sometimes brought out to the periphery. These are all stubs. The stubs are eliminated with the “through pin plating process”. Even given these deficiencies, multilayer cofired ceramic packages are frequently used, even for GaAs devices. An example is shown in Figure 8-39.

Figure 8-38. FR4-Based PGA With Integrated Heatsink

Figure 8-39. GaAs 30K-Gate Array
Environmental Reliability

Water is as close as any liquid to being a universal solvent and reagent. The ideal conditions for corrosion are: having dissimilar metals, adjacent to each other, in a moist, hot environment with bias applied. Unfortunately, this is exactly what the surface of an exposed die in a hot humid climate sees. Under conditions of temperature, humidity, and bias (THB), the lifetime of a device can be as short as days, unless it is protected from the environment.

One sure way of providing protection is with the use of a hermetic package. The die is completely enclosed in a seal, such as a ceramic glass or metal, that is impermeable to moisture (the difference in permeability between an epoxy and a sealing glass is six orders of magnitude). Insulated feedthroughs allow power, ground, and signals to be transported through the seal and various materials on the inside allow heat to transfer from the die to the inside case and eventually to the outside. Examples of metal packages with glass feedthroughs and all-ceramic packages are shown in Figures 8-40 and 8-41, respectively.

![Figure 8-40. 160K-Byte Memory Module Packaged in Hermetic Metal Can With Kovar-Glass Feed Throughs](source: Mosaic Systems/ICE, “Roadmaps of Packaging Technology"

With hermeticity comes a heavier package, which is a more expensive component and more expensive assembly. In addition, making a hermetic package that is reliable over the long-term requires the seal to be made with great attention. Contamination of surfaces and sealing materials, hairline cracks in the seals, or marginal sealing processes will result in a reliability time bomb. The larger the inner cavity that is to be sealed, the greater the risk of a faulty seal.
From a risk perspective, the hermeticity of a hermetic package can be tested after sealing in a non-destructive way, but the reliability of a non-hermetic package cannot. Two tests are commonly used to evaluate the quality of a hermetic seal: a gross leak test using fluorinert bubbling, and a fine leak test, using helium.

In the bubble test, the package is first bombed in a low boiling point fluorocarbon fluid. If there is a leak, the fluid will partially fill the cavity. It is then immediately dumped into a pot of hot fluorinert. A gross leak will be a source of bubbles, visible as a stream of bubbles in the tank.

In a helium leak test, the packages are conditioned in a high-pressure helium environment and then exposed to a helium leak detector. A small leak will allow helium to penetrate the package. When the helium slowly leaks out, it can be detected.

If assembly procedures are used that ensure the residual moisture level inside a hermetically sealed package is low enough (5,000ppm recommended by mil spec), and the lid does not leak, an ultra-reliable package will result. For liquid water to condense in a package and cause corrosion, there must be at least 6,000ppm of water in the cavity. This is the water concentration for a dew point of 0°C. If there is a lower residual water vapor than this, condensation won’t occur until less than 0°C, and the water vapor will condense as ice, which does not promote corrosion. 5,000ppm allows a margin.
Usually, the risk is lower with a hermetic package because of adequate test procedures and the extensive track record of ceramic packages, and is viewed by some companies to be worth the added cost.

Attention to detail and following the correct procedure is important for all types of packages to minimize the risk of experiencing a reliability problem.

Motivated by the vision of lower costs and more versatile assembly methods, non-hermetic packages account for over 85 percent of all packages fabricated. New “glob top” encapsulant materials have made chip-on-board feasible for low-cost applications such as smart cards, watches, calculators, and small computers. Even the high-performance end is moving toward non-hermetic packages, especially the PWB based PGAs and BGAs. The military envisions all MCMs in the future will be non-hermetic.

Non-hermetic packages can be made as reliable as hermetic packages if attention is paid to detail. Environmental protection comes from a three-tiered strategy:

1. On-chip passivation, usually SiO₂ or Si₃N₄
2. Die surfaces cleaned of ionic residue and contamination
3. Die encapsulation by an ultra-clean silicone, epoxy, or polyimide

Military organizations such as Rome Air Development Center (RADC) and DARPA have recently been advocating RWOH: Reliability WithOut Hermeticity. MCC (Microelectronics and Computer Technology Corp.) has been awarded a contract to complete a large-scale study of the failure mechanisms and material properties of encapsulants.

The IEEE has created a task force to review and make recommendations to the industry on the use of silicone gels for encapsulation. The Gel Task Force, chaired by Jack Balde and C.P. Wong, has released a report. The initial findings indicate that devices encapsulated by silicones can be just as reliable as hermetically packaged devices. Not only do the materials have to be qualified, but the process as well. Attention must be paid to the cleanliness of the die and gels, and the curing step must result in good adhesion to all protected surfaces, leaving no voids in contact with metalization.

The choice of a hermetic package is often based on two criteria, perceived value and the degree of the risk. For a chip vendor that is trying to get as high a price for its proprietary chip as possible, selling it in a gold-plated, heavy ceramic package that is known to be ultra-reliable makes it easier to command a much higher price than if it were in a plastic package. This is often how a pricing structure is created, the slower parts and lower priced parts are in plastic packages and the fastest parts are in expensive-looking ceramic packages, which can demand a much higher price. The leading edge microprocessors are usually offered first in hermetic packages because they will be priced high. The market does not expect a plastic packaged chip to be priced high.
With clock speeds in the 200MHz range, and price a major driving force for microprocessors, plastic packages are becoming the package of choice. In our new era of high performance and low cost, ceramic versions don’t meet the performance requirements, and plastic is cheaper. Intel has recently announced it will phase out the use of ceramic packages in favor of PCB based plastic packages.

COSTS

Numerous reports have been published comparing the costs of various packages. These should be used only as rough guides. Actual prices of packages are determined more by market forces such as the following, than by actual manufacturing costs:

- The required unit volume of each type of package
- The long-term business relationship between the vendor and customer
- The market expectations for the price
- Competition among multiple suppliers
- Competition from alternative packaging choices

Quoted package cost is traditionally on a pin count basis. For single layer, high pin count packages, the typical cost is $0.005 to $0.0075 per pin. For multilayer PGA and BGA packages, the cost is roughly $0.02-0.05/pin. For high pin count BGAs, the market expects the cost to be $0.04-0.07/pin in high volume. Ceramic package costs are typically 2-4x the cost of plastic versions, though pricing pressures from lower cost PPGA and PBGA packages are driving the ceramic prices lower.