Surface mount devices are typically held onto the substrate by solder. With a different TCE than the substrates, there will be mechanical stresses applied to the solder joints as the ambient temperature changes. This cycling stress is a potential reliability time bomb. To minimize the problem, compliant leads can be used in the package, as previously discussed, and substrates can be designed with TCEs that more closely match those of the packages.

In some cases, substrates facilitate the removal of heat, however, they must maintain their function in adverse environmental conditions and be manufactured and assembled at reasonable cost.

As pointed out in the last two chapters, the trend toward higher functional density means that there will be more pads per in^2 on the surface of the interconnect substrate. These pads must be interconnected through routing layers. This trend of increasing pad density is shown in Figure 11-2. And, at the same time, the cost for these substrates must be driven lower and lower. Higher pad density and lower cost are the principle driving forces on the evolutionary advances of substrate technologies.

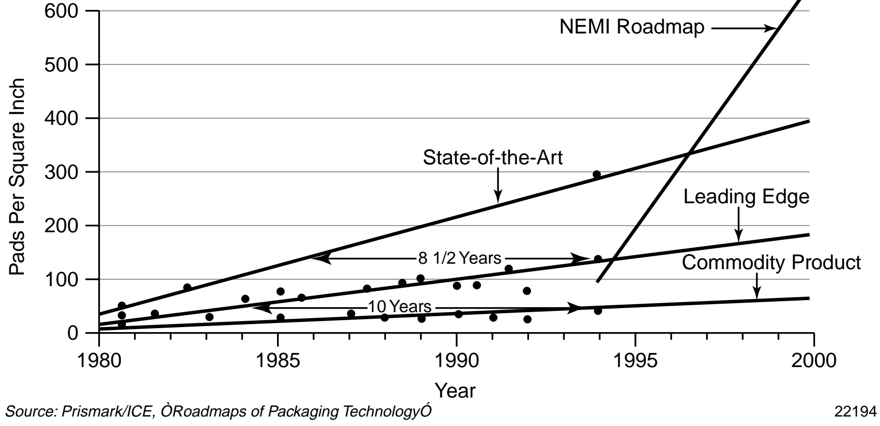


Figure 11-2. Surface Pad Density Over Time

SUBSTRATE APPLICATIONS

Though substrates are popularly considered to be used as just circuit boards, their applications span absolutely every level in the interconnect hierarchy. Each of the four interconnect substrate technologies listed above can used to fabricate:

- single chip packages
- multichip modules
- daughter cards
- specialized cards
- motherboards
- backplanes

PRINTED WIRING BOARD TECHNOLOGY

Basic Process: Patterning, Laminating, Drilling, And Plating

The basic fabrication process for conventional printed wiring boards is outlined in Figure 11-3. The starting place is an epoxy-glass weave core laminated with copper foil on both sides. The thickness of copper is described by its weight per square foot. One ounce of copper per square foot has a thickness of approximately 30 microns. Half-ounce copper foil has a thickness of 15 microns. Typically, 5mil wide or narrower lines are fabricated with half-ounce copper.

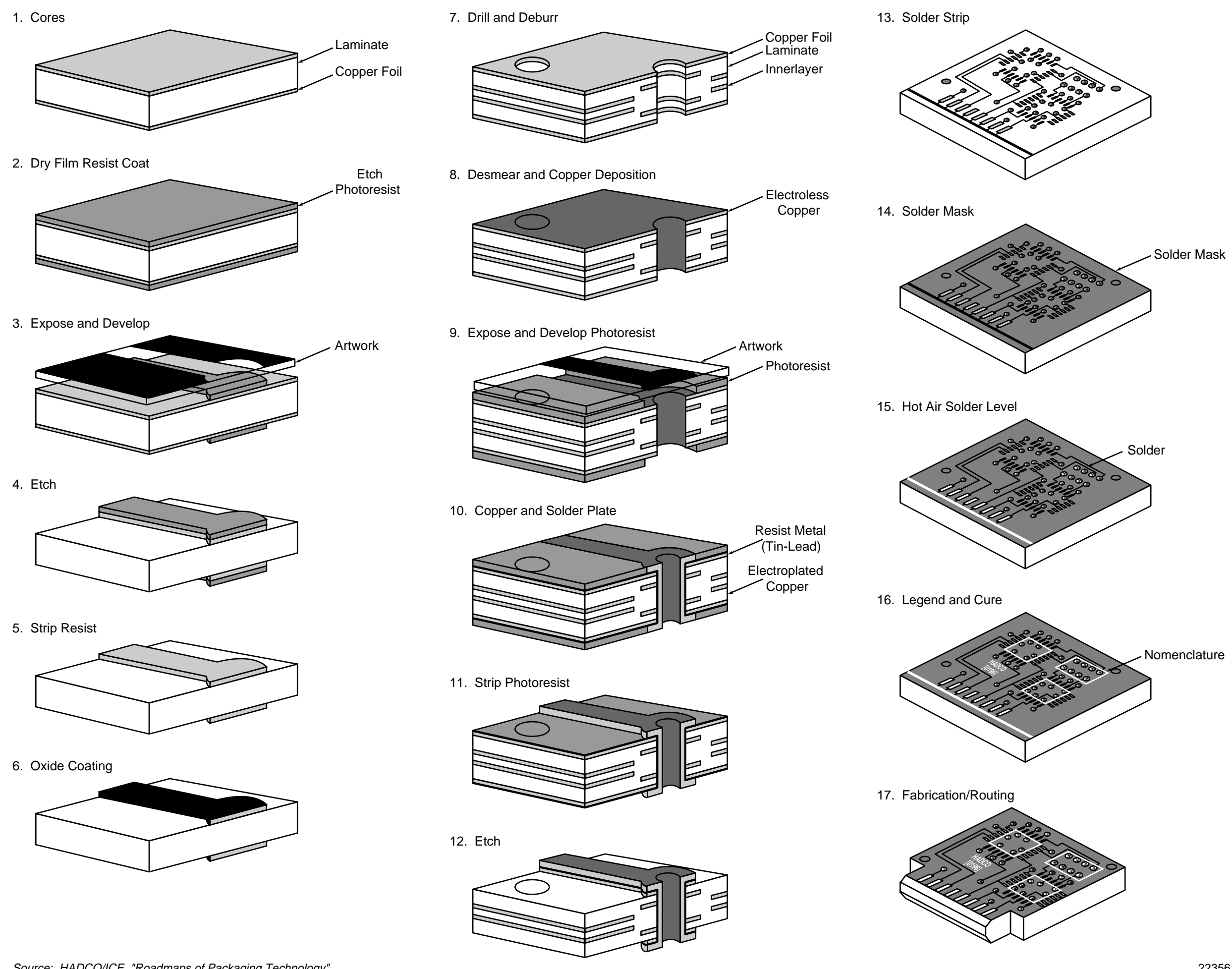


Figure 11-3. How to Build a Circuit Board

Power and ground layers, which must sometimes support very large currents, are typically thicker than one ounce per square foot. A single ECL chip may need 10 amps of current. The Pentium Pro, at 25 watts, and running at 3.3V, requires 7.5 amps. With a number of such devices on a board, the power and ground planes must be very low resistance. For example, in the NEC SX series super computers, the power and ground planes are 7 ounce copper per square foot, or more than 8mils thick.

A typical computer motherboard with interface chips and memory will dissipate on the order of 100 watts. At roughly 4V on the average for all the components, this is 25 amps of current that must flow in the power and ground planes of the board.

Dry film photoresist is typically laminated on both sides of the copper clad board, imaged and developed, leaving exposed copper, which is then etched off. Multiple layers are fabricated in parallel operations. All the layers needed for the design are laminated together with a sheet of partially cured epoxy glass, called "B stage," between them. These stacks are laminated under high pressure and temperature and the epoxy is cured, effectively gluing the layers together.

Holes are mechanically drilled through the stack exposing the edges of inner layers of copper traces in the inside wall of the holes. An example of the ultrafine drill bits used to drill holes as small as 6mil diameter is shown in Figure 11-4. These holes are then plated with copper in an electroless process, thereby electrically connecting multiple layers. The holes are then called "plated through-holes," PTHs. Figure 11-5 is an example of a cross section of a PTH.

Source: UNISYS/ICE, "Roadmaps of Packaging Technology" 22270

Figure 11-4. Various Drill Bit Diameters

0.15mm Hole Diameter
1.2mm Thick Panel

Source: Electrochemicals/
ICE, "Roadmaps of Packaging Technology" 22174

Figure 11-5. Mechanically Drilled Through Hole in FR-4

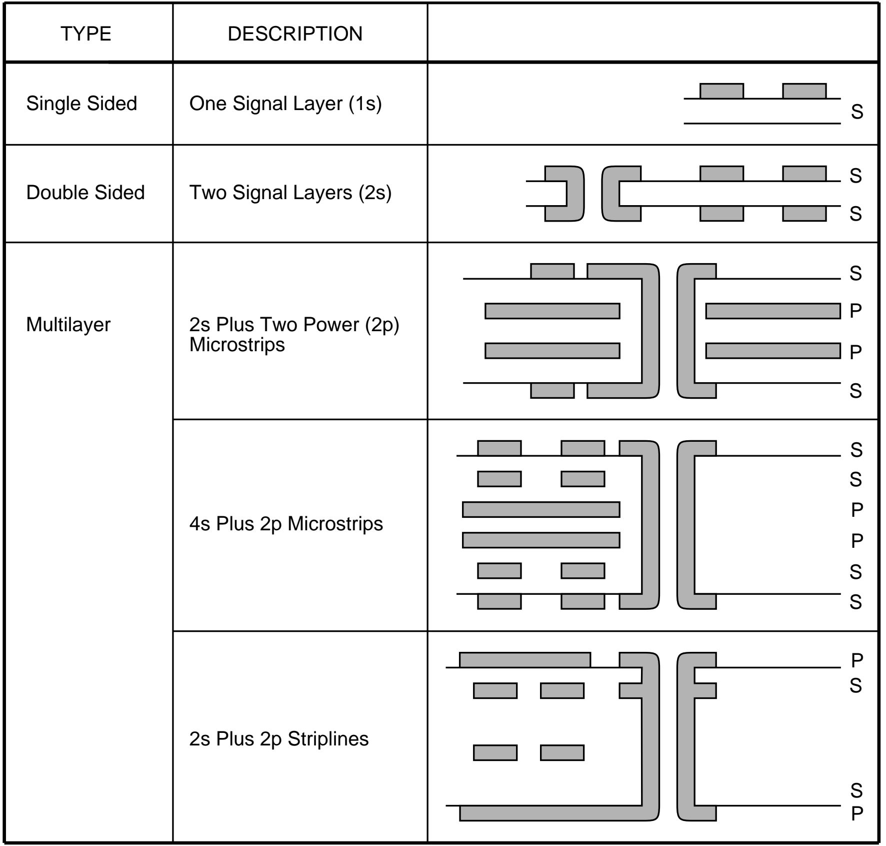
As a final step, the surfaces of the boards may be gold- or tin-plated or screen printed with solder mask or decals. In some cases, an organic coating is applied to the surface to prevent oxidation of the copper and allow good solder wetting.

Boards are typically fabricated in panels on the order of 36 to 48 inches on a side. Panels are built using several small boards, which are then cut or punched out after the panel is fabricated.

The basic features that characterize a printed circuit board are:

1. Number of layers
2. Linewidth of traces
3. Pitch of the vias
4. Pitch of the lines
5. Number of lines that can be routed between via holes, on a single layer

At the low-cost end, there are three common stack-up configurations consisting of two layers, four layers, and six layers, diagrammed in Figure 11-6. When more than six signal layers are required, more complicated stacks are used.



TYPE	DESCRIPTION	
Single Sided	One Signal Layer (1s)	S
Double Sided	Two Signal Layers (2s)	S S
Multilayer	2s Plus Two Power (2p) Microstrips	S P P S
	4s Plus 2p Microstrips	S S P P S S
	2s Plus 2p Striplines	P S S P

Source: Microelectronics Packaging Handbook, Tummala/ICE, "Roadmaps of Packaging Technology" 15844A

Figure 11-6. Printed Wiring Board Structure

Technology Capability And Limits

There is a wide spectrum of feature sizes and capabilities being implemented in the industry, all depending on the interconnect density required, turnaround time, and price. All shops will process 8mil lines and spaces, and most will process 6mil lines and spaces. The high-performance merchant shops can accomplish 5mil lines and spaces with up to 10 layers as standard processes and down to 3mils on special designs.

Of course, the specifications of the features that can currently be fabricated are a moving target. Figure 11-7 illustrates the historical trends in linewidths and Figure 11-8 illustrates historical trends in hole sizes.

The highest performance end boards are used by mainframe computers and fabricated in captive shops, such as Unisys. A typical board, as shown in Figure 11-9, is 50 layers, half of which are signal layers with 4mil lines on 30mil centers. This is over 700 inches of trace per square inch of board area. With a board dimension of 22 inches x 17 inches, there are over four miles of interconnect trace per board!

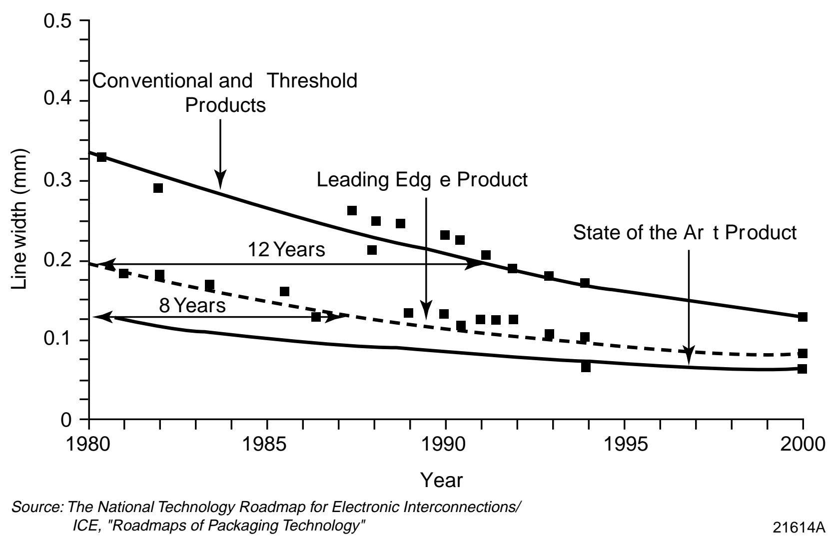


Figure 11-7. Roadmap for PCB Linewidth Reduction Over Time

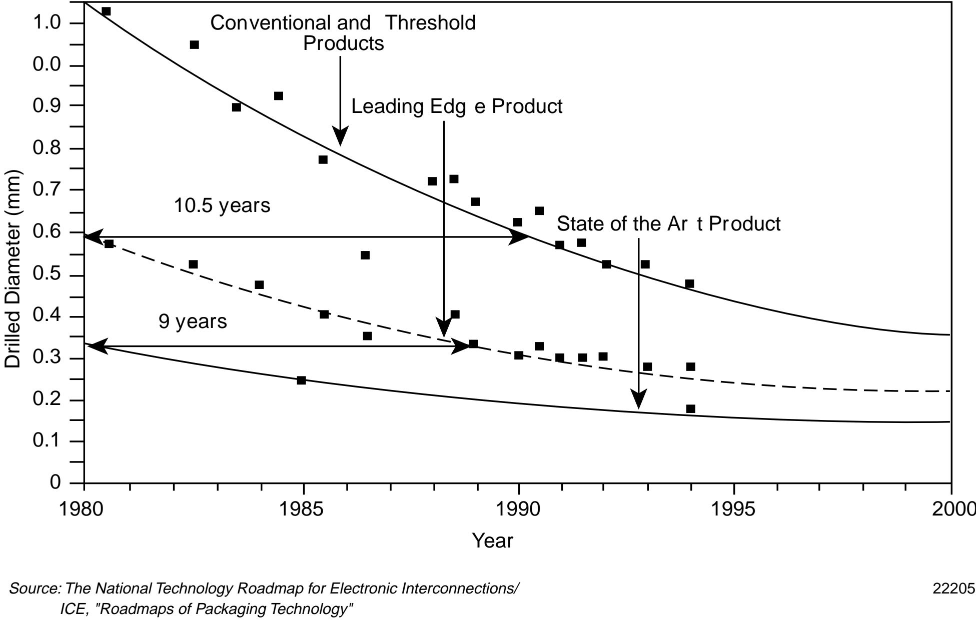


Figure 11-8. Hole-Size Reduction Roadmap

Boards such as this, which are based on extending the traditional PWB technology of mechanically drilling holes, high-temperature and pressure laminated epoxy-glass layers, and subtractive etching of laminated copper foil, are pushing the limits of this technology. To fabricate these boards with a yield greater than zero requires the test, inspection, and repair of each layer before it is laminated. It is estimated these boards cost $100/in^2 to manufacture, and the cost increases radically for each incremental increase in interconnect density. A factor of two increase in interconnect density cannot be manufactured cost-effectively with this technology.

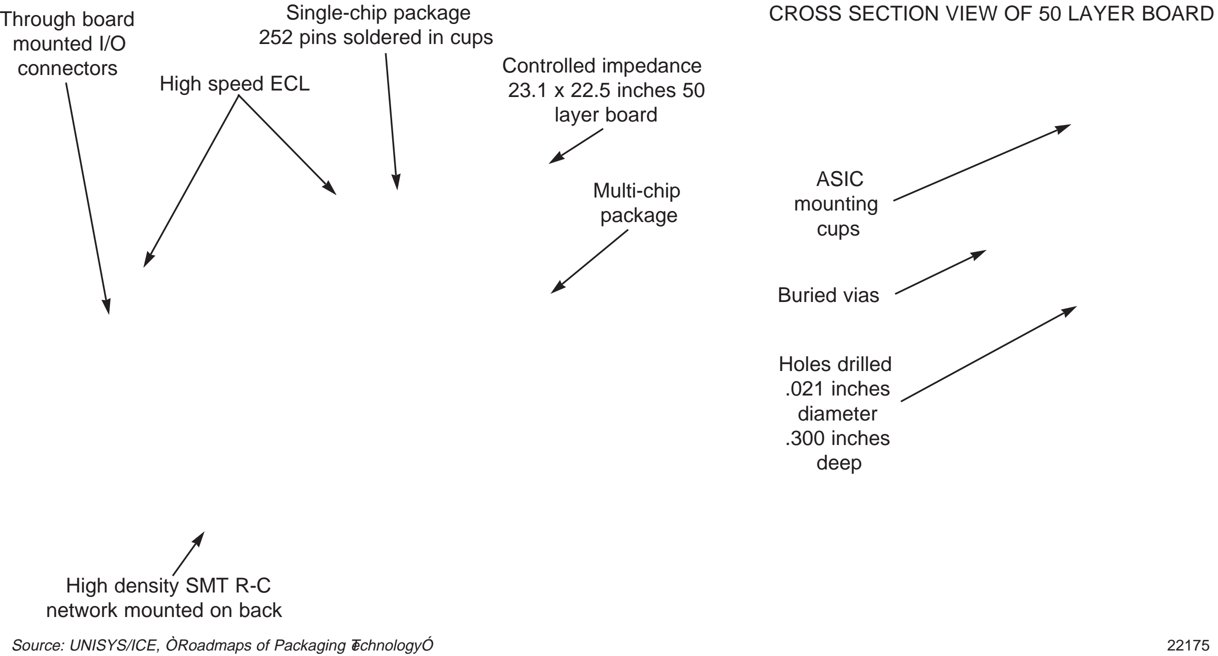


Figure 11-9. 50 Layer Board

This is why packaging strategies based on MCMs are being used for all the high-end systems. IBM has pioneered the approach of off-loading most of the interconnect to high-density modules that use a technology with higher interconnect capability than drilled through-hole printed circuit board technology. The PWB motherboard that the high-density modules plug into is used to distribute power and ground, and provides some signal interconnect between modules. The motherboard in the IBM3081, for example, uses an 18-layer board to interconnect the TCM units. DEC has adopted the same strategy in the VAX 9000. Multi-chip modules using thin-film multilayer technology, containing most of the signal interconnect, are mounted to 20-layer printed circuit boards.

In the NEC SX series computers, single-chip packages are mounted on a high-density substrate composed of multilayer cofired ceramic with multilayer thin-film interconnect. The Fujitsu VP2000 uses multilayer glass-ceramic substrates upon which single-chip packages are mounted. The PWB motherboard is used primarily for power and ground distribution and minimal signal interconnect because it is not cost effective to manufacture a printed circuit board that performs all the interconnect functions.

Pricing

Printed wiring boards are the mainstay substrate technology for all electronic systems. For low end and consumer products, the need for low costs drives the selection of board technology and stack up configurations. The emphasis is on low layer count, typically 2 to 6 layers. The prices for boards will vary considerably from supplier to supplier. A study completed by PC Fabrication magazine illustrates the wide variation in prices for the same board.

Specifications were supplied to a number of board vendors for 4 different boards, a 2 layer, a 4 layer, a 6 layer and an 8 layer board. The detailed specs, for a 8 mil line and space board, each, 5.2 inches x 11.2 inches, are shown in Figure 11-10. The quoted prices for boards vary depending on the quantity and delivery time. For example, a two layer board, with 5 day turn, is priced at $103 per board, but for volume production, the price is only $15/board.

Board size:	X: 5.20", Y: 11.20"
Board type:	Multilayer
Layers (thickness):	2 (0.062")/4 (0.062")/ 6 (0.062")/8 (0.070")
Finish:	SMOBC
Plating:	0.0015-mil minimum
Substrate material:	FR-4
Silkscreen ?:	Y—comp side, white
Gold tab ?:	N
Solder mask ?:	Y—both side(s), LPISM
Surface-mount parts ?:	Y
Min. SMD lead space:	0.020"
Min. circuit width:	0.008"/0.008" lines and spaces
Fabrication spec:	UL approved
Drilled holes	Total: 2000 Smallest: 0.0180"
Tool changes:	8 hole sizes
Electrical test:	Y
Test voltage:	40 volts
Verify net to schematic ?:	N
Networks on this part:	135
Shipping method:	FOB, your plant

Source: Printed Circuit Fab Magazine/ICE, "Roadmaps of Packaging Technology" 22206

Figure 11-10. Sample Board Specifications Sent Out to Suppliers for Quote

The quoted prices are summarized in Figure 11-11, and selectively plotted in Figure 11-12. The spread in prices for each of the boards is indicative of the pricing strategies used by the PCB industry. For example, the spread in prices across the selected vendors, for a volume production rate of 5,000 units/month varied by almost a factor or 4 between the high and low price.

Quantity	Delivery	2-Layer Avg.	2-Layer High	2-Layer Low	4-Layer Avg.	4-Layer High	4-Layer Low	6-Layer Avg.	6-Layer High	6-Layer Low	8-Layer Avg.	8-Layer High	8-Layer Low
10	5 days	103.43	189.00	43.35	184.29	350.00	120.00	232.00	450.00	140.00	305.44	550.00	190.00
10	10 days	84.61	154.00	33.35	113.75	190.00	80.00	142.14	230.00	106.50	169.35	210.00	140.00
50	3 weeks	30.72	72.00	17.16	51.86	112.00	24.00	60.37	125.00	28.80	65.11	110.00	35.28
100	4 weeks	21.41	43.00	12.00	38.58	94.00	16.00	47.50	118.00	25.00	49.43	92.00	32.00
500	6 weeks	16.76	42.00	11.00	26.22	62.00	15.00	32.52	73.00	23.50	42.82	89.00	30.25
5000	Monthly	15.35	40.00	10.00	24.70	60.00	14.25	30.00	67.00	21.00	40.29	82.00	29.15

Source: Printed Circuit Fabrication/ICE, "Roadmaps of Packaging Technology" 22207

Figure 11-11. Quoted Average, High and Low Price/Board by Quantity/Delivery Schedule

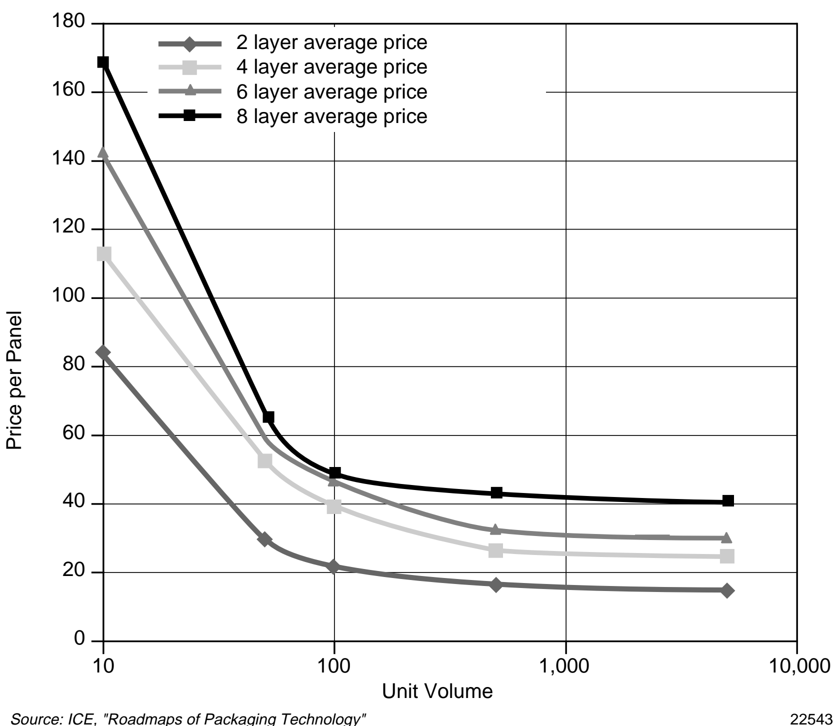


Figure 11-12. Average Price Quoted for PCBs

In this case study the board area was 58 in^2. For a six layer board, for example, the average price of \$30 corresponds to about \$0.5/in^2. This matches the rough rule of thumb of \$0.1/in^2 per layer of board. However, the prices ranged from \$0.36/in^2 to \$1.15/in^2.

Based on this analysis, it is dangerous to generalize about the price of PCB substrates. Although it may be possible to look at the trends based on the manufacturing cost, it is important to recognize that the price depends strongly on the relationship between the supplier and the vendor.

There is a growing trend to change the traditional vendor-customer relationship into a partnership. This is illustrated in Figure 11-13. A partnership can more effectively drive toward an optimized balance of price and performance.

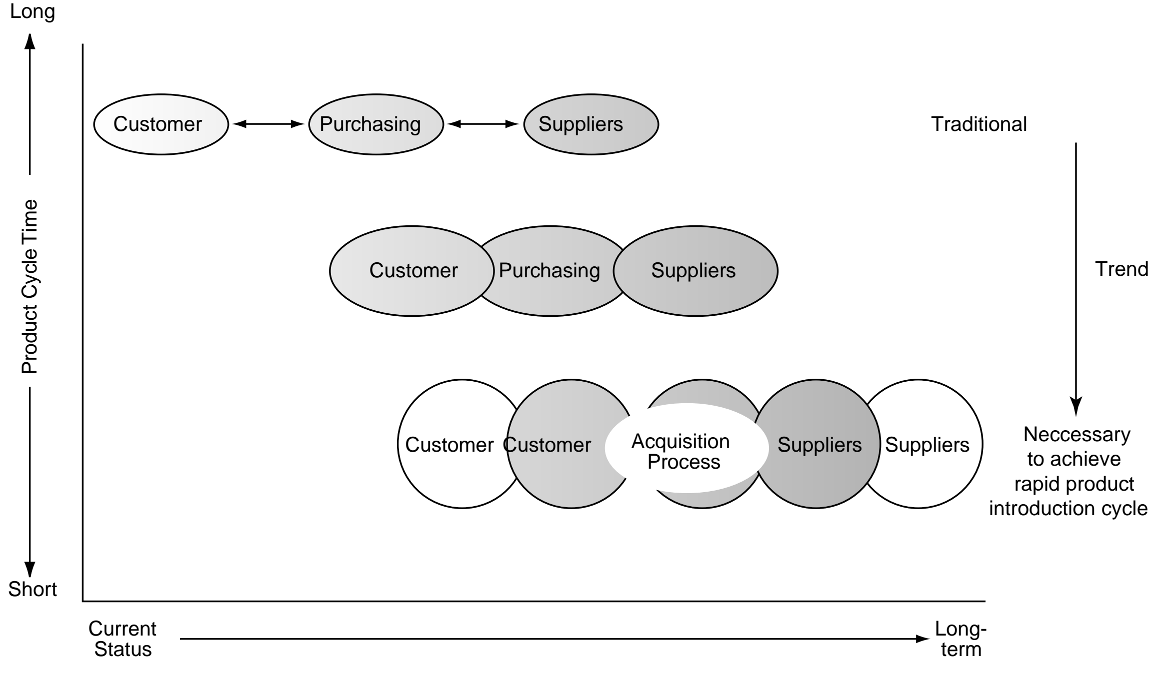
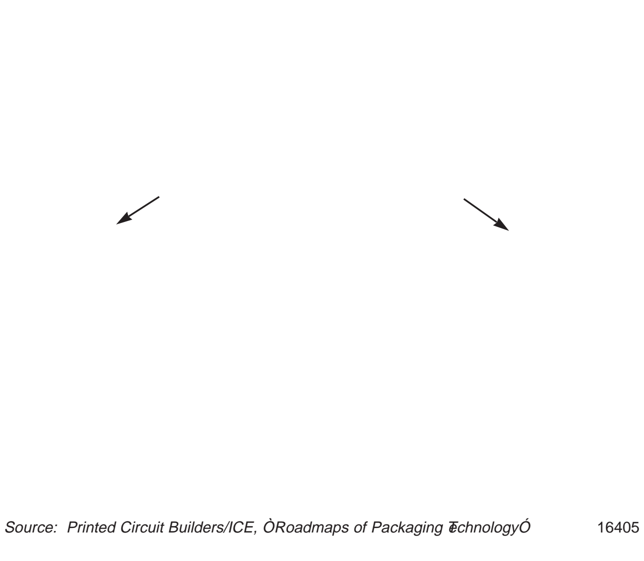


Figure 11-13. Customer Supplier Relationships

Added Features: Buried Vias and Blind Vias

Often, only traces on adjacent layers need to be interconnected. Rather than use a plated-through hole that goes through the entire board, a buried via is used. At an early stage in the process, before all the layers are laminated, through vias can be drilled and plated in double-sided innerlayers. Because the innerlayer is thin at this point, smaller diameter vias can be drilled and a higher interconnect density can be achieved. If the use of buried vias allows a board with fewer layers to be used, there may be a cost advantage. In the very high density boards, buried vias are a must. An example of a cross section of a board showing a buried via and a through-hole via is shown in Figure 11-14.

Alternatively, in the fabrication of a substrate, holes can terminate on particular layers rather than going all the way through. Blind vias are difficult to manufacture with mechanical drilling because they require precision stopping of the drill. They can, however, be made small in diameter and layers can be connected after they are laminated. Laser-drilling is finding wide use in blind via formation. An example of a mechanically drilled blind via is shown in Figure 11-15.



Source: Printed Circuit Builders/ICE, “Roadmaps of Packaging Technology” 16405

Figure 11-14. Buried Via and Through-Hole Via

Source: Electrochemicals/
ICE, “Roadmaps of Packaging Technology” 22542

Figure 11-15. Mechanically Drilled Blind Hole in FR-4

New Materials: Low Dielectric Constant, Controlled TCE

The most commonly used board material is glass weave impregnated with epoxy, described as Flame Retardant (FR) number 4, or FR-4. There are a host of materials that have been used over the years, each with slightly different cost and performance features. Figure 11-16 summarizes these traditional board laminate materials.

Resins and weaves with lower dielectric constants are being utilized in high-speed boards because they reduce the interconnect wiring delays. Rogers offers a Teflon-based material, RO2800, filled with a ceramic to give low dielectric constant and good mechanical stability. 50-layer experimental boards have been made with these laminates.

Grade	Composition	General Properties	Applications	Alternates	Comments
XXXPC	Phenolic/Kraft paper	¥ Excellent punching at room temperature ¥ Low flex strength ¥ Poor wet electrical properties	Automotive Video game controls Calculators	FR-2 FR-6 FR-1	No domestic suppliers (as clad laminate) Non-flame retardant
FR-1	Phenolic/Kraft paper	¥ Punchable at room temperature ¥ Extremely poor wet electrical properties ¥ Lesser grade than XXXPC/FR-4	Automotive Consumer electronics	FR-2 FR-6	No sources in the U.S.
FR-2	Phenolic/Kraft paper	¥ Brittle, but punchable with heat ¥ Similar physical/electrical properties as as XXXPC	Automotive Video game controls Calculators	FR-6 CEM-1 CEM-7	No sources in the U.S. Popular in Far East/Europe
FR-3	Epoxy/Kraft paper	¥ Extremely brittle but punchable with heat ¥ Good wet electrical properties for paper laminate	Telephone sets	FR-6 CEM-1 CEM-3	No sources in the U.S. Popular in Far East/Europe
FR-6	Polyester/Glass material	¥ Outstanding electrical properties ¥ Punchable at room temperature ¥ Higher flex strength than paper products	Consumer electronics Automotive Telecommunications	CEM-1 CRM-5 CRM-7	Excellent high freq. prop. in punchable grade Suitable for low drift apps.
CRM-5	Polyester/Glass fabric surface Polyester/Glass paper core	¥ Outstanding electrical properties ¥ Punchable at room temperature ¥ Double flex strength of FR-6	Consumer electronics Automotive Telecommunications	FR-6 FR-4 CEM-3	Used where outstanding elec. props required Can be drilled/punched
CRM-7	Polyester/Glass fabric surface Polyester/Glass paper core	¥ Same physical/electrical properties as FR-6 ¥ Smoother surface finish	Consumer electronics Automotive Telecommunications	CEM-1 CRM-5 FR-6	Smoother surface suitable for fine-line applications
CEM-1	Polyester/Glass fabric surface Polyester/Glass paper core	¥ Punchable at room temperature ¥ Good electrical properties, but less than polyester ¥ Good flex and impact strength	Consumer electronics	FR-6 CEM-1 CRM-7	Good for punching Performance varies greatly between suppliers
CEM-3	Polyester/Glass fabric surface Polyester/Glass paper core	¥ Punchable, but harder than CEM-1 ¥ Good electrical properties ¥ Suitable for PTH applications	Computer peripherals Keyboards	DRM-5 FR-4	One domestic source Popular in Far East for two-sided applications
FR-4	Epoxy/Glass fabric	¥ High flex and impact strength ¥ Excellent electrical properties ¥ Excellent for PTH applications	Computer applications Telecommunications Military applications	CEM-3 CRM-5 FR-5	Most popular lminate material for drilled PTH applications
G-10	Epoxy/Glass fabric Non-flame retardant	¥ High flex and impact strength ¥ Excellent electrical properties ¥ Excellent dimensional stability	Structural applications	FR-4	Used as unclad laminate for structural parts Non-flame retardant
FR-5	Modified epoxy/Glass fabric	¥ Improved hot flex strength over FR-4 ¥ Excellent electrical properties	Military applications	Polyimide	Original FR-5 materials have disappeared Composition varies by supplier

Source: Printed Circuit Fabrications/ICE, "Roadmaps of Packaging Technology" 22195

Figure 11-16. Copper-Clad Laminate Materials

Alternatively, Gore offers a Gore-Texª weave that can be impregnated with epoxy, which lowers the dielectric constant from 4.8 to 3.5. These Gore-Tex B-stage sheets can be used as the glue layers between copper-clad boards, so that they readily conform with current manufacturing processes. These boards go under the trade name Speed Boards.

The properties of these new materials are summarized in Figure 11-17.

The polymer resin has a very low modulus and typically, a high TCE. The weave and the core dominate the TCE of the composite board. In Figure 11-18, the TCEs of various board compositions are compared. For leadless chip carriers, where the solder joint is particularly sensitive to TCE mis-match, there is a tendency to use copper-clad Invar cores.

MATERIAL	DIELECTRIC CONSTANT
FR4 Epoxy-Glass	4.5-5.5
Polytetrafluoroethylene (PTFE) (Teflon)	2.1
PTFE/Microfiber	2.3
PTFE/Kevlar	2.6
PTFE/Glass	2.3-2.5
Rogers RO2500	2.5
Rogers RO2800	2.8
Gore-Texª Fiber	1.3
Gore-Clad (Bonding layer)	2.6
Gore-Ply (Pre-Preg)	2.8
Polyimide Resin	3.4
Polyimide-Glass	4.5
Polyimide/Fused Quartz	3.4
Polyimide/Kevlar	3.6
Polysulfone	3.0
Benzocyclobutene (BCB)	2.6

Source: ICE, "Roadmaps of Packaging Technology" 15846A

Figure 11-17. Dielectric Properties of New PWB Laminates

MATERIAL	TCE PPM/¡C	MATERIAL	TCE PPM/¡C
Silicon	2.6	INORGANICS	
GaAs	5.7	92% Alumina	6.0
METAL		96% Alumina	6.6
Copper	17.0	SiC	3.7
Silver	19.7	AlN	3.3
Gold	14.2	BeO	6.8
Tungsten	4.5	Diamond	2.3
Molybdenum	5.0	Glass Ceramic	3.0-5.0
Nickel	13.3	Quartz	1.8
Invarª	1.5	Cu-INVAR-Cu	
Kovarª	5.3	12.5/75/12.5	4.4
Aluminum	23.0	20/60/20	5.3
Stainless Steel	11.0	PWB SUBSTRATES	
Au-Sn (80-20)	15.9	Epoxy Kevlarª	9.5
Pb-Sn (95-5)	29.0	Polyimide/Kevlar	3.0-7.0
Cu-W (20-80)	7.0	Polyimide Quartz	14.0
		FR4	18.0
		Polyimide	50.0
		BCB	40.0
		Teflonª	20.0

Source: ICE, "Roadmaps of Packaging Technology" 15847A

Figure 11-18. Temperature Coefficient of Expansion of Common Packaging Materials

Multiwire

A fundamentally different type of wiring process termed "multiwire," which was developed by PCK over 15 years ago, is gaining acceptance today. It combines the benefits of printed circuit technology with some of the features of discrete wiring.

A standard multilayer PWB core is coated with a thin layer of adhesive, and thin polyimide-coated wires are laid out on the surface by an X-Y driven spool. If the top layer of the board is a ground plane, then the impedance of the wires can be controlled. Figure 11-19 shows such a board.

Source: Hitachi/ICE, "Roadmaps of Packaging Technology" 16211

Figure 11-19. Diagonal Wiring Multiwire Boards

The wires are typically 3 mil diameter with a 1 mil coating of polyimide. They can be routed on a 14 mil pitch. Because of their insulated coating, X and Y lines can overlap on the same layer. After all the wires are routed, holes are drilled either mechanically, or more commonly, with a laser to expose the copper of the wire and the copper pads or traces on the board. These pads are copper plated, electrically connecting the wires. Examples are shown in Figure 11-20.

One side coated with X, Y, and diagonal tracks is roughly equivalent to four 2-track layers. Thus, a double-sided core with multiwires on both sides can be equivalent in interconnect capability to a 10-layer PWB. This is also where the prices are at parity. Stacks of multiwire boards can be laminated together to increase the interconnect density even more.

2.5mil Wire Passing Through a Lased Hole

Cross Section of a Lased Via After Metallization

Source: Kollmorgen Corporation/ICE, "Roadmaps of Packaging Technology" 22582

Figure 11-20. SEM Views of Laser Drilled Connections Between Multiwire and PCB Pad

Spool speed is about 4in/sec, depending on the track length. In a typical 2-track multilayer board with 8 signal layers, there are 160 inches of trace per square inch of board area. A board that is 18 inches on a side can have a total trace length of 50,000 inches. The wires for an equivalent multiwire board can be laid out in less than 4 hours.

The chief advantage of multiwire is in the ability to construct or make engineering changes on a prototype with very good electrical properties quickly. For multilayer boards above 10 layers, multiwire may offer a cost advantage as well. This technique may find application with other substrate technologies to provide for the engineering changes that are necessary in nearly every large, complex board design.

BUM Technology (Build Up Multilayer)

The most revolutionary changes in conventional printed circuit board technology are driven by the needs of higher via density. It is the via density that determines the number of I/O per in^2 that can be assembled to the surface and ultimately integrated into the routing channels. This determines the functional density of the board.

The costs associated with mechanically drilling smaller vias take a step function increase below 8 mil diameters, as shown in Figure 11-21. This high cost has been an incentive to find more economical methods of creating smaller vias. With smaller vias, finer pitch traces are also possible. The combination of these two requirements are fueling a revolution in printed circuit board technology. The current leading edge approach to tighter via pitch and finer lines has been popularly termed build up multilayer technology or BUM. It has also been called sequential build up or SBU.

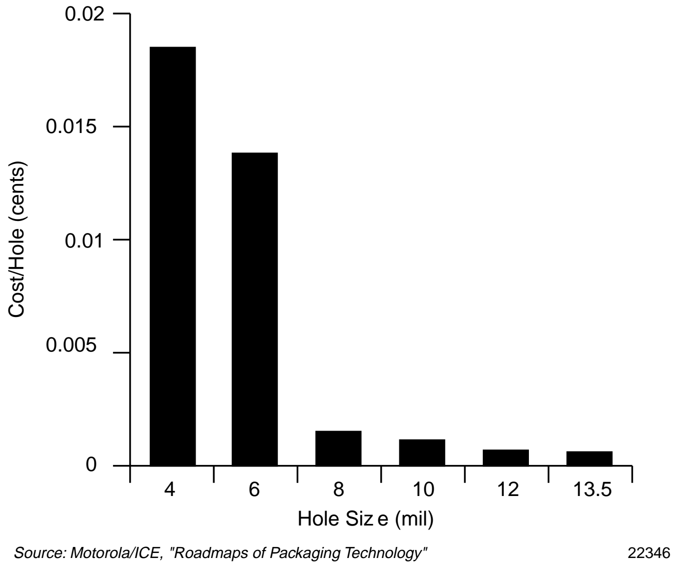


Figure 11-21. Drilling Cost Versus Hole Size

In 1989, Siemens had in production a sequential build up board technology with 3mil wide, half-ounce copper lines, 3mil diameter vias on a 20mil grid, and two tracks of conductors between the vias. This substrate was used to interconnect Motorola ECL gate arrays for a high end mainframe. The gate arrays were flip TAB attached to the surface. The interconnect density of the board is 100 inches of trace per square inch of board area per layer. An example of the board is shown in Figure 11-22. The use of laser drilled holes enabled the small diameter vias between adjacent layers.

Siemens has fabricated boards using six signal layers that have an interconnect density equivalent to the highest of any through-hole printed wiring board technology, even those with 50 layers.

Also in the late 1980Õs, IBMÕs facility Yasu, Japan, began shipment of conventional circuit boards with a layer of photoimageable solder mask used as the last dielectric layer. Vias were imaged into the solder mask and an additive layer of copper was applied with 3mil lines and 5mil spaces. This process was called surface laminar circuit technology (SLC). An example of the surface pads of a SLC board is shown in Figure 11-23, comparing a conventional through-hole with the photo defined holes.

The chief value of applying an extra layer of fine line traces and closely spaced vias on the top surface is to enable the escapes needed for fine pitch packages, such as BGAs, CSPs and DCAs. In addition, as the cost of the BUM layers drops, overall system cost savings may be possible by reducing the number of conventional layers needed. The projected costs for BUM technology based layers is shown in Figure 11-24. Increased volume from BGA, CSP and DCA applications will increase the maturity of the technology and drive the cost curve lower into the cost effective realm that may replace replace conventional technology.

Source: Motorola/Siemens/ICE, "Roadmaps of Packaging Technology" 16111

Figure 11-22. 80-Chip Bipolar MCM Using Fine-Line PWB Interconnect Substrate

Source: IBM/ICE, "Roadmaps of Packaging Technology" 22217

Figure 11-23. Close Up of SLC Substrate with Mechanically Drilled Holes and Photoimaged Micro Vias

When the BUM layers are used to replace the conventional interconnect layers and reduce the total board layer count, the potential cost savings are shown in Figure 11-25. The cost parity point is roughly at a 10 layer conventional board. However, this assumes a mature cost structure

of the BUM technology. An example of the substrate layer stack up in a combined conventional core with three layers of BUM on the top and bottom surfaces are shown in Figure 11-26 and Figure 11-27.

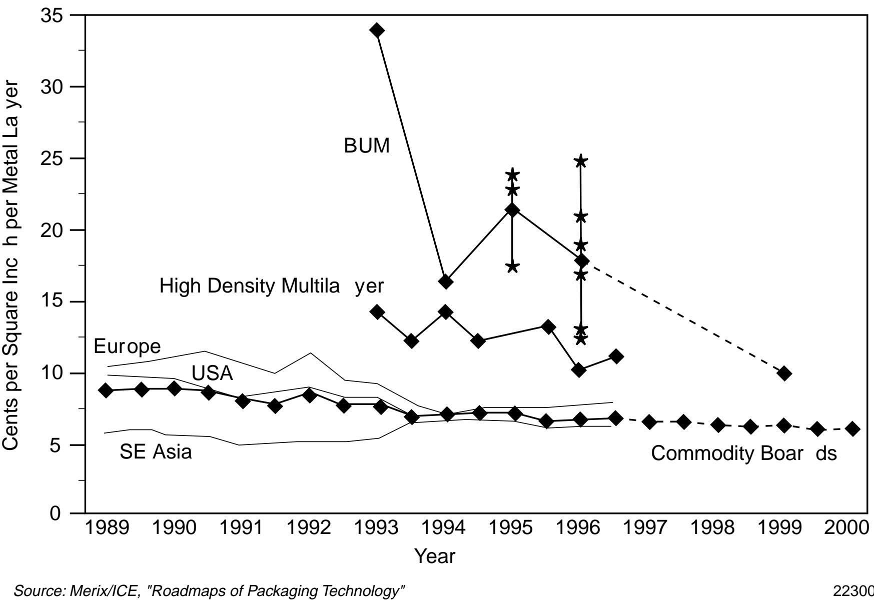


Figure 11-24. Price and Availability Time Line for High Density Multilayers

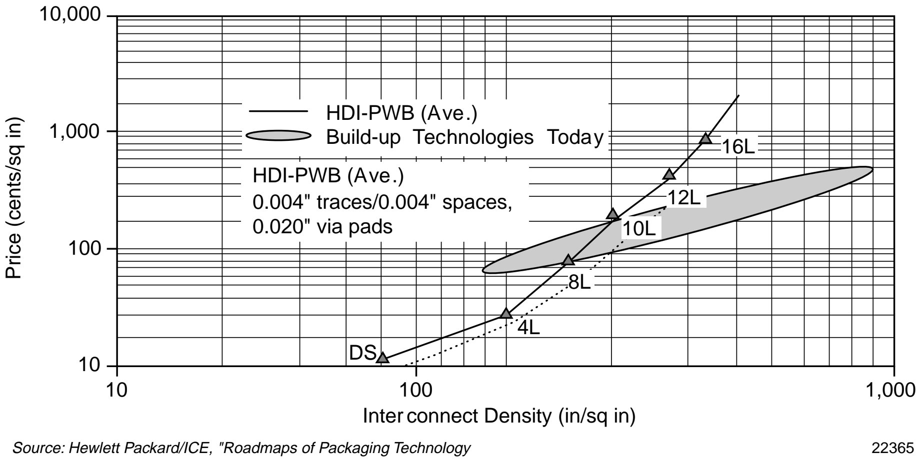


Figure 11-25. Prices for Conventional and BUM Boards

Fueled by this vision of enabling smaller form factor packages and increased functional density for low end consumer portable products and high performance server products, BUM technology has proliferated in the industry. Many names have been used to refer to one or more forms

of this new technology or the processes used to manufacture it. One measure of this prolifera-tion and popularity is the list of acronyms that have arisen to describe the fabrication process or final substrate, such as:

MCM-L multi-chip module, laminate
SLC- surface laminar circuits
MVT- micro via technology
ASM- advanced solder mask
ALT- advanced laminate technology
HDI- high density inter connect
PPM- photo polymer multistrates
ALIVH- any layer inner via hole
DVH- dimple via hole
FRL- film redistribution layer
IBSS- IbidenÕs built up structure system
RCC- resin coated copper
CFC- carrier formed circuits
PID- photoimageable dielectric
PERL- plasma etched redistribution layers

Design Rule	Current (µm)
Line width	45
Line-Line Spacing	45
Via Diameter	100
Via Pad Diameter	150
Conductor Thickness	15 - 20
Insulator Thickness	40 - 60

Source: Fujitsu Computer Packaging Technologies/ICE, "Roadmaps of Packaging Technology" 22351

Figure 11-26. Lay-Up Structure for Core Substrate and 6 Layers of BUM

There is a blurring of the boundary between BUM substrates and MCM-L, MCM-D or MCM-D/L substrates. Often, BUM and these MCM substrates are fabricated with the same processes and end up with the same feature sizes.

Source: SMT/ICE, "Roadmaps of Packaging Technology" 22416

Figure 11-27. Cross Section of a Plasma-Produced Eight-Layer Micro Via Board Showing Blind Vias and a Buried Via Core

In general, there are three generic processes used to form the micro vias. Listed below are the processes and some of the vendors using the technique. Figure 11-28 lists the major vendors for these technologies. Figure 11-29 summaries typical features for these processes.

- photo defined dielectric: IBM, Continental
- plasma etching: Dyconex, HP, Merix
- laser etching: Lumonics, ESI, Sheldahl

These fabrication processes are outlined in Figure 11-30. In all cases, the lower layer of interconnect is patterned with conventional methods, either additive or subtractive. In a subtractive process, the copper is applied as a laminated sheet. Photoresist is applied over the copper foil as dry film, liquid or electrophoretically coated. In the latter case, photoresist layers as thin as 10 microns can be applied, which translates to finer linewidths than can be traditionally imaged and etched.

The photoresist is imaged and developed for the fine traces that are required to interconnect the micro vias, with typically 1 to 3mil linewidths. An example of very fine lines on an organic substrate is shown in Figure 11-31. After patterning, the dielectric is applied and the via layer created.

Company	Description
Amoco	Liquid dielectric, photoimaged (polyimide)
Continental Circuits	Liquid dielectric, photoimaged (epoxy)
Fujitsu	Liquid dielectric, photoimaged (polyimide)
Ibiden, IBSS	Liquid dielectric, photoimaged (epoxy)
IBM, Yasu, SLC	Liquid dielectric, photoimaged (epoxy)
NEC	Liquid dielectric, photoimaged (benzocyclobutene)
IBM Endicott/Austin	Laminated dielectric, photoimaged (epoxy)
Dyconex	Laminated dielectric, plasma-etched (polyimide)
HP GmbH	Laminated dielectric, plasma-etched (epoxy or polyimide)
STP	Laminated dielectric, plasma-etched (polyimide)
GEC-Marconi, Microtrace	Film dielectric, laser-drilled (polyimide)
General Electric, HDI	Film dielectric, laser-drilled (polyimide)
Sheldahl, Novaflex	Film dielectric, laser-drilled (polyimide)
Hitachi, HITAVIA	Film dielectric, drilled (polyimide)
Hitachi, Transfer LAM. Circ.	Plated Cu post process (epoxy)
Oki Electric, Via Post	Plated Cu post process (epoxy)

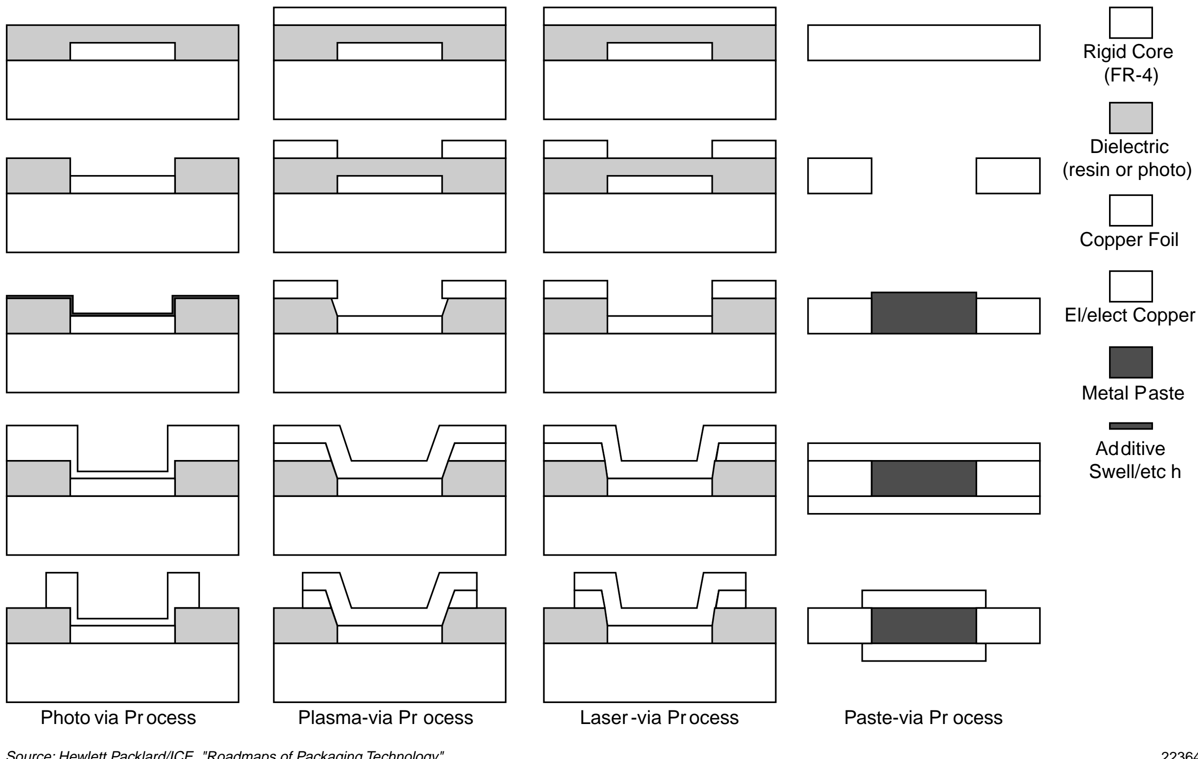
Source: TechSearch International, Inc./ICE, "Roadmaps of Packaging Technology" 22394

Figure 11-28. Build-Up Board Suppliers

Technology	Insulation Material and Dielectric Constant	Lines/Spaces (µm)	Via/Land Diameter (µm)
Microfilled Vias (MfVia)	Epoxy, PID, 3.8	75/75	125/250
Photo-via Redistribution Layer	Epoxy, PID	100/100	125/380
Conductive Adhesive Bonded Flex	Polyimide film, 3.8	25/50	25/200
Seq. Bonded Film (DYCOstrate)	Polyimide film, 3.8	75/75	100/200
Surface Laminar Circuits (SLC)	Epoxy, PID, 3.8	75/75	125/250
Build-up Structure System (IBSS)	Epoxy, +PES, 4.0	75/75	125/250
Carrier-Formed Circuits	Epoxy arcylate, 3.6	100/100	150/400
Roll Sheet Build-up	Epoxy, 3.2	100/100	150/450
Sheet Build-up	Epoxy, 3.2	75/75	100/400
Sequential Bonded Solid Vias	Epoxy aramid, 3.8	100/100	125/250
High-Density Interconnect (HDI)	Polyimide film, 3.8	25/50	25/200
Buried Bump Interconnect (B^{2}it)	Epoxy glass, 4.3	100/100	125/250
Microwiring	Polyimide film, 3.8	100/100	125/250
Conductive Ink Build-up	Epoxy, PID	75/75	125/125

Source: Hewlett Packard/ICE, "Roadmaps of Packaging Technology" 22363

Figure 11-29. Dielectric and Densities of 14 ÒBuild-UpÓ Technologies



Source: Hewlett Packlard/ICE, "Roadmaps of Packaging Technology" 22364

Figure 11-30. µVia Process Flow

Source: Circuitree/ICE, "Roadmaps of Packaging Technology" 22348

Figure 11-31. 50 Micron Traces on Flex

In the case of photoimageable dielectric, the dielectric is applied, vias opened up, and a layer of copper is grown additively over the entire surface. This is built up electrolytically and either subtractively etched or pattern plated. In the case of plasma etched or laser etched, the top

dielectric layer is actually a laminated copper foil with adhesive. This is often termed RCC (resin coated copper), and is typically 1-2mils thick. After the copper foil is laminated, vias are photoimaged in the copper with photoresist and the copper is etched. These micro via holes in the copper are used as the mask to create the vias in the dielectric. The copper pad on the other side of the via is used as the etch stop. After via formation, copper is plated in the hole and up the side with additive chemistry.

Figure 11-32 is a magnified view of an MCM substrate based on BUM technology and a magnified view of the interconnect, after the surrounding dielectric has been plasma etched away. Also shown is a cross section of a laser drilled hole and plated up via.

Source: Lumonics

Laser µVias on an MCM

Source: Electro Scientific Industries

150µm Laser Drilled Blind Via in Polyimide

Source: Electro Scientific Industries

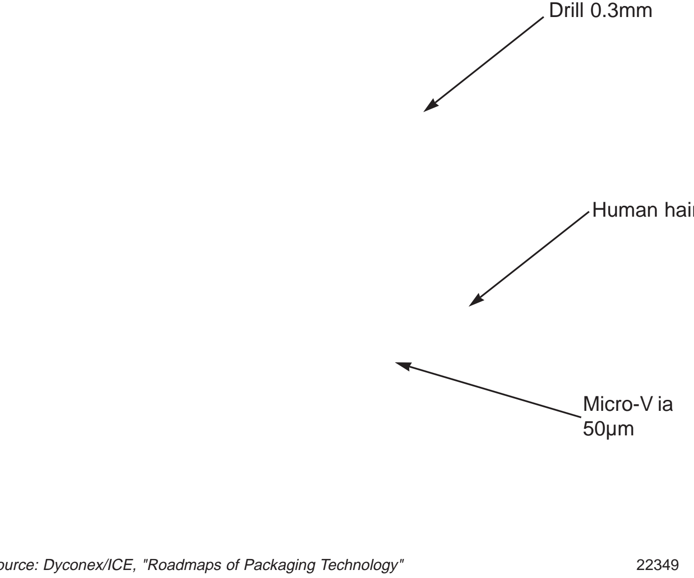
Cross Section of 6mil Laser Drilled Blind Via in FR-4

Source: ICE, "Roadmaps of Packaging Technology"

22173

Figure 11-32. Close Up of Laser Drilled Vias

Figure 11-33 provides a magnified view and a size comparison between a 50 micron via hole created with plasma etching on a 200 micron pad, with 75 micron linewidths, and a conventional 12mil diameter drill bit.



Source: Dyconex/ICE, "Roadmaps of Packaging Technology" 22349

Figure 11-33. Comparison of 50µm Microvia Fabricated by Plasma Etching and 12mil Drill Bit

An intriguing alternative to the popular BUM approaches is based on a new process from Toranaga Technologies that uses an organic based thick film conductive paste. Traditionally, conductive pastes have been screened on circuit boards as polymer thick film. There has always been a limitation to the feature sizes due to the screen printing process. Lines are typically larger than 6 mils and vias are typically larger than 8mils.

In the Toranaga process, outlined in Figure 11-34, a blanket coat of a photoimageable dielectric is applied to the surface of the substrate, either as dry film laminate or curtain coated. Trenches, forming the area for the conductor traces, are patterned in the dielectric. These can be as fine as 2mils wide. The Ormet copper based conductive ink is screened into the trenches using a doctor blade, forming the traces on that layer. The ink is then cured and the surface burnished to remove any excess ink. Another layer of photoimageable dielectric is then applied and imaged forming the vias. Via holes as fine as 75 microns have been demonstrated. The ink is screen printed into the vias and then fused and the process can start over again.

Figure 11-35 is a magnified view of the cross section of two conductor layers and a via between them. Figure 11-36 shows the via structure when the Ormet paste is used to form the via connections between three conventional inner layers cores.

This process shares the same via forming process as the PID techniques of BUM, but utilizes a potentially lower cost metallization process. This technique might be well suited for small manufacturing plants that do not want to avoid the waste treatment issues associated with electroless and electrolytic copper deposition.

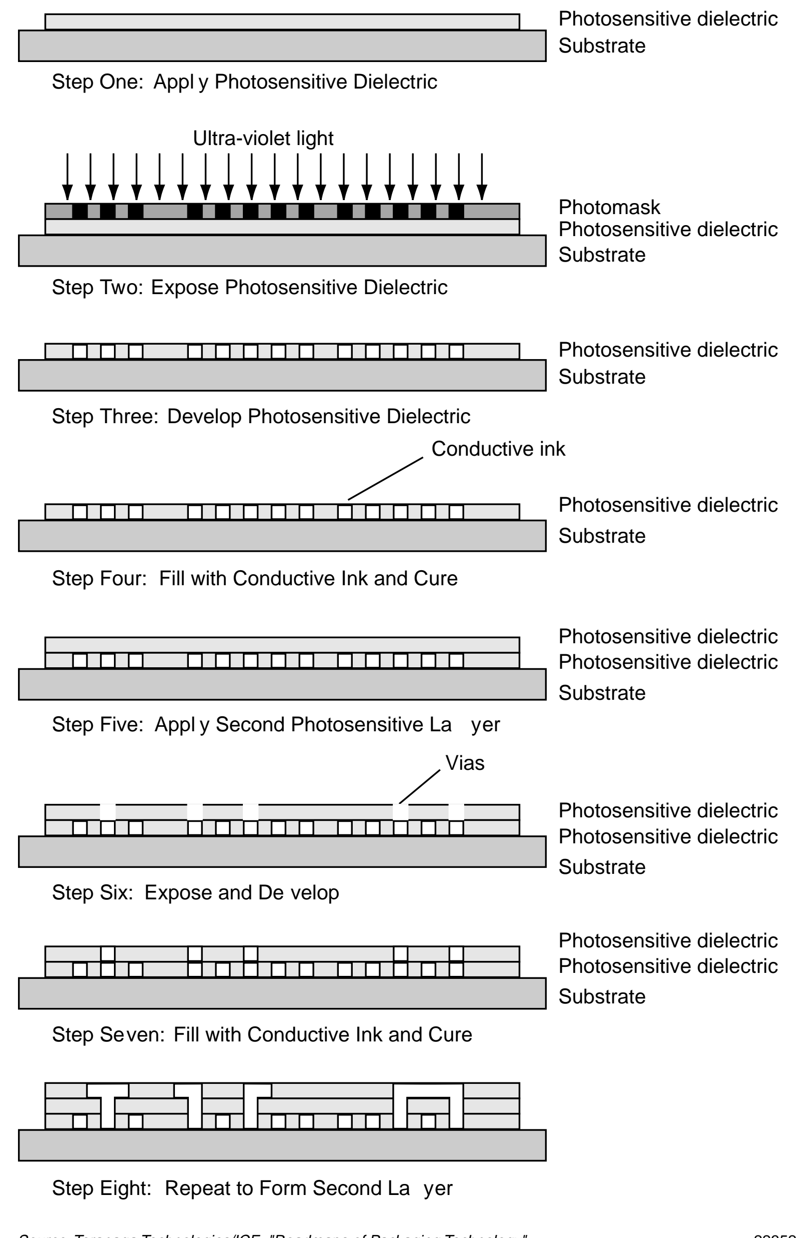
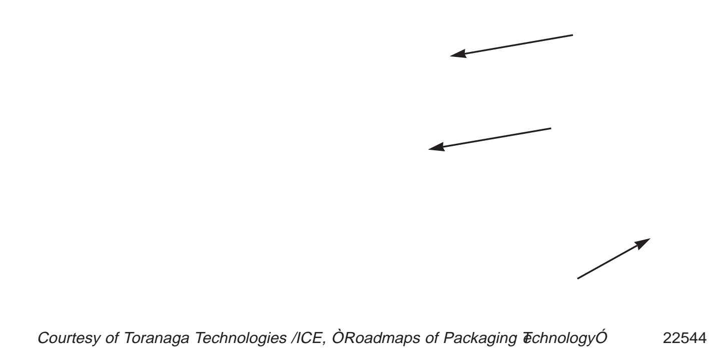
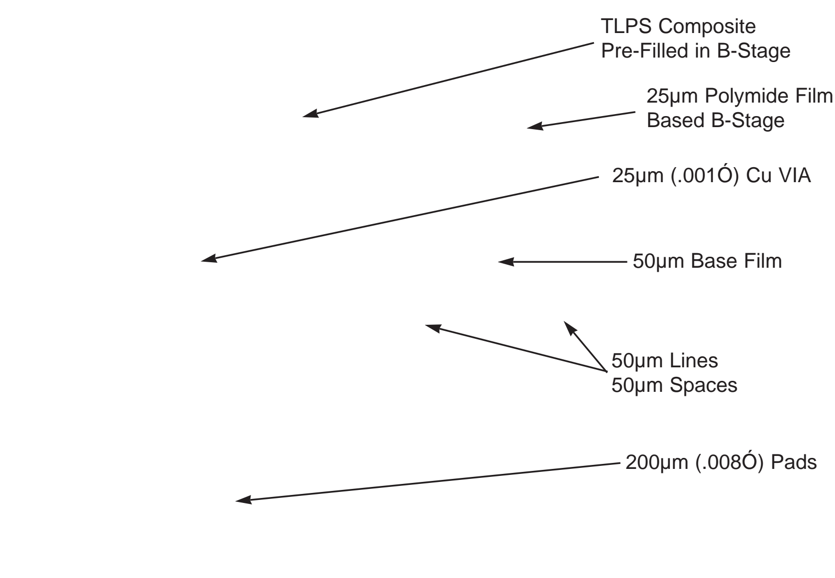


Figure 11-34. Multilayer Fine-Line Printed Circuitry Using Toranaga's Process



Courtesy of Toranaga Technologies /ICE, ÒRoadmaps of Packaging TechnologyÓ 22544

Figure 11-35. Ormet¨ TLPS Conductive Material in Circuit Traces and Vias



Source: Toranaga Technologies/ICE, ÒRoadmaps of Packaging TechnologyÓ 22548

Figure 11-36. Ormet¨ TLPS Conductive Composite Between 200 µm Pads

THICK-FILM BOARD TECHNOLOGY

Basic Process: Screen Printing and Firing

Thick-film substrates have been the workhorse substrates for small military cards and hybrids for many years. An example of an assembled board is shown in Figure 11-37. Thick film will not be an important candidate technology for substrates used in high-density, high-speed applications for four fundamental reasons.

1. It is very difficult to fabricate boards with thick enough dielectric layers to provide 50 Ohm characteristic impedance traces.

2. The via diameters must be at least 8mils and the pitch typically on the order of 20mils, thereby reducing the potential via density.

3. The dielectric materials have dielectric constants on the order of 8-14, and alternative substrates are available with higher interconnect density and better electrical performance.

4. Thick film manufacturing is fundamentally a sequential process. For high interconnect density, many layers are needed and the yield drops exponentially as the number of layers increases.

Source: White Technology/ICE, "Roadmaps of Packaging Technology" 16084

Figure 11-37. 68020 Computer Module on Thick Film Substrate

Despite these drawbacks, some applications are well suited for thick-film substrates. This technology is ideal where low-cost, ultra-reliable, low-density interconnects are required and bandwidths are low enough that controlled impedance interconnects are not needed. The capital costs and manufacturing expertise for thick-film are lower than for cofired ceramic substrates.

The inert base substrate is typically made from 95 percent alumina and 5 percent glass. A paste composed of either small metal particles or dielectric material and an organic binder is squeezed through a fine-mesh screen that has unmasked openings in the screen only where the final mate-

rial is to appear. Using photolithography, the conductor pattern artwork is transferred to openings in an emulsion coating which has been patterned. A squeegee forces the paste out through these openings, translating the artwork into physical patterns on the substrate. This is diagrammed in Figure 11-38.

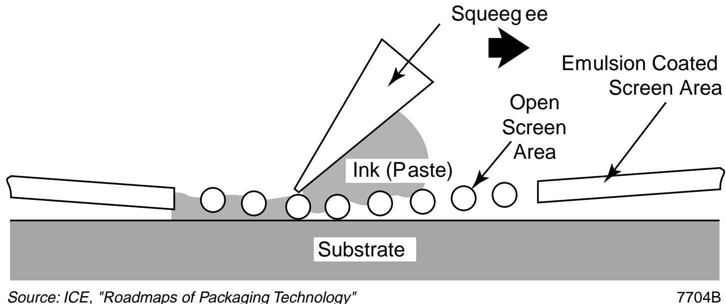


Figure 11-38. Screen Printing Process

After each layer is screened down, it is fired at high temperature, typically 900¡C, to remove the organic binder and sinter the conductor particles together. After firing, the next layer is deposited.

Dielectric layers are also deposited by screen printing, and vias are formed by obstructions in the screen preventing deposition. The minimum via size, about 8mils in current technology, is limited by the flow of the paste after screening. The separation between vias is typically 20mils. A close-up and a cross section of a typical thick-film substrate are shown in Figure 11-39 and Figure 11-40, respectively.

Source: ICE, ÒRoadmaps of Packaging TechnologyÓ 15934

Figure 11-39. Close-Up of a Thick Film Substrate

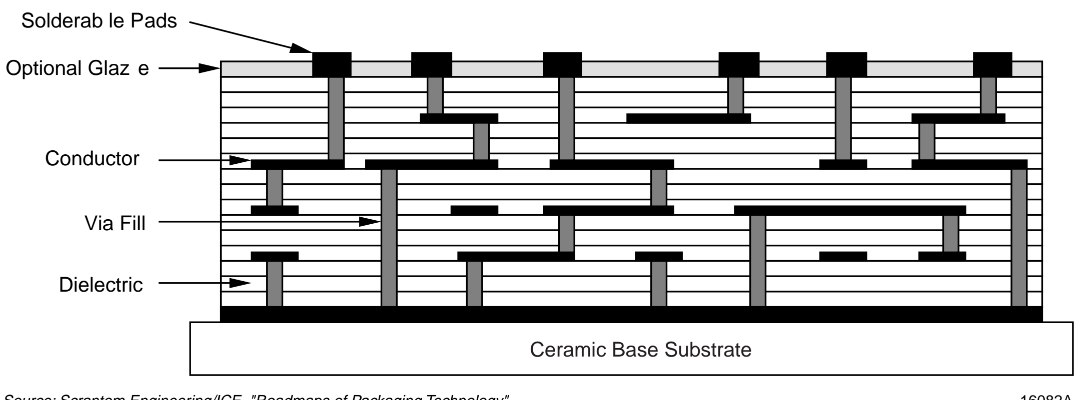


Figure 11-40. Typical Cross Section of a Thick-Film Ceramic Substrate

The thickness of dielectric that can be deposited depends on the paste viscosity and composition and the thickness of the emulsion on the screen. It is typically about 0.75-1mil per coating. With a linewidth of 5mils and dielectric thickness of 1mil, the characteristic impedance of a microstrip line with dielectric constant of 8 will be about 15 Ohms, in a best case scenario.

The layers are built up sequentially, so the value of the substrate increases through the process steps and larger features are sometimes used at higher layers to increase the yield. More than 8 to 10 layers become very expensive with thick film.

Photoformed Conductors On Ceramic Substrates (PCS)

DuPont has introduced a new process and material system for generating fine lines with thick-film substrates. In conventional thick film technology, the linewidth is determined by the screen printing process. DuPont's PCS process involves coating the substrate with a proprietary, photo-sensitive organic coating that becomes tacky when exposed to UV light. After exposure, the surface is coated with a toner of fine gold particles, which adheres where the polymer was exposed.

These coated substrates are fired as in conventional thick-film and the resulting traces are further processed in the standard way. This process is diagrammed in Figure 11-41. Because they are photolithographically patterned, features as small as 1mil in width have been fabricated.

COFIRED CERAMIC TECHNOLOGY

Cofired ceramic substrates are similar to thick film in that conductors are patterned, and the final product is basically a brick with embedded three-dimensional wiring. However, the substrates differ in the metallurgy and in specific process sequences. With the use of thicker dielectric layers and punched vias, cofired ceramic substrates allow tighter via pitches, higher interconnect density and better electrical performance than thick film technology.

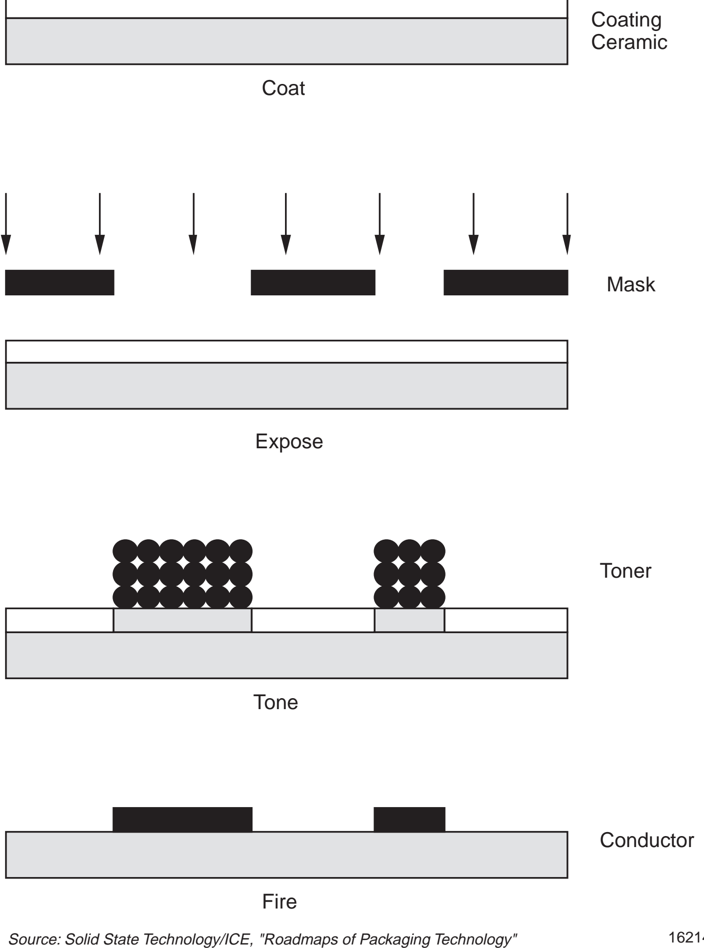


Figure 11-41. PCS Process

Cofired ceramic substrates compose over 95 percent of the high-performance, ceramic, single-chip packages and form the basis for IBM's multichip modules. The chief features of cofired ceramic substrates and their advantages over thick-film are:

1. They are able to provide a reliable and hermetic environment for the interconnect and the chips.

2. Their TCE, 6ppm/¡C, closely matches silicon's TCE of 3.0ppm/¡C.

3. With thick dielectric layers they offer better electrical performance than thick-film ceramic.

4. With punched vias, the via pitch can be made tighter than thick-film.

5. Each layer is fabricated separately and can be inspected before laminating. This allows reasonable yields for a high number of layers.

6. There are a number of merchant suppliers of cofired ceramic substrates.

The basic material in use today is a mixture of 90-95 percent alumina (Al_2O_3) and glass, fired at about 1,600°C, with tungsten or molybdenum metallization. This is termed high temperature cofired ceramic (HTCC).

This is in distinction to a process based on a high glass concentration ceramic which fires at a lower temperature, close to 900°C. This material system is termed low temperature cofired ceramic (LTCC). Though the ceramic is different, and the conductor paste can be copper or silver based, the process steps to manufacture LTCC is the same as HTCC. In addition to the higher conductivity conductors, the dielectric constant of the glass-ceramic is lower, typically 5-7 and since the firing temperature is lower, the manufacturing costs are lower.

Basic Process: Green Tape, Screen Printing, Laminating, Cofiring, And Plating

The generic cofired process is shown in Figure 11-42. A slurry of the ceramic powder and an organic binder is mixed and cast as a continuous tape, which is then cut into sheets. Because this tape often has a green tint, it is usually termed "green tape." The name has been applied to other tapes that are not tinted green, referring to the fact that before firing, it is not "ripe" yet, as in a green banana.

Each sheet will have vias punched and filled with a conductive paste, and conductor traces screen printed on one side. These sheets are laminated together and fired under high pressure to remove the organics and sinter the ceramic substrate and the conductors.

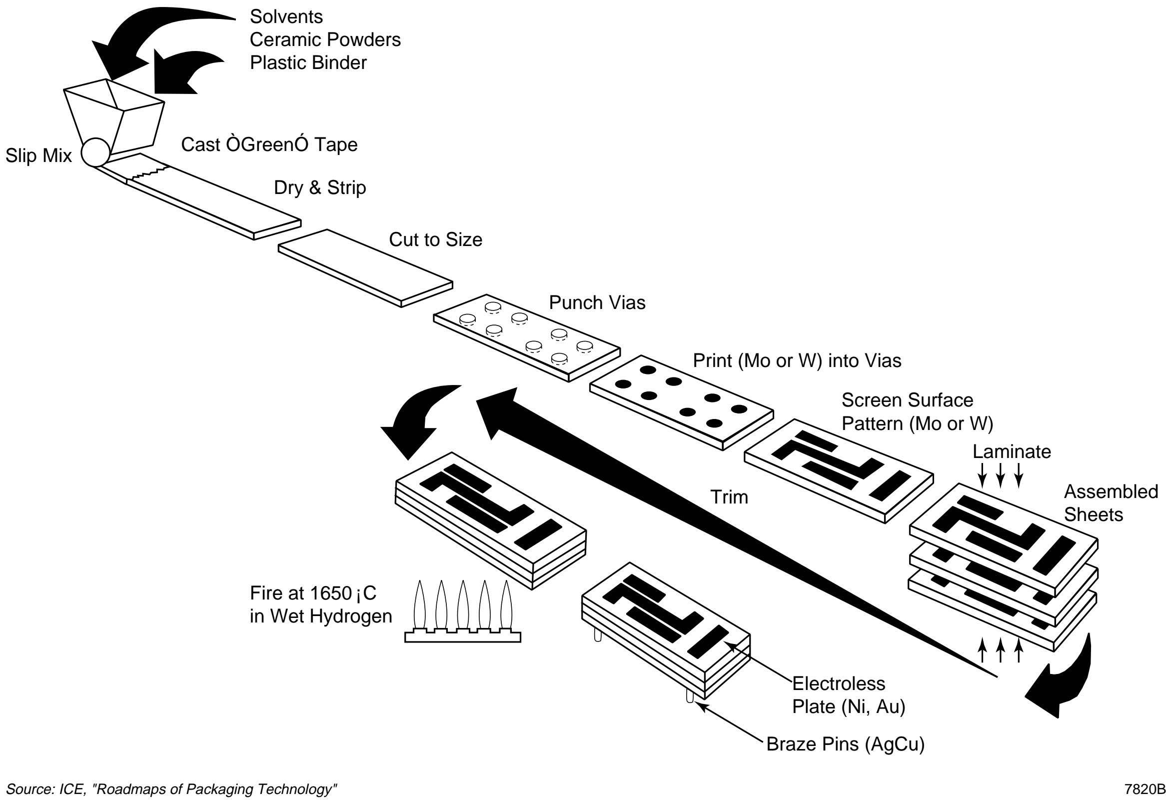
All of the layers are fabricated in parallel and are usually inspected and repaired as needed, before lamination. Because these layers are all fired at the same time, the process is termed "cofired" to contrast it with thick film, which is a sequentially fired process.

After firing, nickel and gold are plated on the surfaces, as required, and pins or leads can be brazed to the base or periphery. An example of a cross section of a cofired substrate is shown in Figure 11-43.

Technology Capability

The dielectric thickness is set by the tape thickness, which can range from 2 to 10mils. Via diameters are typically the same as the thickness of the tape. In volume production, they are mechanically punched, either with a single tool with multiple pins or a tool mounted to an X-Y positioner.

Laser drilling is in use in captive lines at IBM and Unisys, for example. Laser drilling allows very fast turnaround of a prototype part. Unisys has claimed two weeks from design to tested part on its prototype line.



Source: ICE, "Roadmaps of Packaging Technology"

Figure 11-42. Multilayer Ceramic Substrate Process Sequence

Source: Medtronic, Micro-Rel Division/ICE, "Roadmaps of Packaging Technology" 16122

Figure 11-43. Cross Section of Cofired Ceramic Hybrid Pacemaker

Vias can be staggered or stacked. To ensure a hermetic barrier, at least one pair of vias should be staggered from the inside to the outside because the metallization in the vias can be porous.

Conductor features are determined by the screen printing process and are typically 4 to 10mils in width, with 5mil minimum spacing.

High firing temperature alumina is fired at 1,600°C. Only refractory metals such as tungsten or molybdenum can withstand this temperature. The resistivity of tungsten paste, about 20μΩ-cm, provides a sheet resistance of about 10mΩ/sq. A trace 5mils wide would have a series resistance of 2Ω/in. The series resistance of a 5mil wide, 1 ounce copper trace on a PWB would be 0.13Ω/in.

The material properties, geometric features, and electrical properties are summarized in Figure 11-44.

Dielectric Material	Alumina
Dielectric Constant	9.5
Time of Flight	0.25nsec/in
Dielectric Thickness	4 – 8mils
Conductor	Tungsten
Conductor Thickness	0.5 – 1.0mil
Sheet Resistance	8 – 16mΩ/□
Min Linewidth	4mils
Resistance per Length	2Ω/in
Capacitance per Length (at 50Ω Characteristic Impedance)	5.2pF/in
Via Diameter	4mils
Min Via Grid Pitch	10mils

Source: ICE, "Roadmaps of Packaging Technology" 15848A

Figure 11-44. Cofired Ceramic Properties

Shrinkage Control

A significant design concern with cofired ceramic substrates is their shrinkage in the cofiring stage. The after-fired shape is typically 17 percent smaller in linear dimension than the green-tape version. Various factors affect the precise amount of shrinkage: the tape composition, the paste, the via density, and the particular metallization pattern. Significant development work has been dedicated to matching the shrinkage of the ceramic tape and the tungsten paste.

A problem arises from the uncertainty in the amount of shrinkage. It is typically about 17 ±0.7%. In very well controlled processes it can be as low as ±0.2%. Over a field of two inches, an uncertainty of ±0.7% means a variation in pad location of ±14 mils. This sets a minimum size for capture pads on the surface to allow further applications of the substrates that rely on a fixed geometry, such as automated pick-and-place or wirebonding devices.

Precise control of the powder starting materials improves the shrinkage uncertainty. Ceramic Process System (CPS) uses a sol gel process to create uniform particle sizes, which offers 99.6 percent Al_2O_3 substrates with a shrinkage tolerance of ±0.2%, suitable for tungsten metallization. With this control, substrates that have an array of 14mil diameter vias with a center-to-center tolerance over a 4 inch span of less than 8mils can be manufactured. The use of 99.6 percent alumina also offers a very flat and smooth surface finish on both sides. An example of the CPS Viastrate™ is shown in Figure 11-45.

Source: *Ceramics Process Systems Corporation/ICE, "Roadmaps of Packaging Technology"* 16072

Figure 11-45. Viastrate™ Conductive Feedthrough Ceramic Substrate

New Materials

DuPont has introduced a new "low-fire" ceramic with a fired dielectric constant of about 8.5. This material has been termed low temperature cofired ceramic (LTCC). Other materials in this family are composed of Cordierite ceramic. The fabrication process is identical to high-temperature cofired ceramic processing, except the material fires at only 900°C. This allows the use of lower melting point metals such as gold, silver, copper and silver-palladium. Typical sheet resistance at 0.3mil thick coatings is 5mΩ/sq, about half that of tungsten paste that is twice as thick. The other advantage of this material is the shrinkage control, which is within ±0.2%.

Tektronix's version of low-fire multilayer ceramic has a dielectric constant of 5.8 and TCE of 4.6ppm/°C. With careful process control, it can allow fabrication of 4mil vias and 4mil lines on a 7mil pitch.

Fujitsu has announced a new glass-ceramic substrate with a dielectric constant of 5.7 that is used in its VP2000 super computer. Substrates are fabricated in a cofired process at 1,000°C. This allows the use of copper conductors. Substrates with up to 62 layers have been fabricated. Conductors are 4mils wide, with vias 3mils in diameter, on a 17mil grid. An example of the cross section of a 62 layer LTCC cofired ceramic substrate with 4 layers of thin film polyimide on top is shown in Figure 11-46.

Courtesy of Fujitsu Computer Packaging Technologies/
Source: ICE, "Roadmaps of Packaging Technology"
22472

Figure 11-46. Cross Section of 62 Layer LTCC Substrate Used in the Fujitsu VP2000 Super Computer

This technology is also used in IBM's System 9000 mainframes. Figure 11-47 is an example of the cross section of a 52 layer LTCC substrate with one layer of thin film polyimide on top.

LTCC is becoming a popular technology, replacing some applications of HTCC. It offers lower cost than HTCC and has a lower dielectric constant and lower resistivity conductors. DuPont and Ferro offer LTCC tapes with fired dielectric constants from 5.3 to 6.5.

CPS and WR Grace/Coors are working on cofired aluminum-nitride and copper conductors. These substrates would offer the added advantage of high thermal conductivity.

The features of selected new materials systems are summarized in Figure 11-48.

Source: IBM/ICE, "Roadmaps of Packaging Technology" 22392

Figure 11-47. Cross Section of 52 Layer Cordierite Substrate with 1 Layer Thin Film-Polyimide on Top

MATERIAL	COMPOSITION	SINTERING TEMP.	CONDUCTOR METAL	e_r	TCE	THERMAL CONDUCTIVITY (W/cm•°K)
DuPont "Lowfire Green Tape"	Glass-Ceramic	900°C	Gold, Silver, Copper, Silver/Paladium	8.5	7.9	0.04
Tektronix "Low-fire"	Aluminum (25%) Glass (75%)	900°C	Gold, Silver, Silver/Paladium	5.8	4.6	0.02
NEC Glass Ceramics	Aluminum (55%) Lead-Borosilicate Glass (45%)	900°C	Silver/Paladium, Platinum/Gold	7.5	4.2	—
	Cordierite (MgO-Al_2O_3) (45%) Borosilicate Glass (55%)			5.0	7.9	—
	SiO_2 (35%) Borosilicate Glass (65%)			3.9	1.9	—
W.R. Grace/Coors AlN	Tungsten	1800°C		4.3	2.3	—

Source: ICE, "Roadmaps of Packaging Technology" 15849A

Figure 11-48. New Cofired Ceramic Materials

THIN-FILM MULTILAYER SUBSTRATES

The thirst for higher interconnect density substrates has driven the introduction of a wide spectrum of new technologies. Methods whose origins are in printed wiring board, thick film, and cofired ceramic were described earlier in this chapter. They push the state of the art in these technologies to generate features in the 2mil to 4mil range. Each incremental step toward smaller features is much harder than the one before. To approach the sub-mil range, it is probably necessary to consider IC thin-film technology, which is already producing sub-micron features, and to scale the technology up.

Thin-film metallization, applied by either evaporation or sputtering, has its origins in the IC fabrication steps. In general, the finest feature that is possible to delineate in a conductor is a small multiple of the thickness of the trace. For example, in PWB processes, the narrowest lines are typically about two to five times the thickness of the metal. The key feature of thin-film metallization is that the thinness, typically five microns or less, allows lithographic features in the 10-25 micron wide range. These narrow traces, combined with small via technology, offer an interconnect density that can be a factor of 10 greater than all other conventional methods, for the same number of layers.

Thin-film technology has been used in substrates for over 25 years, pioneered by AT&T in its thin-film hybrid products. An example of an early thin-film hybrid is shown in Figure 11-49. The early substrates were 99 percent alumina ceramic and were termed "thin-film ceramic" because they were used in this thin-film application. These substrates have a small grain structure and relatively smooth surface finish. A metallization of titanium, palladium and gold (Ti/Pd/Au) allowed 3mil lines to be fabricated routinely. The early thin-film structures were one layer only. Combining thin-film with thick-film made cross-unders feasible and these substrates were termed one and a half layers of interconnect.

Source: AT&T/ICE, "Roadmaps of Packaging Technology" 15925

Figure 11-49. AT&T Beam-Lead Hybrid

The key common feature among the plethora of "thin-film," high-density substrates is their use of IC manufacturing technology to fabricate the fine lines. Typical IC interconnect features are less than two microns. They are easily capable of being relaxed to provide the 10 micron to 25 micron features currently being used for interconnect substrates. The common method in practice to fabricate high-density, thin-film interconnect substrates is the use of vacuum sputtering to deposit at least the initial flash coating of metal and spin coating of photoresist in a very thin layer to define the feature sizes.

However, there has been tremendous diversity in every other aspect of thin-film substrates, such as the choice of:

- Substrate material
- Type of conductor metal
- Method of fabricating the full conductor thickness
- Dielectric materials
- Via generation methods
- Top metallization method

In Figure 11-50, some of the options that have been tried for these various features are listed.

SUBSTRATES:
- Silicon
- Thin-Film Ceramic (98 - 99.5% Al_2O_3)
- SiC
- AlN
- Cofired Ceramic (90% Al_2O_3)
- Glass Ceramic (55% Al_2O_3)
- Glass
- Sacrificial Al

THIN-FILM CONDUCTOR METAL:
- Gold
- Chrome/Copper/Chrome
- Titanium/Copper/Titanium
- Nickel/Copper/Nickel
- Copper
- Aluminum

DIELECTRIC MATERIALS:
- Polyimide
- Photo-Imageable Polyimide
- Benzocyclobutene (BCB)
- SiO_2

PROCESSES:
- Metallization:
  - Sputtering (all metals)
  - Electroplating (Copper, Nickel, Gold)
  - Electroless Plating (Copper, Nickel, Gold)
- Via Formation:
  - Wet Etching
  - Plasma Etching
  - Laser Etching
  - Mechanical Punching by Posts
  - Mechanical Drilling
  - Photo-imageable

Source: ICE, "Roadmaps of Packaging Technology" 15850A

Figure 11-50. Demonstrated Material and Process Options in Thin-Film MCM Technology

Glass Versus Polymer Dielectric

Gate array technology is currently using 3-4 layers of metal interconnect and will soon be moving to 5-6. Why not use exactly the same technology for high-density interconnect substrates? In fact, one of the first demonstration vehicles of silicon-on-silicon packaging used an IC process. In 1975, K. Reinitz and R. Hicks of Johns Hopkins' Applied Physics lab built a 5-chip multichip "hybrid," using an aluminum/silicon-dioxide wafer, fabricated on a standard CMOS line. The silicon substrate started with an oxide coating and three layers of aluminum with silicon-dioxide insulation layers. The dice were epoxy die attached and gold wirebonds were used. This demonstration vehicle was motivated as a replacement for thick-film hybrids. A cross section of the module is shown in Figure 11-51. There are three fundamental reasons why the process has not been adopted: poor yields, poor electrical performance and planarization requirements.

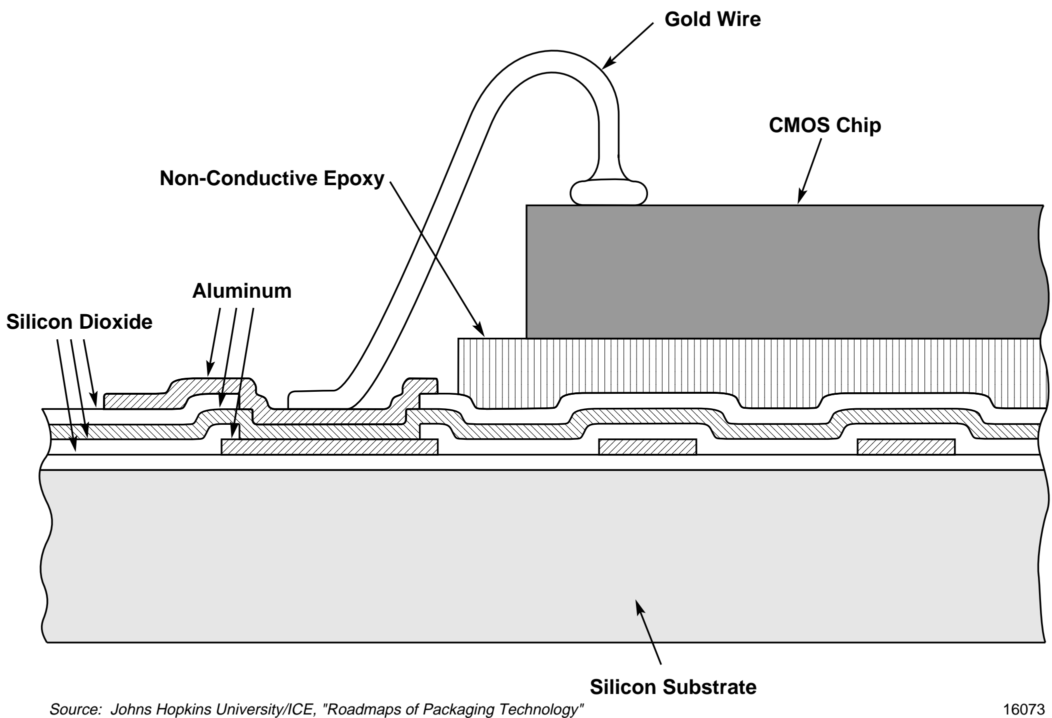
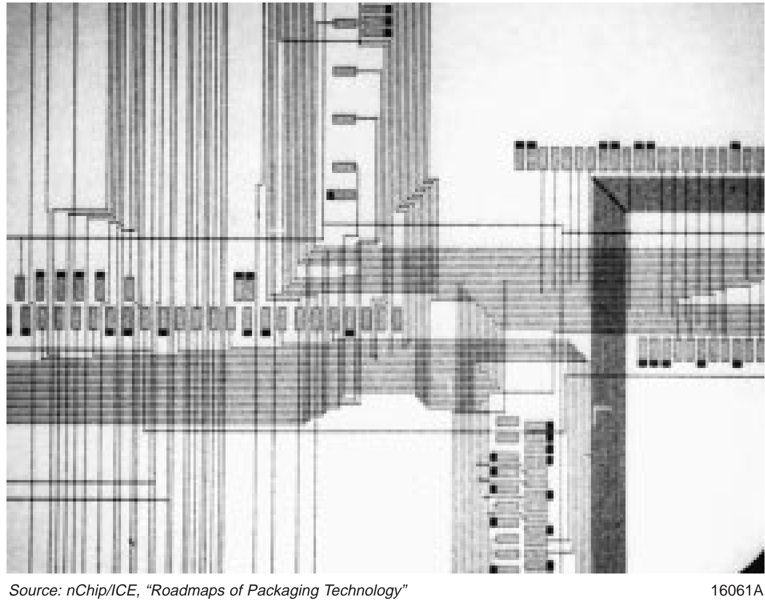


Figure 11-51. Sectional View of Aluminum/Silicon Dioxide Multilevel Substrate and CMOS Chip

When features are 2.5 microns or less, they are very sensitive to one micron and larger particles. With interconnect substrates, the effective "die" size is much larger than a typical IC, sometimes taking up the whole wafer. The yield issues associated with a "wafer-scale chip," using IC feature sizes, results in prohibitively expensive substrates.

The resistance per length of an aluminum trace, one micron thick and 2.5 microns wide, is 300 Ohms/in. If the dielectric were made thick enough to be a 50 Ohm characteristic impedance line, the wiring delay, including the interconnect RC delay, for a two inch trace would be about 3nsec. A printed wiring board trace 15 inches long would have a lower wiring delay. Reducing the delays requires lower resistance interconnects. One way to accomplish this is to make the lines wider and thicker. If the lines are wider, the dielectric must also be thicker to maintain a 50 Ohm characteristic impedance. IC technology is not well suited for applying thick dielectrics. There are stress cracking problems and, typically, poor planarization over thick conductors.

nCHIP has successfully developed a proprietary process of depositing planarizing SiO_2 dielectrics seven to ten microns thick, over conductors two microns thick. A top view is shown in Figure 11-52, and in cross section in Figure 11-53.

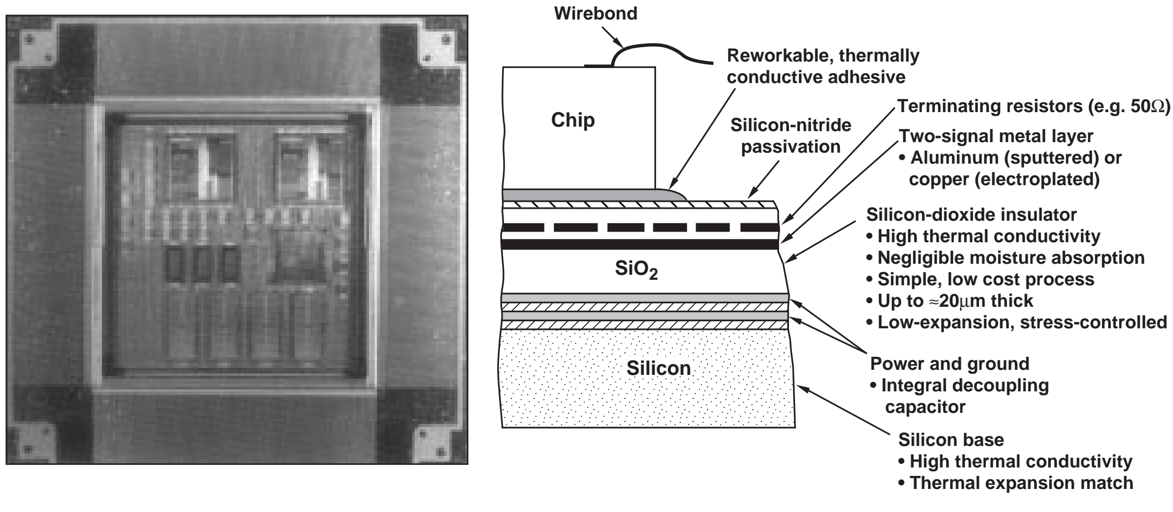


Source: nChip/ICE, "Roadmaps of Packaging Technology" 16061A

Figure 11-52. Top View of 10μm Lines on 25μm Pitch, Thin-Film Interconnect

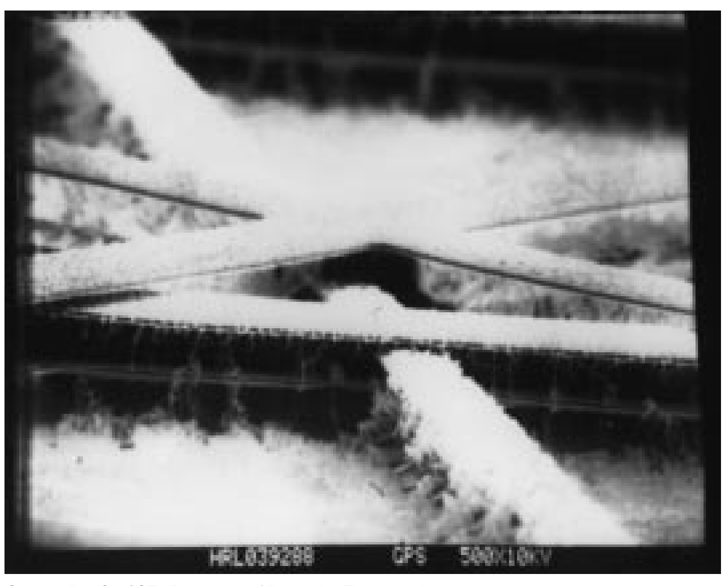
All other industry approaches involve the use of polymers. The advantage of polymers over conventional IC technology is their typically low dielectric constant, good planarizing ability and potentially low manufacturing costs. Figure 11-54 illustrates the planarizing abilities of Benzocyclcobutene (BCB) polymers.

In the last five years, advances have been made in the quality and reliability of polymer materials for use in thin film multilayer substrates. Polyimide and BCB are becoming the materials of choice. As photo-imageable versions of these materials are introduced into production, they have the potential of reducing fabrication costs.



Source: nChip/ICE, "Roadmaps of Packaging Technology" 19475A

Figure 11-53. nChip Silicon Circuit Board



Source: PolyCon/ICE, "Roadmaps of Packaging Technology" 16196

Figure 11-54. Multilayer Thin-Film Interconnect with the BCB Polymer Removed Using Plasma Etching

Basic Process And Capabilities

The basic steps in the process to fabricate a multilayer thin-film substrate are shown in Figure 11-55. Polymer dielectric layers are applied by spin coating. Polyimide layers are deposited, typically three microns thick, limited by the low viscosity. An advantage of Dow Chemical's BCB is its high viscosity and ability to be spin-coated to a thickness of 25 microns in one pass.

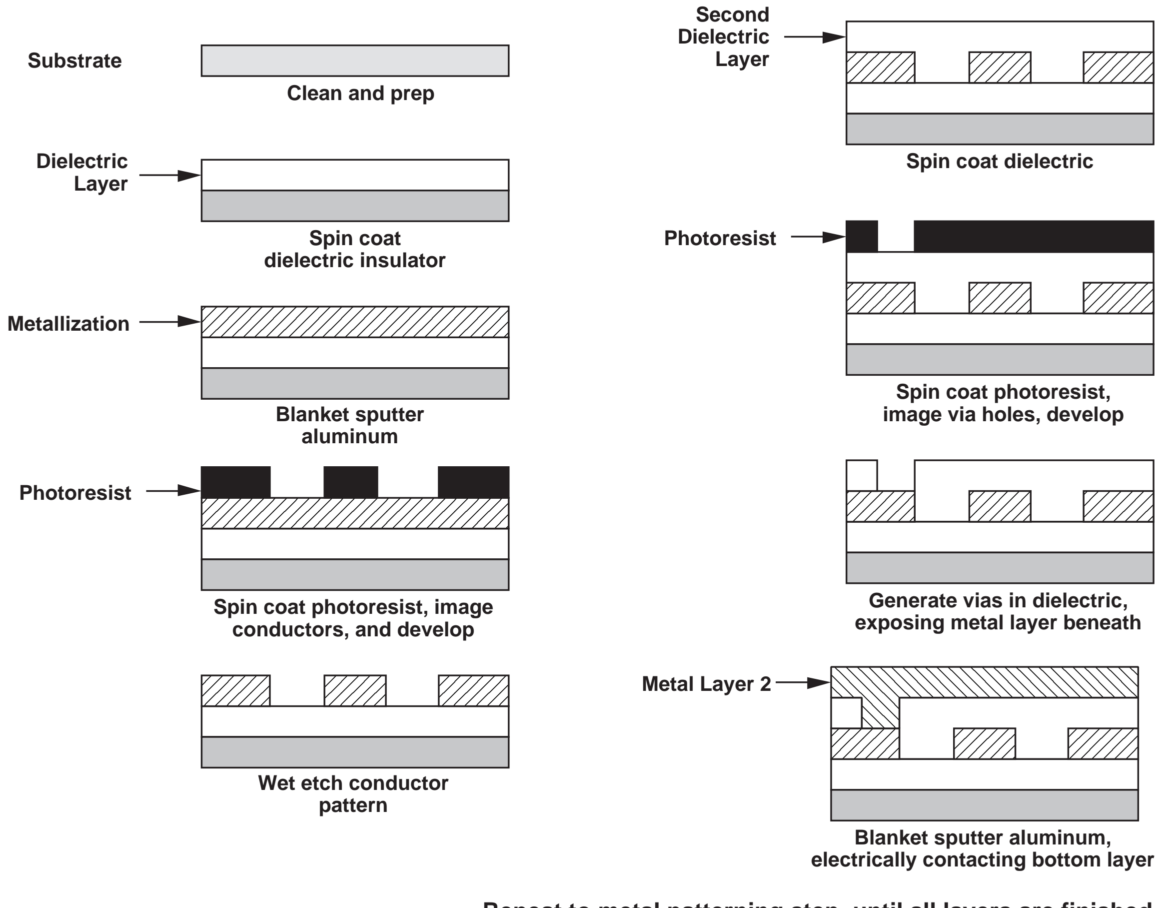


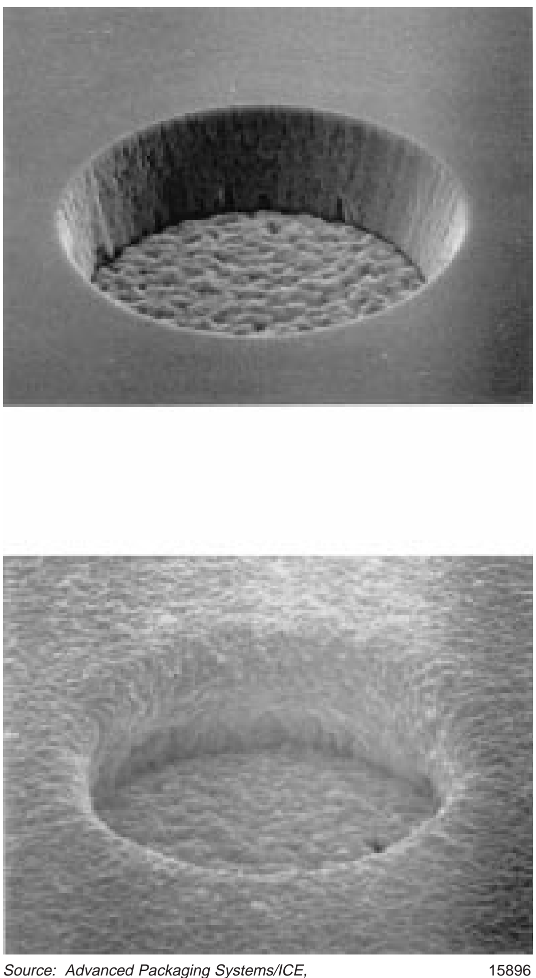
Figure 11-55. Thin-Film Process Sequence (Metal/Polyimide Process)

Vias are patterned in photoresist and typically the vias in the polyimide are plasma-etched in an oxygen plasma. A CF_4 gas is used for oxide etch. Wet etching has also been used.

After the vias have been opened up, exposing the underlying metallization, the next layer of conductor is blanket-deposited. This step connects the previous layer to the current layer. Figure 11-56 shows the aluminum metallization of such a via hole. In the AT&T AVP (Advanced VLSI Package) process, electroless nickel rather than aluminum is used to plate-up a solid post in the plasma-etched via hole.

The adhesion between most polyimides and copper is very poor, which can result in a potential reliability problem. For this reason, there is usually a glue metal layer between the copper and the polyimide. Chrome and titanium are most commonly used, and are applied to the top and bottom surfaces. Thus, the copper-polyimide structure is really a three-metal-layer structure. Typically,

the glue metal is blanket-coated, followed by the copper layer, followed by the top glue metal layer. All three metal layers are etched away to define the interconnect traces. This leaves the side walls of copper exposed to the polyimide.

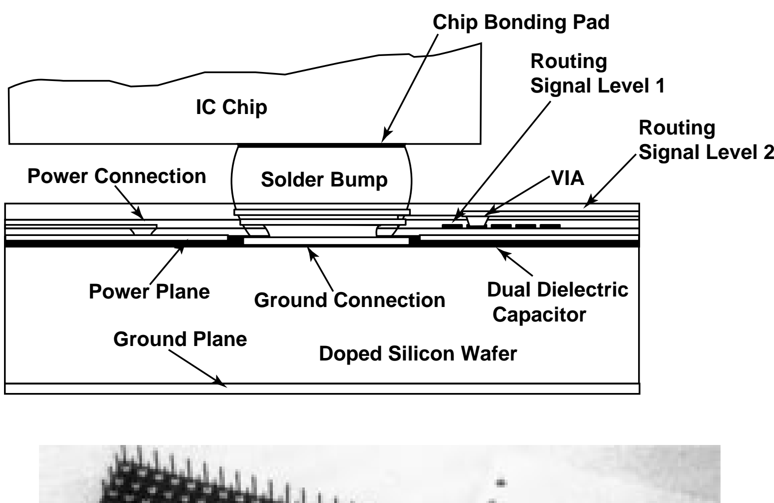


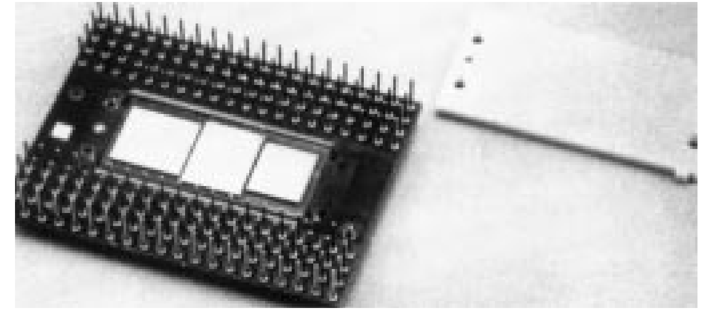
Source: Advanced Packaging Systems/ICE, "Roadmaps of Packaging" 15896

Figure 11-56. 35μ Via in Polyimide Before and After Metallization

In the AT&T AVP process, nickel is used as the barrier metal between the polyimide and the copper. After the flash coating of nickel and copper, the copper traces are pattern-plated to their full thickness, and electroless nickel is used to fully encapsulate the copper. Via holes are plated-up with electroless nickel to the top surface (Figure 11-57).

When a subtractive patterning method is used, for example with aluminum metallization, the entire surface is blanket-coated to the final thickness. Photoresist defines the metal interconnect patterns and metal in the exposed areas is etched away, usually by wet etch.





Source: AT&T/ICE, "Roadmaps of Packaging Technology" 12008

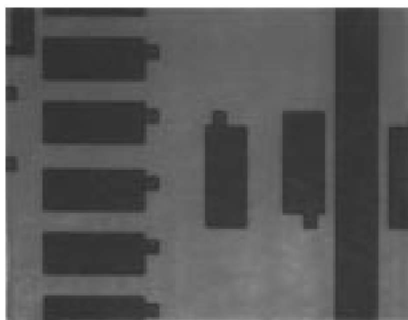
Figure 11-57. Silicon Substrate Packaging

In a semi-additive process with copper, a flash coating typically of nickel, chrome, or titanium is sputtered, followed by a thin sputtered layer of copper. The photoresist is applied to reveal traces and a pattern-plating process is used to build up the full conductor thickness. At the completion of this stage, the photoresist is stripped off and the flash layers are etched off, leaving just the patterned lines.

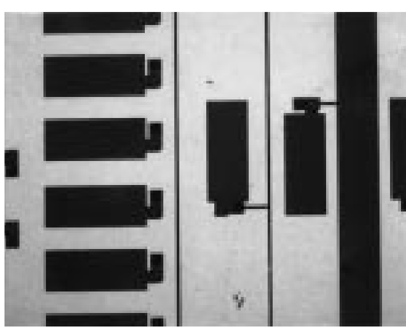
After the traces are defined, another layer of dielectric is spin-coated and the process repeats. Figure 11-58 shows the same region in a substrate as it goes through four metal-layer additions. In this way, each layer is grafted onto the one below it.

The top metal is typically aluminum, gold or solder. For gold metallization, barrier layers of chrome/nickel/gold are often used. Figure 11-59 shows a cross section of a five-metal-layer structure with aluminum buried traces and gold on top. Aluminum can be used for aluminum or gold wirebonding, and gold and solder can be used for conductive epoxy or solder attach of devices or leadframes.

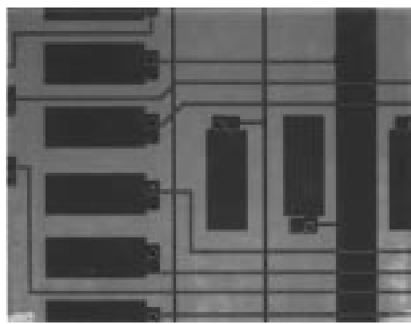
The linewidths currently in production or demonstrated in prototypes range from 10 microns to 25 microns.



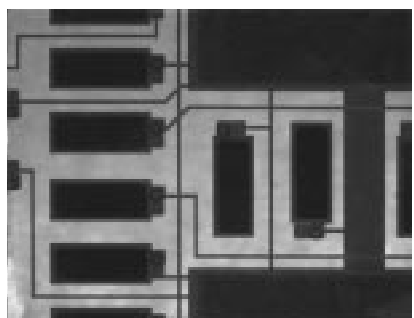
First Layer Metallization



Second Layer Metallization Added



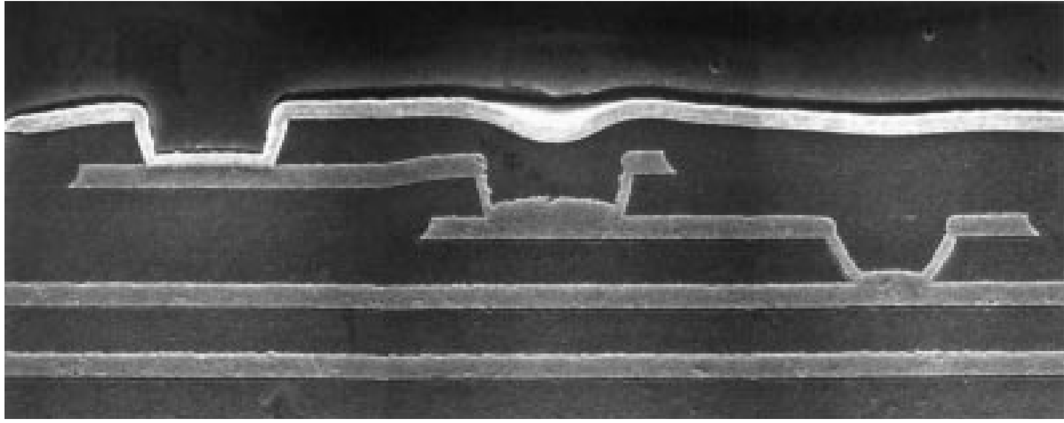
Third Layer Metallization Added



Fourth Layer Metallization (Complete)

Source: PolyCon/ICE, "Roadmaps of Packaging Technology" 22551

Figure 11-58. Top View, Four Metal Layer Thin-Film Substrate



Source: Advanced Packaging Systems/ICE, "Roadmaps of Packaging Technology" 15883

Figure 11-59. Cross Section of a Five-Layer Thin-Film Polyimide Substrate

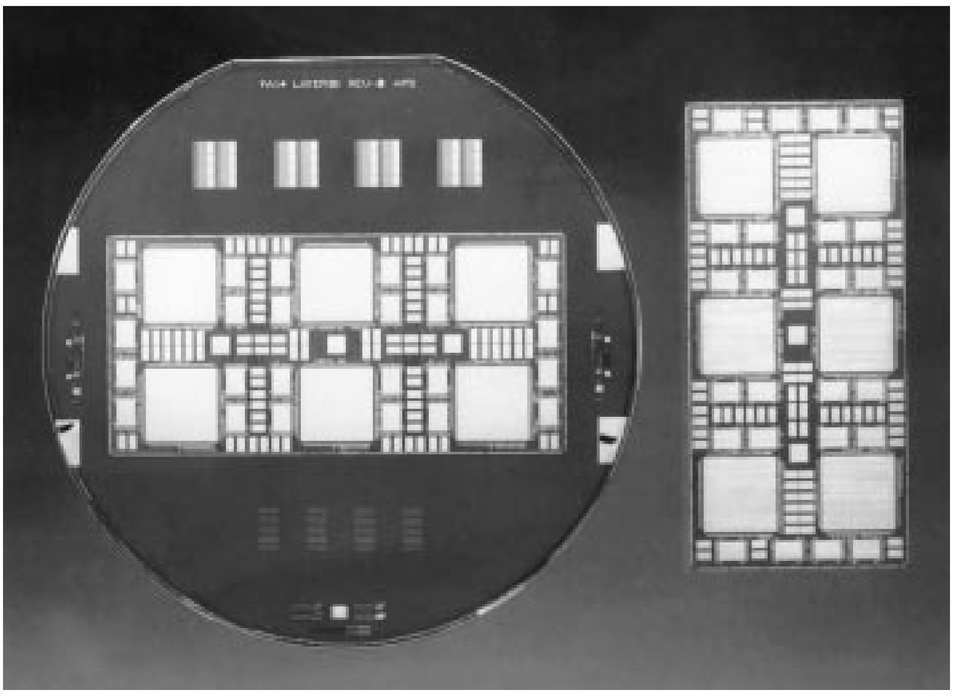
Substrates: Silicon, Ceramic, Or Cofired Ceramic

Thin-film multilayer technology is often called "silicon-on-silicon" packaging. In fact, exactly the same features can be fabricated on silicon as on ceramic, glass, and many other substrates. A variety of substrates have been analyzed and some have potential advantages over others for specialized applications. The most popular substrates are: silicon, thin-film ceramic, aluminum and cofired ceramic. Free-standing films, which are subsequently laminated to any substrate, have also been evaluated.

Silicon, thin-film ceramic, aluminum and cofired ceramic substrates offer some similar features:

- Mechanical compatibility with IC process equipment, when cut to a round format. Figure 11-60 shows an example of how a thin-film ceramic substrate can be made to look like a wafer when laser cut.

- A TCE that matches silicon well enough so that C4 can be used. They will all have the same problems under power cycling.



Source: Advanced Packaging Systems 15887

Figure 11-60. 125mm Round Ceramic Substrate and Diced Component

Other features that substrate materials should be compatible with include:

- Integrated capacitors and resistors
- Integrated active devices
- PGA or BGA format
- High thermal conductivity
- Power and ground planes
- Low cost—scalable to large area panels

Fabricating thin film on top of cofired ceramic poses two challenges. Typically the surface is rougher than thin-film ceramic, exhibiting mil-sized mountains and valleys. These will normally interfere with the lithography of fine lines. To provide a smooth surface, either a thick dielectric layer can be used to planarize the starting surface, or it can be smoothed by mechanical grinding and polishing. Alternatively, by carefully controlling the particle size of the cofired ceramic, the surface can be fabricated intrinsically smooth.

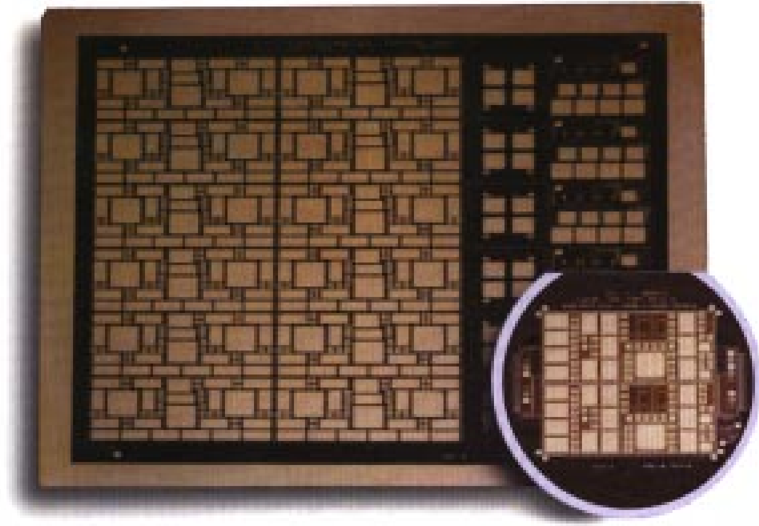
The second challenge is in the uncertainty of the shrinkage. Capture pads on the surface that are made to match with thin-film features must be large enough so that they will align even after worst-case shrinkage. For example, over a span of five inches, a ±0.2% uncertainty in shrinkage would result in a 10mil uncertainty in the center position of a pad. This may mean the smallest capture pad has to be at least 20mils in diameter. If the actual shrinkage uncertainty were ±0.75%, then the capture pad has to be at least 50mils in diameter.

All high end mainframe computer systems use the combination of multilayer low temperature cofired ceramic substrates with one or more layers of thin film metallization on top. Figures 11-46 and 11-47 are examples of LTCC substrates with layers of thin film on top, primarily used as redistribution layers for the fine pitch devices assembled on top.

The most important advance in thin film substrates in the last few years is the introduction of large area panels (LAP) in production. MMS and Hughes have introduced LAPs in production. An example of the panels from Hughes is shown in Figure 11-61. In the case of MMS, the panels are composed of aluminum metal. In the case of Hughes, the panels can be alumina (Al_2O_3), aluminum or glass. The use of large panels means the cost structure for thin film multilayer can approach the manufacturing costs of circuit boards, rather than be driven by the cost structure for ICs.

Added Features: Integrated Decoupling Capacitors

CMOS is especially sensitive to simultaneous switching noise. One feature that helps to minimize this is a low inductance decoupling capacitor across the power and ground planes, as close as possible to the leads of the chip. When the capacitor is integrated into the power and ground planes, it avoids the typical 1nH inductance associated with a surface mounted chip capacitor.



Courtesy of Hughes Microelectronics Division/ICE, "Roadmaps of Packaging Technology" 22547

Figure 11-61. Large Area Panel Used in the Hughes HDMI Thin-Film Process

In the silicon substrates used by AT&T and nCHIP, a thin-film decoupling capacitor is integrated into the substrate. AT&T uses a heavily n-doped wafer that is very conductive. The back side is ground and the top side has a thin layer of thermal oxide and silicon-nitride dielectric, followed by the power-layer metallization. This thin-film capacitor provides about 25nF/cm^2 of decoupling.

nCHIP uses a proprietary process to fabricate a thin-film decoupling capacitor (42nF/cm^2) on the base metal layer.

For over 25 years, AT&T has used tantalum-oxide thin-film capacitors with 90nF/cm^2 decoupling, in its single-layer, thin-film hybrids on ceramic substrate. These capacitors can be located on the starting substrate of its PolyHIC module, offering integrated decoupling capacitors.

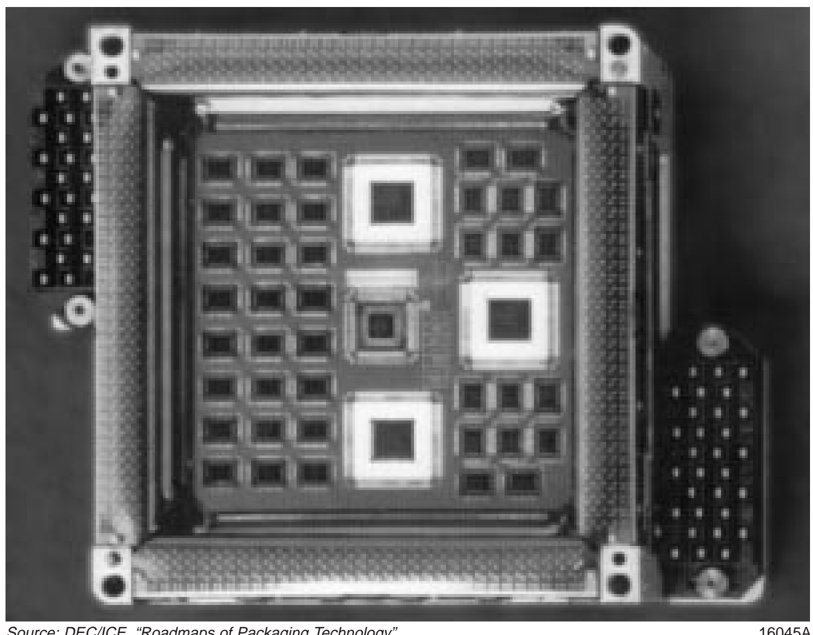
Added Features: Free Films

If the multilayer interconnect layers are removed from the substrate on which they are fabricated either by dissolving the base or using a release agent, a free-standing film can result. This concept has been used in flex circuits by Sandy Lebow in the past, has been exploited by DEC in the VAX 9000, and has been used by Polylithics in a unique application. It is also being considered to create cavity-up single chip BGA packages by MMS.

The VAX 9000 computer is designed with 35-watt ECL gate arrays. To provide adequate thermal spreading, the back of each die is mounted in direct contact with a copper heat spreader. To allow direct thermal contact, the polyimide interconnect layers are cut out from under the

dice. The copper-polyimide interconnect layers are fabricated using an aluminum disk as a sacrificial substrate. After the thin-film fabrication is completed, a stainless steel frame is glued to the perimeter of the top polyimide layer.

The interconnect free film is then removed from the substrate. The steel ring helps maintain the planar shape of the sheet. Regions where the dice would be mounted are cut out with a laser, and the free film is laminated to a copper heat spreader plate. In this way, the copper-polyimide layers provide the necessary high-density interconnect, while the copper substrate provides the thermal spreading. A photo of the VAX 9000 MCM is shown in Figure 11-62.



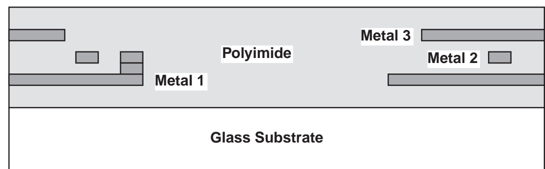
Source: DEC/ICE, "Roadmaps of Packaging Technology" 16045A

Figure 11-62. Multichip Module Used in VAX 9000 Super Computer

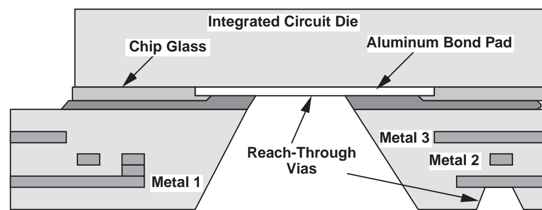
In the Polylithics process, the copper-polyimide, thin-film interconnects are fabricated on a glass disk substrate. After the completion of the thin-film fabrication, the dice are glued in place face down onto the interconnect with their pads aligned with the pads in the interconnect. Alignment is performed using optical inspection through the glass substrate.

A ceramic frame is glued around the chips to hold the free film in place after it is released from the glass. A free film of interconnect, mounted to a window frame of ceramic with chips glued to it, is the result. Holes are opened from the now-exposed back side of the free film that opens up the chip pads and connects them to the interconnect. This process is diagrammed in Figure 11-63.

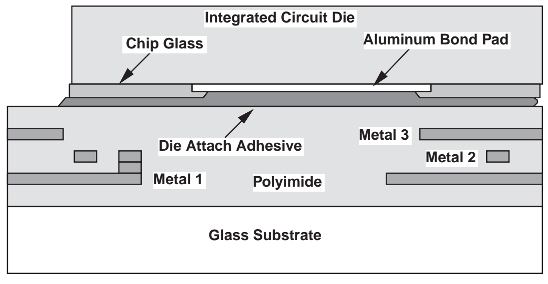
Step 1. Thin Film Manufacture



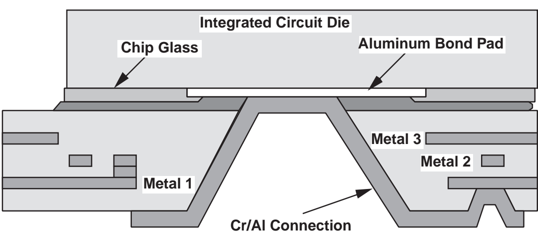
Step 3. Reach-Through Via Etch



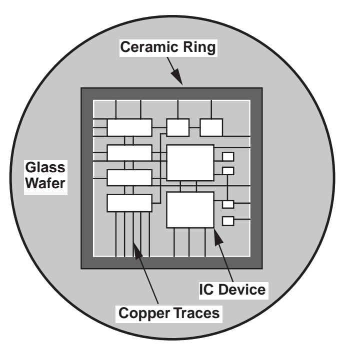
Step 2a. Chip Attachment



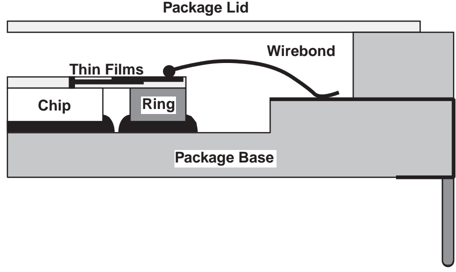
Step 4. Electrical Chip Connection



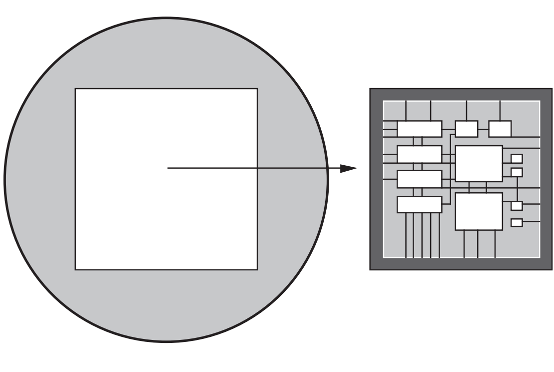
Step 2b. Ring Attachment



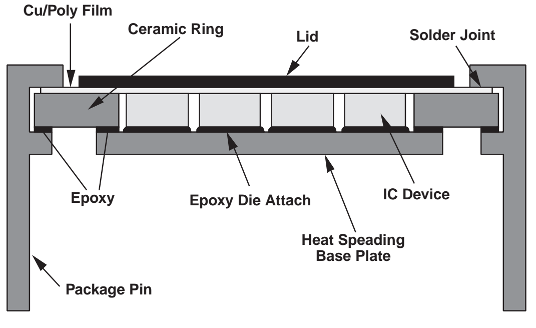
Step 5. Packaging - Ceramic



Step 2c. Release From Substrate



Step 5. Packaging - DIP



Source: Polylithics, Inc./ICE, "Roadmaps of Packaging Technology" 16215

Figure 11-63. Free-Standing, Thin-Film Multilayer Interconnect

Electrical Performance Limits: High Series Resistance

The benefit of fine lines is very high interconnect density. Unfortunately, the linewidth cannot shrink to finer and finer features without nature exacting a penalty. The penalty in this case is high series resistance, which affects wiring delay and signal integrity.

As the trace width, w, gets more narrow, and the metal thickness, t, is adjusted to be equal to the width (so the cross section is square), the resistance per length of a trace, R_L, increases rapidly:

$$R_L = \frac{\rho}{w^2}$$

where ρ is the metal resistivity.

For example, a 25 micron wide, 25 micron thick, copper trace has a resistance of about 0.8Ω/in. A 10 micron wide, 10 micron thick trace has a resistance of 5Ω/in. When the series resistance of a trace is a large percentage of the characteristic impedance of the line, it will significantly distort the rise time.

If the dielectric thickness is scaled to keep the characteristic impedance at about 50 Ohms, and the dielectric constant is on the order of 3.5, then the capacitance per length will always be approximately 3.1pF/in. The wiring delay, t_{wiring}, in propagating a length, L, due to the time of flight and series resistance and capacitance, will increase as the linewidth shrinks. When the metallization is copper and the cross section is square, the wiring delay variation with linewidth is given by:

$$T_{wiring} = \frac{\sqrt{\varepsilon_r}\ L}{12[in/nsec]} + R_L C_L L^2 = 0.16L + 1.6\frac{L^2}{w^2}[nsec]$$

with:

w in units of microns

and

L in units of inches

This relationship is shown graphically in Figure 11-64.

It should be noted that the resistivity of aluminum is 2.8μΩ-cm, compared with copper's 1.8μΩ-cm. For example, a copper trace 10 microns wide, 10 microns thick and 6 inches long will have a wiring delay of 1.5nsec. If the trace were 2.5 microns in width, the wiring delay for the 6 inch trace would be 10nsec. With these delays, the advantage of high-density interconnect is negated by very long electrical length. A printed circuit board 20 inches on a side would look electrically shorter than a 6 inch trace made from 2.5 micron wide metal!

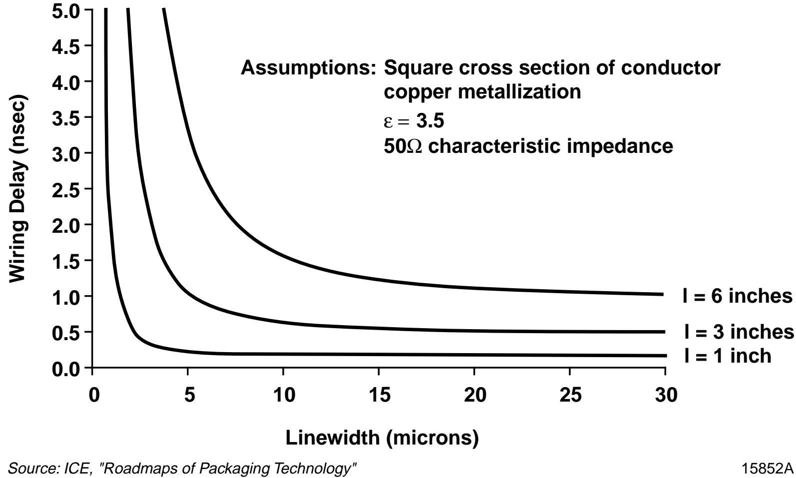


Figure 11-64. Wiring Delay of Thin-Film Interconnects

There is a limit to how fine a linewidth is practical for acceptable performance at room temperature. To obtain reasonable wiring delays yet high interconnect densities, other approaches will be needed such as: more than two signal layers, cryogenic cooling, superconductors, or 3-D packaging, as described in Chapter 13.

IMPS: Interconnected Mesh Power System

An intriguing design suitable for high density thin film structures that could reduce the layer count to only two layers was invented by Len Shaper at Univ. of Arkansas. Coined IMPS (interconnected mesh power system), it takes advantage of a sea of vias and an interwoven mesh of power and ground lines.

An example of the IMPS architecture is shown in Figure 11-65. On the bottom layer is an array of lines all going in the y direction. On the top layer is an array of lines all going in the x direction. Each line on the y layer alternates between being a power and a ground line. On the x layer, every other line alternates between being a power or ground line. Between each power line on the x layer and the y layer, a via is used to interconnect them. Likewise for the ground lines. The result is an interleaved mesh of power and ground lines that are continuous from one side of the substrate to the other.

Within this x-y grid, power and ground lines take up potential signal routing channels. When signals need to be routed, the power and ground lines in the way are removed and replaced by the signal lines. Signal lines see a pseudo-coplanar transmission line environment. An example of routed signals in the IMPS system is shown in Figure 11-66 and Figure 11-67.

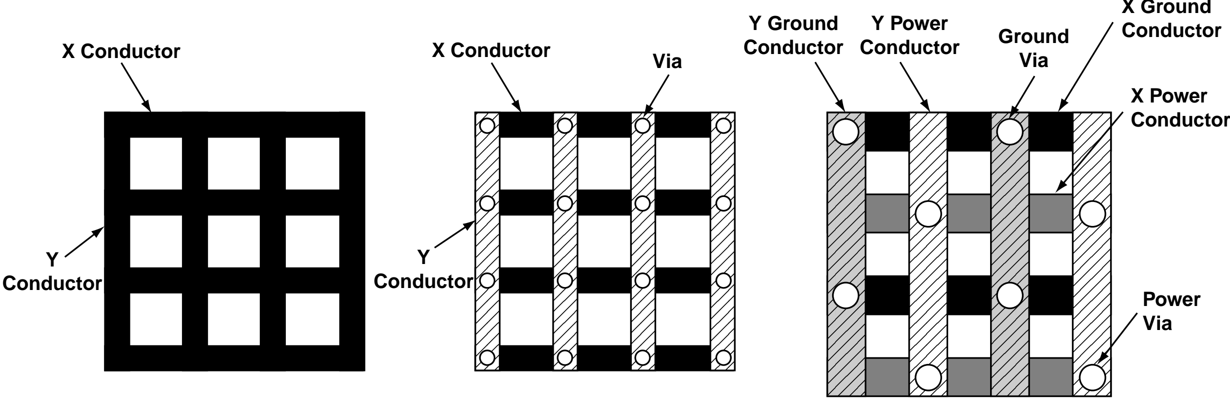


Figure 11-65. IMPS: Intermeshed Power System

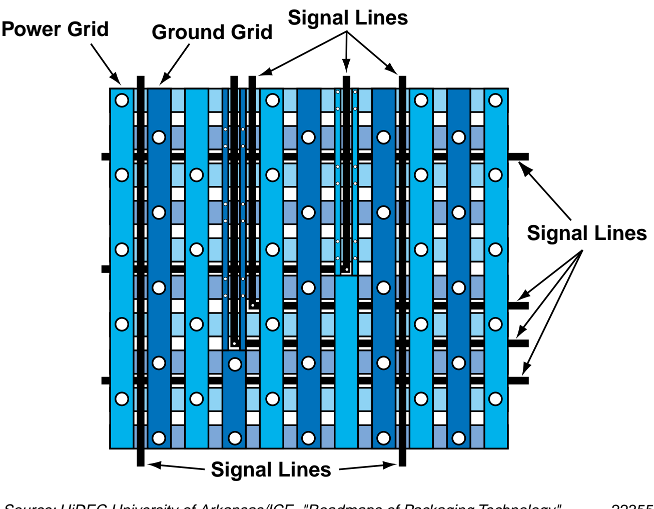


Figure 11-66. Dual Pitch IMPS

This approach can be cost effective when vias are fabricated in batch rather than one at a time, and when the interconnect density is not very high. With thin film technology, two layers of IMPS may enable a wide variety of applications that require a high density of surface pads.

BARE BOARD SUBSTRATE TEST—KNOWN GOOD SUBSTRATES

Traditionally, all circuit boards are tested for opens and shorts, or, in a more positive sense, continuity and isolation, after fabrication and before assembly of expensive surface mount components. When surface pads are on a 100mil grid or even 50mil grid in selected areas, it is possible to use a bed of nails to contact every pad, and with a system of relays, verify that all pads are connected that are on the same net and that no two nets are connected together.

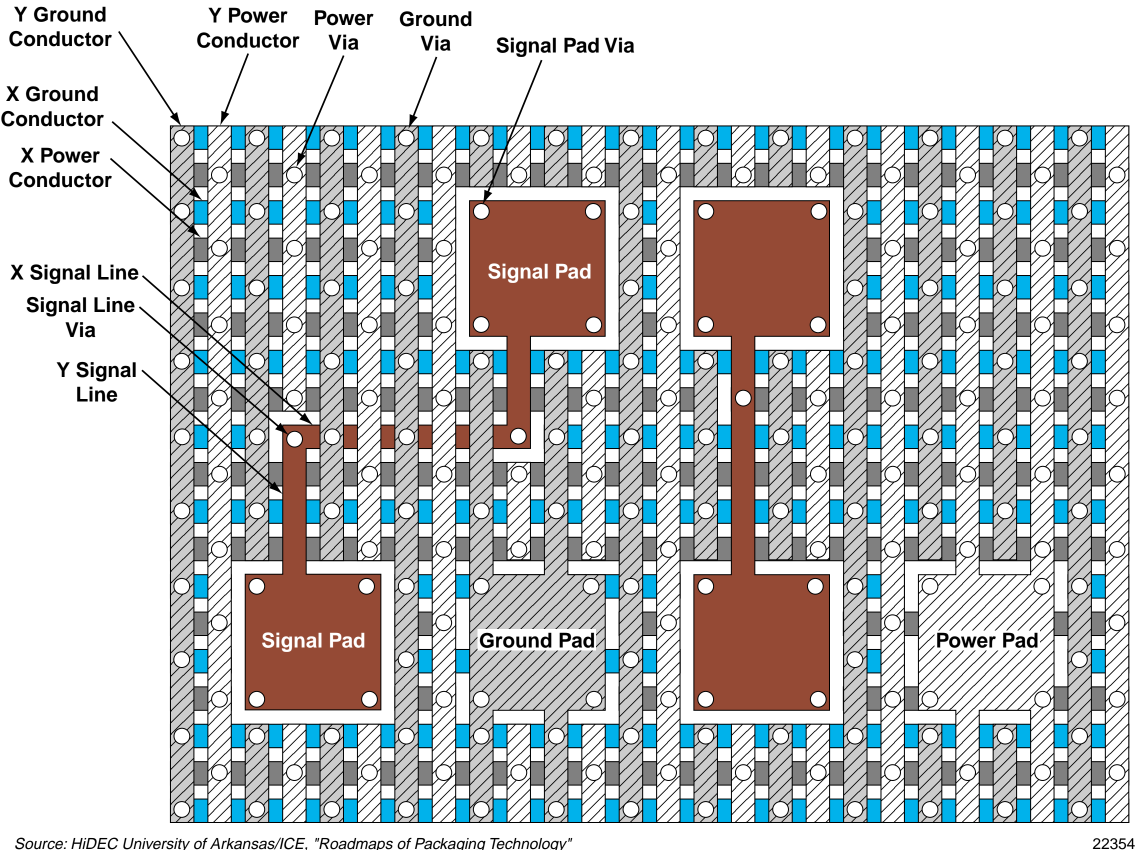


Figure 11-67. IMPS with Routing of Pads

Some boards can have over 10,000 pads that must be contacted. Testers are designed to handle even more than this number. An example of a bed of nails tester is shown in Figure 11-68.

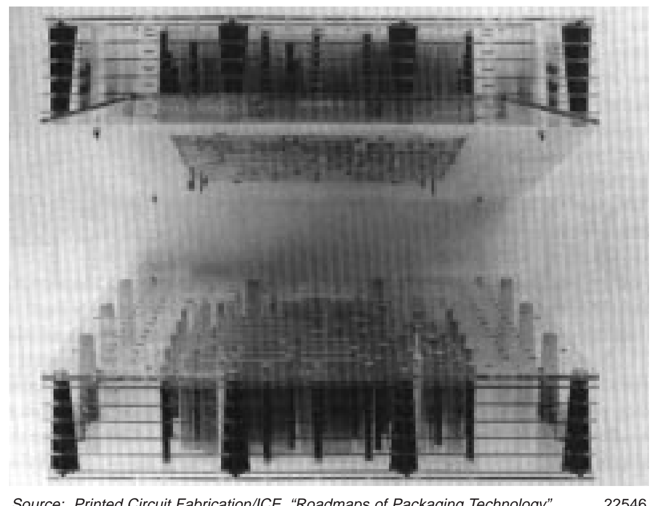


Figure 11-68. A Double-Sided Universal Grid System

However, as surface pad pitch drops below even 25mils, and the use of BGA, CSP and DCA increases, it becomes impossible to use a bed of nails to test an interconnect substrate. A promising new technique, based on capacitance testing has become commercially available. The principle is illustrated in Figure 11-69.

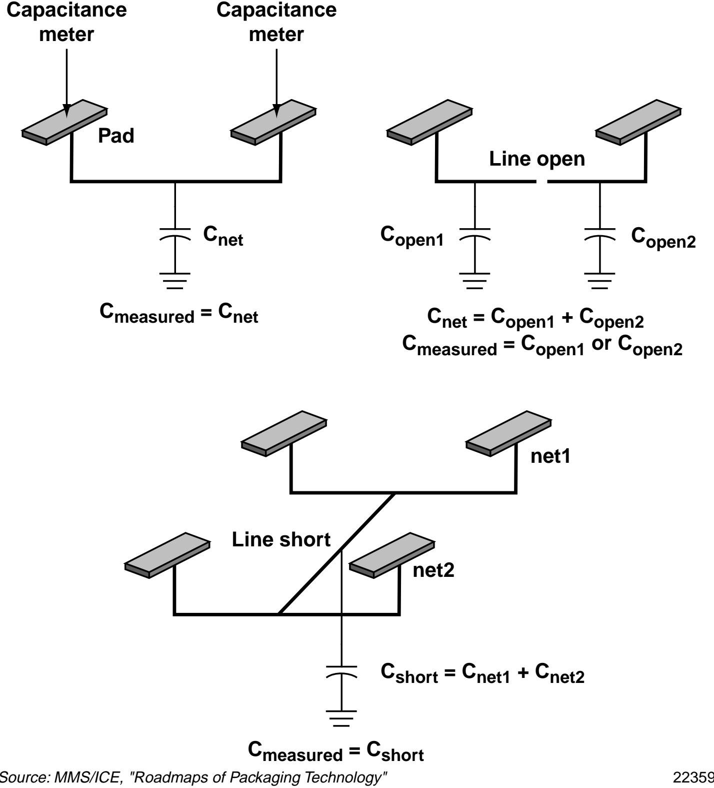


Figure 11-69. Principle of Capacitance Testing for Opens and Shorts

Consider two pads that are supposed to be connected to the same net. When the capacitance of each pad is measured relative to an internal ground plane, the same value should be measured on each pad. If there is an open in the net, both pads will show a lower value than they should, and in general, not the same. This will be an indication of an open. If there is a short between this net and another, the capacitance of the two shorted nets will be higher than either should be.

By using a single flying head probe, measuring the capacitance of each pad, and comparing the values to a look-up table, opens and shorts can be identified. Figure 11-70 is an example of all the measured capacitances of the pads on a thin film multilayer substrate, compared with the high and low values expected for each net. This shows a few capacitances that are much higher than they should be, corresponding to two nets that were shorted, and a few values that are lower than they should be, corresponding to nets that have opens.

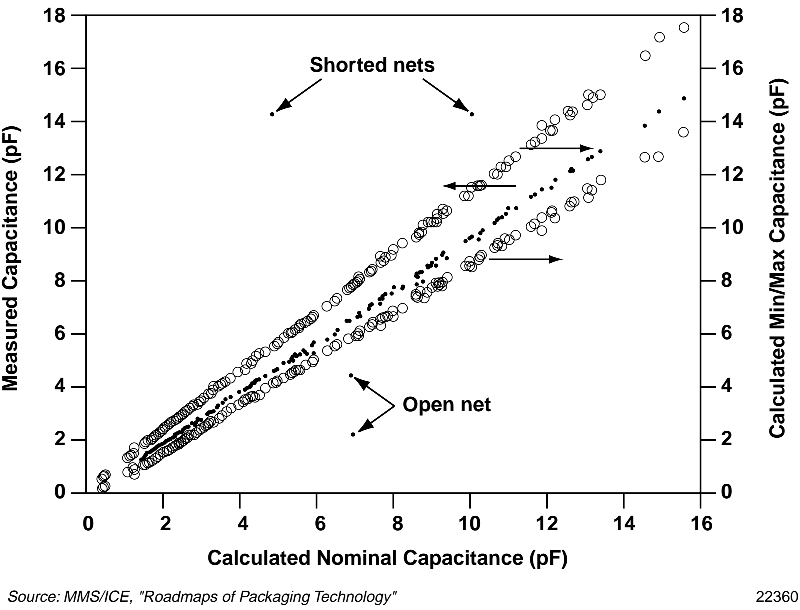
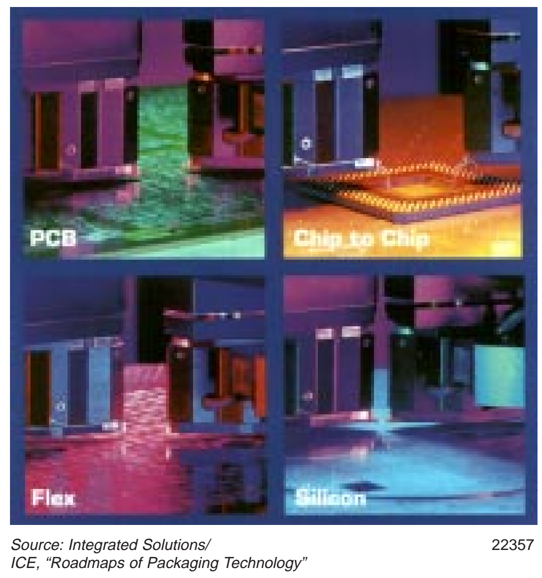


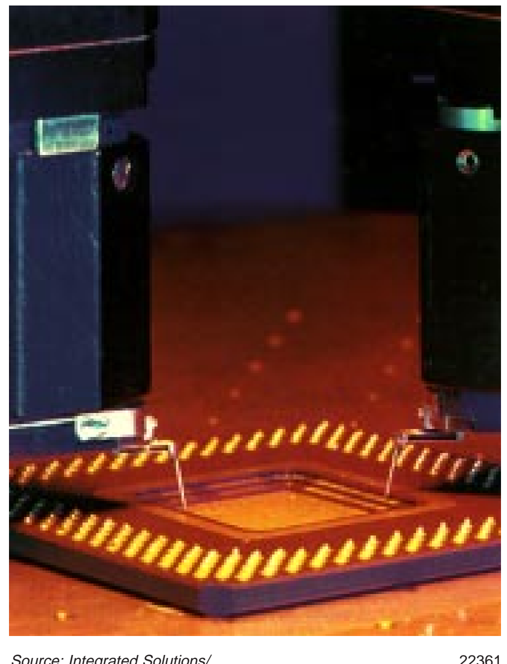
Figure 11-70. Using Capacitance to Identify Opens and Shorts

Figure 11-71 is a close up of a flying head prober from Integrated Solutions Inc. Depending on the test, 10 to 100 pads can be probed per second! Versions are available that can also test resistance with two probes, as shown in Figure 11-72. Even large area circuit boards can be tested with this technique, as shown in Figure 11-73. This type of testing will be an essential enabling element for the successful implementation of the next generation of higher and higher density substrates.



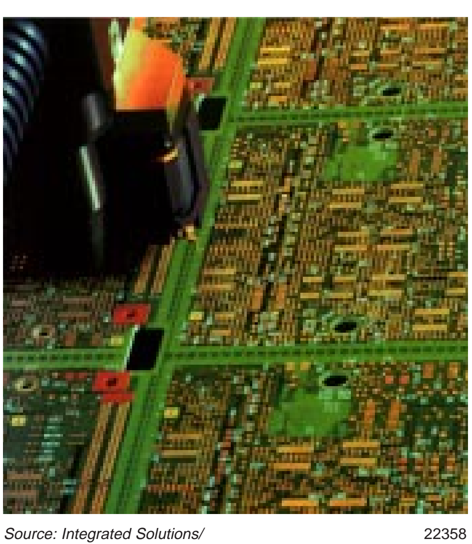
Source: Integrated Solutions/
ICE, "Roadmaps of Packaging Technology" 22357

Figure 11-71. Flying Head Probing of Fine Line Substrates



Source: Integrated Solutions/ ICE, "Roadmaps of Packaging Technology" 22361

Figure 11-72. Dual Probe Heads for Capacitance and Resistance Testing



Source: Integrated Solutions/ ICE, "Roadmaps of Packaging Technology" 22358

Figure 11-73. Flying Head Capacitance Testing of a Large Board