E / EEPROMs

We may be approaching the time when it’s appropriate to say “stand back, here comes FLASH.” We saw two 32Mbit devices and both include examples of very up-to-date technology, including the 0.25 micron gates on the Toshiba device. Also, the two-bit per cell capability seems to be getting very near! There just seems to be no way this product type can be excluded from any new technology developments. Almost everything developed for any other class of products should be useable by FLASH. Even the UVEPROMs are at the 0.5 micron gate length stage now.
# Horizontal Dimensions (Design Rules)

## E/EEPROMs

<table>
<thead>
<tr>
<th></th>
<th><strong>SANDISK</strong></th>
<th><strong>TOSHIBA</strong></th>
<th><strong>SGS-THOMSON</strong></th>
<th><strong>AMD</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>E/EEPROMs</td>
<td>34Mb Flash EEPROM 1996</td>
<td>TC5832FT 32Mb (x8) NAND EEPROM 9528</td>
<td>M27C1001-15F1 1Mb (x8) UVEPROM 9514</td>
<td>AM27C010-200DC 1Mb (x8) UVEPROM 9634</td>
</tr>
<tr>
<td>Die size</td>
<td>9.1 x 13.3mm (121mm^2)</td>
<td>14.7 x 7mm (103mm^2)</td>
<td>3.4 x 3.4mm (11.5mm^2)</td>
<td>3.7 x 4.3mm (15.9mm^2)</td>
</tr>
<tr>
<td>Min. M1 width/space</td>
<td>0.75μm/0.9μm</td>
<td>0.7μm/0.6μm</td>
<td>1.3μm/1.0μm</td>
<td>1.2μm/1.1μm</td>
</tr>
<tr>
<td>Min contact (Met. to Si)</td>
<td>0.8μm*</td>
<td>1.0μm</td>
<td>0.7μm*</td>
<td>1.0μm*</td>
</tr>
<tr>
<td>Min. Poly 3</td>
<td>1.0μm</td>
<td>0.5μm*</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Min. Poly 2</td>
<td>0.35μm</td>
<td>0.25μm</td>
<td>0.5μm*</td>
<td>0.7μm*</td>
</tr>
<tr>
<td>Min. Poly 1</td>
<td>0.6μm</td>
<td>0.25μm</td>
<td>0.5μm</td>
<td>0.7μm</td>
</tr>
<tr>
<td>Min. gate-(N)†</td>
<td>1.0μm</td>
<td>0.25μm</td>
<td>0.5μm</td>
<td>0.8μm</td>
</tr>
<tr>
<td>Min. gate-(P)†</td>
<td>1.0μm</td>
<td>0.6μm</td>
<td>0.5μm</td>
<td></td>
</tr>
<tr>
<td>Cell pitch</td>
<td>1.1μm x 1.6μm</td>
<td>0.85μm x 1.5μm</td>
<td>1.8μm x 1.95μm</td>
<td>2.3μm x 2.4μm</td>
</tr>
<tr>
<td>Cell area</td>
<td>1.8μm^2</td>
<td>1.3μm^2</td>
<td>3.5μm^2</td>
<td>5.5μm^2</td>
</tr>
</tbody>
</table>

* Polycide  † Physical gate length  ‡ Plugs

Table 3-1
### VERTICAL DIMENSIONS

<table>
<thead>
<tr>
<th>E/EEPROMs</th>
<th>SANDISK 34Mb Flash EEPROM 1996</th>
<th>TOSHIBA TC5832FT 32Mb (x8) NAND EEPROM 9528</th>
<th>SGS-THOMSON M27C1001-15F1 1Mb (x8) UVEPROM 9514</th>
<th>AMD AM27C010-200DC 1Mb (x8) UVEPROM 9634</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final passivation</td>
<td>0.45(\mu)m</td>
<td>1(\mu)m</td>
<td>0.75(\mu)m</td>
<td>0.6(\mu)m</td>
</tr>
<tr>
<td>Metal 1</td>
<td>0.8(\mu)m</td>
<td>0.9(\mu)m</td>
<td>0.75(\mu)m</td>
<td>1.0(\mu)m</td>
</tr>
<tr>
<td>Pre-metal dielectric</td>
<td>0.5(\mu)m</td>
<td>1.1(\mu)m</td>
<td>0.5(\mu)m</td>
<td>0.6(\mu)m</td>
</tr>
<tr>
<td>Poly 3</td>
<td>0.2(\mu)m</td>
<td>0.3(\mu)m*</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Poly 2</td>
<td>0.3(\mu)m</td>
<td>0.2(\mu)m</td>
<td>0.5(\mu)m*</td>
<td>0.3(\mu)m*</td>
</tr>
<tr>
<td>Poly 1</td>
<td>0.25(\mu)m</td>
<td>0.15(\mu)m</td>
<td>0.15(\mu)m</td>
<td>0.15(\mu)m</td>
</tr>
<tr>
<td>Recessed oxide</td>
<td>0.45(\mu)m*</td>
<td>0.4(\mu)m</td>
<td>0.45(\mu)m</td>
<td>0.4(\mu)m</td>
</tr>
<tr>
<td>N-well</td>
<td>3(\mu)m</td>
<td>3.0(\mu)m</td>
<td>4.5(\mu)m</td>
<td>4.5(\mu)m</td>
</tr>
<tr>
<td>P-well</td>
<td>?</td>
<td>10(\mu)m</td>
<td>?</td>
<td>?</td>
</tr>
<tr>
<td>Epi</td>
<td>8(\mu)m</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>

* Polycide
*<sup>1</sup> Could not delineate
*<sup>2</sup> Non-recessed

Table 3-2
## Die Materials

### E/EEPROMs

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Device Details</th>
<th>Final Passivation</th>
<th>Metal 1</th>
<th>Plugs</th>
<th>Reflow Glass</th>
<th>Polycide Metal</th>
</tr>
</thead>
<tbody>
<tr>
<td>SANDISK</td>
<td>34Mb</td>
<td>Nitride</td>
<td>Titanium-Nitride</td>
<td>Tungsten</td>
<td>BPSG</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td>Flash EEPROM 1996</td>
<td></td>
<td>Aluminum</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOSHIBA</td>
<td>TC5832FT 32Mb (x8) NAND EEPROM 9528</td>
<td>undoped glass</td>
<td>Titanium-Nitride</td>
<td>NA</td>
<td>BPSG + TEOS(?)</td>
<td>Tungsten</td>
</tr>
<tr>
<td>SGS-THOMSON</td>
<td>M27C1001-15F1 1Mb (x8) UVEPROM 9514</td>
<td>glass</td>
<td>Titanium-Nitride</td>
<td></td>
<td>BPSG</td>
<td>Tungsten</td>
</tr>
<tr>
<td>AMD</td>
<td>AM27C010-200DC 1Mb (x8) UVEPROM 9634</td>
<td>glass</td>
<td>Titanium-Nitride</td>
<td></td>
<td></td>
<td>Tungsten</td>
</tr>
</tbody>
</table>

Table 3-3
TECHNOLOGY DESCRIPTION

SANDISK
34Mbit CMOS FLASH EEPROM

Introduction

Ref. report SCA 9611-471

These dice were obtained from a 15 CF (“COMPACTFLASH”) Flash card. One 15Mbyte and one 10Mbyte FLASHCARD was received for the analysis. The dice analyzed were 34Mbit devices. No information on speed, organization or power requirements was available. It is believed that dice were fabbed early in 1996.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Important/Unique Features

– Non-recessed field oxide isolation.

– Tungsten plugs used at all contacts.

– Three poly unique Flash EEPROM cell design.

Quality

Quality of the process implementation was good. We found no items of serious concern.

In the area of layer patterning, etch definition and control were both good.

Alignment and registration were also good.

Technology

These devices were manufactured by a non-recessed field oxide, CMOS (possibly twin-well) process in a P-epi on a P substrate. One level of metal and three levels of poly were present.

Passivation consisted of a thick layer of nitride and was not planarized.
The single level of metal was defined by a standard dry-etch technique. Metal consisted of aluminum with a titanium-nitride cap (no barrier was visible).

Tungsten plugs were used for all vertical interconnect. Plugs appeared to be lined (underneath only) with titanium-nitride liners.

Pre-metal dielectric was a single layer of reflow glass (BPSG) over various densified oxides. This layer was reflowed prior to contact cuts, and provided the only planarization. No SOG was used anywhere in the process.

Three layers of poly (no silicide) were used in the cell array. It is probable that poly 3 is also used to form all standard gates on the die; however, it was impossible to positively identify the gate poly as poly 3, and it is possible that gates are made with a fourth level of poly.

Oxide sidewall spacers were present and were left in place, but an LDD process was not used (according to Sandisk). Apparently, standard source/drain diffusions were implanted in peripheral circuits, but a separate non-self-aligned diffusion formed the sources/drains in the memory cells.

Direct poly to diffusion (buried) contacts were not used.

Field oxide isolation consisted of a non-recessed (deposited and densified) oxide that was well implemented. A step in this oxide was present at well boundaries but no sign of the presence of twin-wells was found. An epi layer was present.

Redundancy fuses were not present.

**Memory Cell Structures**

The Flash cell design employed three levels of poly, a non self-aligned bit line diffusion, and no nitrides for the thin dielectrics. It was noted that the thick non-recessed field oxide provides for minimum spacing between the poly 1 elements. It should be mentioned that although peripheral gates measured only 1 micron in length (not very aggressive), the memory array uses 0.35 micron wide poly 2 lines and 0.6 x 0.9 micron poly 1 pads with 0.4 micron spacing. The EEPROM cell size was 1.8 microns².

Overall minimum feature size measured anywhere on these dice was the 0.35 micron (poly 2 in cell).
Packaging/Assembly

As mentioned, these EEPROM dice were obtained from a 15 CF (“COMPACTFLASH”) Flash card.

The 15Mbyte FLASHCARD employed five dice (one controller die and four 34Mbit Flash EEPROM dice) mounted on printed circuit boards along with various surface mount devices. All EEPROM dice were embedded in an epoxy encapsulant. The controller die was packaged in a standard 100-pin Plastic Quad Flat Pack (PQFP) and mounted on the PC board.

The standard thermosonic wirebonds on the die were made to pads on the die that had a pitch of 250 microns with 140 micron spacing and all placed along one edge of the die. Pads were 110 microns wide with a 100 micron windows.

No die coat was present.
Optical photographs of the SanDisk 15M Compactflash Flash Card.
Whole die photograph of the SanDisk 505032A 34Mbit EEPROM. Mag. 17x.
SEM section views of general construction.

Mag. 10,000x

Mag. 5000x, 60°
Perspective and section views of the Flash EEPROM cells.
TECHNOLOGY DESCRIPTION

TOSHIBA TC5832FT
32Mbit CMOS NAND EEPROM

Introduction

Ref. report SCA 9604-458

These parts were packaged in 44-pin format (40 pin) plastic Thin Small Outline Packages (TSOPs). They were engineering samples (marked ES). They are organized in a 528 x 8K x 8 array (528 byte page), offer a 10nsec. maximum access time and operate from a single 5V power source. They were date coded 9528 (week 28 of 1995).

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Important/Unique Features

– Single metal, three poly, twin/nested well CMOS process.

– Shallow extended source/drains.

– Use of at least three different gate oxides plus the interpoly dielectric.

– Smallest cell size seen in 1996!

Quality

Quality of the process implementation was good, except at metal contacts where aluminum thinning greater than 95 percent was noted. These devices would really benefit from a tungsten plug addition.

In the area of layer patterning, etch definition and control were both good.

Alignment and registration were also good.

Technology

The devices were manufactured by a twin (multiple)-well, selective oxidation CMOS process employing an N-substrate (no epi), one level of metal, and three levels of poly.
Passivation consisted of two layers of undoped glass, which varied greatly in thickness due to the large metal steps.

They incorporated a single level of metal defined by a standard dry-etch technique. Metal consisted of aluminum with a titanium-nitride barrier (no cap was visible). It should be noted that poly 3 (tungsten polycide) functioned as a metal interconnect also.

Standard contacts were employed throughout (no plugs), and represent a feature hopefully eliminated in the full production devices.

Pre-metal dielectric 2 (between metal and poly 3) appeared to be a layer of BPSG reflow glass used for planarization. A first thick layer of BPSG reflow glass (pre-metal dielectric 1) was used for planarization under poly 3. No spin-on-glass (SOG) was used anywhere.

Three levels of polysilicon were used. Polycide 3 (poly and tungsten silicide) was used as a metal substitute in both the array and peripheral circuit areas. Poly 2 formed all gates for the peripheral circuits and the word (control) lines in the cell array. Poly 1 was employed only in the cell array (for all floating gates). A separate (third) gate oxide was used under all poly 2 gates in the periphery.

Sidewall spacers had been used throughout and removed.

Implanted source/drain diffusions included shallow LLD extensions plus deep diffusions at metal contacts. Diffusions were not silicided.

Direct poly to diffusion contacts (buried contacts) were used only in the cell array for the polycide (poly 3) bit line contacts.

Standard recessed field oxide isolation (LOCOS) was used and was well implemented. A step was present at the top of the LOCOS only.

Redundancy fuses were not present.

Memory Cell Structures

The EEPROM array used the standard dual gate stacked cell implemented in a NAND configuration. Separate program lines were present at the edge of each end of the 16-bit string (for “Flash” programming?). These program gates used a continuous poly 1 line under the poly 2, a different gate oxide under the poly 1, the same ONO between poly 1 and 2, and wider poly 1
and 2 (gate length) than the memory gates. Polycide (poly 3) was used for all bit lines. The memory cell gates themselves are arranged in strings of 16 cells, use a different gate oxide than either the control cells or the peripheral circuit gates, use an ONO between poly 1 and poly 2 and are the shortest gates anywhere on the dice. The EEPROM cell size was 1.3 micron², by far the smallest cell size we’ve ever seen. However, this dimension does not include the overhead due to the special control lines, etc. But, if the array is measured and divided by the number of memory bits, the cell size is 1.68 micron² - still the smallest cell size seen in 1996!

Overall minimum feature size measured anywhere on these dice was the 0.25 micron poly 1 and 2 (gates in cell).

**Packaging/Assembly**

As mentioned, these parts were packaged in 44-pin format (40 pin) plastic Thin Small Outline Packages (TSOPs) date coded 9528. They used a hollow center leadframe paddle, silver epoxy die attach, and standard thermosonic wirebonding employing gold wire.

Wirebond pads on the die had a minimum pitch of 665 microns with 550 micron spacing. Pads were 115 microns wide with a 105 micron windows.

No die coat was present.
Whole die photograph of the Toshiba TC5832. Mag. 16x.
SEM views of the general die structures.
SEM views of memory cells in section.
TECHNOLOGY DESCRIPTION

SGS-THOMSON M17C1001-15F1
1Mbit CMOS UVEPROM

Introduction

The parts were packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs) with a quartz window. These were fully functional production devices organized in an 128K x 8 design. They offer a fast access time of 45 nsec., a low power standby mode, electronic signature, operate from a 5V power source but require a 12.75V programming voltage. They were date coded 9514 (week 14 of 1995).

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Important/Unique Features

– Unusual metal interconnect.

– Aggressive design rules (0.5 micron gates).

Quality

Quality of the process implementation was very good. We found no areas of concern.

In the area of layer patterning, etch definition and control were both good.

Alignment and registration were also good.

Technology

These devices were manufactured by a twin-well, selective oxidation CMOS process on a P substrate (no epi). A single level of metal and two levels of poly were used.

Passivation consisted of two layers of silicon-dioxide and was not planarized.

Ref. report SCA 9612-518
They incorporated a single level of metal defined by standard dry-etch techniques. Metal consisted of aluminum with a titanium-nitride cap and titanium over titanium-nitride on titanium barrier. The presence of the titanium layer over the titanium-nitride barrier is unique. This layer is deposited after plug formation thus covering the tops of the plugs which normally is done with a titanium-nitride.

Tungsten plugs were used at all contacts, and were lined underneath with titanium-nitride.

Pre-metal dielectric was a single layer of reflow glass (BPSG) over densified oxides. This layer was reflowed prior to contact cuts, and it provides the only planarization as no SOG was used anywhere in this process.

Two levels of polysilicon were used. Poly 2 (tungsten silicide) was used to form all gates on the die and the select/word lines in the EPROM cell array. All gates in the periphery used oxide sidewall spaces that were left in place. Poly 1 (no silicide) was used exclusively in the memory cells to form the floating gates.

Standard implanted source/drain diffusions were used in the peripheral circuits and they included an LDD process. Salicide was not used. Other implants were present in the memory array (see below).

The process appears to use three different thin oxide dielectrics. One for gate oxide in peripheral circuits, one for gate oxide in the memory array and one for the interpoly in the array.

Interpoly or buried contacts were not used, nor was any other special interconnect such as a local interconnect.

Standard LOCOS isolation was employed and well implemented. A step was present confirming the presence of twin-wells.

Redundancy fuses were not present.

**Memory Cell Structures**

Memory cells consisted of a standard dual gate stacked poly EPROM design. Metal was used for the bit lines. Poly 2 was used to form the word/select lines, and poly 1 was used exclusively to form the floating gates. As mentioned, oxide was used as the interpoly dielectric. The gates used for the memory cells were very small, measuring 0.5 micron long and only 0.4 micron wide. The EPROM cell size was 3.5 microns², which is the smallest cell size we’ve seen for a
UVEPROM cell. Sidewall spacers were left only on the bit contact side of the memory cell gates where they appear to have provided the masking for the deep contact diffusions.

Overall minimum feature size measured anywhere on these dice was the 0.5 micron gates in the cell array.

**Packaging/Assembly**

As mentioned, the parts were packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs) with quartz windows. Aluminum ultrasonic wirebonds were employed.

The die was mounted to the cavity floor with silver-filled glass die attach. Wirebond pads on the die had a pitch of 170 microns with 30 micron spacing. Pads were 140 microns wide with 130 micron windows.
Whole die photograph of the SGS M27C1001. Mag. 50x.
SEM section and perspective views of general structure.
SEM section views of the memory cell array. Mag. 13,000x.
TECHNOLOGY DESCRIPTION

AMD AM27C010
1Mbit CMOS UVEPROM

Introduction

Ref. report SCA 9612-517

The parts were packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs) with quartz windows. These were fully functional production devices organized in a 128K x 8 design. They offer a fast access time (55 nsec), a static standby mode and operate from a 5V power source but require a 12.75V programming voltage. They were coded 9634 (week 34 of 1996).

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

– Twin-well CMOS with tungsten plugs.
– Sub-micron gate lengths (0.7 micron).
– ONO dielectric used in array cells.

Quality

Quality of the process implementation was very good. We found no areas of concern.

In the area of layer patterning, etch definition and control were both good.

Alignment and registration were also good.

Technology

These devices were manufactured by a twin-well, selective oxidation CMOS process on a P substrate (no epi). A single level of metal was used and two levels of poly.

Passivation consisted of two layers of silicon-dioxide and was not planarized (a method AMD has used on some products of this type).
They incorporated a single level of metal defined by a standard dry-etch technique. The metal consisted of aluminum with a titanium-nitride barrier. A thin titanium adhesion layer was used under the barrier.

Tungsten plugs were used for all vertical interconnect and they were lined with titanium-nitride liners underneath only (i.e., titanium-nitride deposition before tungsten deposition only).

Pre-metal dielectric was a single layer of reflow glass (BPSG) over densified oxides. This layer was reflowed (prior to contact cuts) to provide the only planarization present. No SOG was used anywhere in this process.

Two levels of polysilicon were used. Poly 2 (tungsten silicide) was used to form all gates on the die and the select/word lines in the EPROM cell array. All gates in the peripheral circuitry used oxide sidewall spacers that were left in place. Poly 1 (no silicide) was used exclusively in the memory cells to form the floating gates.

Standard implanted source/drain diffusions were used in the peripheral circuits and they included oxide sidewall spacers that were left in place, and an LDD process. Salicide was not used.

Interpoly or buried contacts were not used, nor was any special contact layers such as a local interconnect.

At least three thin oxide dielectrics were used. One under poly 1 in the memory array, one under all gates in the peripheral circuits, and the interpoly (ONO) layer in the array.

Standard LOCOS isolation was employed and well implemented. A step was present, confirming the presence of twin-wells.

Redundancy fuses were not present.

**Memory Cell Structures**

Memory cells consisted of a standard dual gate stacked EPROM design. Metal was used for the bit lines. Poly 2 was used to form the word/select lines, and poly 1 was used exclusively to form the floating gates. An oxide-nitride-oxide (ONO) was used as the interpoly dielectric. The EPROM cell size was 5.5 microns\(^2\). This is surprisingly large for a mid-1996 timeframe technology.
Overall minimum feature size measured anywhere on these dice was the 0.7 micron poly 1 and poly 2 (memory cell gates).

**Packaging/Assembly**

As mentioned, the parts were packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs) with quartz windows. Aluminum ultrasonic wirebonds were employed.

The die was mounted to the cavity floor with silver-filled glass die attach. Wirebond pads on the die had a pitch of 230 microns with 90 micron spacing. Pads were 140 microns wide with 120 micron windows.
Whole die photograph of the AMD AM27C010. Mag. 40x.
SEM views of general structures.
Perspective and section SEM views of the EPROM cells.