E/EEPROM

We’ve tried to include a broader category of products in this section this year to try to illustrate the wide range of products available (and finding market acceptance), and the corresponding range of technologies used. We thus have die sizes from 13 microns$^2$ to 130 microns$^2$, gate lengths from 0.2 micron to 1.3 micron and cell sizes from 1.4 micron$^2$ to 117 microns$^2$. 
# Horizontal Dimensions (Design Rules)

## E/EEPROMs

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Model/Description</th>
<th>Die size</th>
<th>Min. M2 width/pace</th>
<th>Min. M1 width/pace</th>
<th>Min. Via (Met. to Met.)</th>
<th>Min. contact (Met. to Si)</th>
<th>Min. Poly 3</th>
<th>Min. Poly 2</th>
<th>Min. Poly 1</th>
<th>Min. gate-(N)†</th>
<th>Min. gate-(P)†</th>
<th>Cell pitch</th>
<th>Cell area</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHARP</td>
<td>LH28F032SUTD-70 32Mb (2 16M dice) Flash E&lt;/br&gt;EEPROM 9652</td>
<td>10.6 x 12.2mm (130mm²)</td>
<td>1μm/0.9μm</td>
<td>N/A</td>
<td>1.0μm</td>
<td>0.65μm</td>
<td>N/A</td>
<td>0.6μm*</td>
<td>0.75μm</td>
<td>0.75μm</td>
<td>0.75μm</td>
<td>1.8μm x 1.9μm</td>
<td>3.4μm²</td>
</tr>
<tr>
<td>MACRONIX</td>
<td>27C8100PC-10 8Mb NAND EPROM 9717</td>
<td>7.4 x 7.5mm (55.5mm²)</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>0.9μm</td>
<td>N/A</td>
<td>0.6μm*</td>
<td>0.6μm</td>
<td>0.8μm</td>
<td>0.9μm</td>
<td>1.15μm x 2.4μm</td>
<td>2.76μm²</td>
</tr>
<tr>
<td>TOSHIBA</td>
<td>TC58A04OF 4Mb Serial Audio NAND EEPROM 9610</td>
<td>5.6 x 6.3mm (35mm²)</td>
<td>0.9μm/1.0μm</td>
<td>1.2μm/1.0μm</td>
<td>0.6μm</td>
<td>0.6μm</td>
<td>0.6μm*</td>
<td>0.6μm</td>
<td>0.5μm</td>
<td>0.5μm</td>
<td>0.5μm</td>
<td>1.3μm x 2.15μm</td>
<td>2.8μm²</td>
</tr>
<tr>
<td>WINDBOND</td>
<td>W27E512-12 512Kb EEPROM 9647</td>
<td>3.6 x 3.6mm (13mm²)</td>
<td>1.5μm/1.1μm</td>
<td>0.9μm</td>
<td>0.9μm</td>
<td>0.7μm</td>
<td>0.7μm</td>
<td>0.9μm</td>
<td>0.9μm</td>
<td>0.9μm</td>
<td>0.9μm</td>
<td>1.3μm x 2.15μm</td>
<td>7.8μm²</td>
</tr>
<tr>
<td>SGS-THOMSON</td>
<td>M28C64-12L 64Kb Parallel EEPROM 9621</td>
<td>3.2 x 6.7mm (21.5mm²)</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>0.9μm</td>
<td>0.9μm</td>
<td>N/A</td>
<td>1.2μm</td>
<td>1.2μm</td>
<td>1.0μm</td>
<td>7.8μm x 15μm</td>
<td>117μm²</td>
</tr>
<tr>
<td>NEC</td>
<td>MPR-18853 32Mb Serial-Parallel NAND MROM 9644</td>
<td>5.6 x 8.8mm (49mm²)</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>0.8μm</td>
<td>N/A</td>
<td>N/A</td>
<td>0.2μm</td>
<td>0.2μm*</td>
<td>0.6μm</td>
<td>0.75μm x 1.9μm</td>
<td>1.425μm²</td>
</tr>
</tbody>
</table>

* Polyide  † Physical gate length  ‡ Plugs  †† 2 dice in package  ‡‡ ROM array  ‡§ Periphery

**Table 3-1**
# VERTICAL DIMENSIONS

<table>
<thead>
<tr>
<th>E/EEPROMs</th>
<th>SHARP LH28F032SUTD-70 32Mb (2 16M dice) Flash EEPROM 9652</th>
<th>MACRONIX 27CS100PC-10 8Mb NAND EPROM 9717</th>
<th>TOSHIBA TC58A040F 4Mb Serial Audio NAND EEPROM 9610</th>
<th>WINDBOND W27E512-12 512Kb EEPROM 9647</th>
<th>SGS-THOMSON M28C64-12L 64Kb Parallel EEPROM 9621</th>
<th>NEC MPR-18853 32Mb Serial-Parallel NAND MRROM 9644</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final passivation</td>
<td>3.3μm</td>
<td>1.8μm</td>
<td>1.1μm</td>
<td>0.75μm</td>
<td>1.0μm</td>
<td>0.4μm</td>
</tr>
<tr>
<td>Metal 2</td>
<td>1.15μm</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Metal 1</td>
<td>0.55μm</td>
<td>1.1μm</td>
<td>0.9μm</td>
<td>1.2μm</td>
<td>0.9μm</td>
<td>0.95μm</td>
</tr>
<tr>
<td>Intermetal dielectric</td>
<td>0.8μm</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Pre-metal dielectric</td>
<td>0.85μm</td>
<td>0.35μm</td>
<td>1.2μm</td>
<td>0.65μm</td>
<td>0.6μm</td>
<td>0.3μm</td>
</tr>
<tr>
<td>Poly 3</td>
<td>N/A</td>
<td>0.3μm*</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Poly 2</td>
<td>0.3μm*</td>
<td>0.06μm</td>
<td>0.1μm</td>
<td>0.3μm</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Poly 1</td>
<td>0.12μm</td>
<td>0.06μm</td>
<td>0.1μm</td>
<td>0.06μm</td>
<td>0.3μm</td>
<td>0.28μm</td>
</tr>
<tr>
<td>Recessed oxide</td>
<td>0.5μm</td>
<td>0.5μm</td>
<td>0.6μm</td>
<td>0.6μm</td>
<td>0.55μm</td>
<td>0.3μm</td>
</tr>
<tr>
<td>N-well</td>
<td>1.6μm</td>
<td>2.5μm</td>
<td>1.5μm</td>
<td>6μm</td>
<td>4μm</td>
<td>4.3μm</td>
</tr>
<tr>
<td>P-well</td>
<td>?.Appendix 2</td>
<td>N/A</td>
<td>9.5μm</td>
<td>N/A</td>
<td>N/A</td>
<td>?Appendix 2</td>
</tr>
<tr>
<td>Epi</td>
<td>5μm (P)</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>

* Polycide  
① Could not delineate
### DIE MATERIALS

#### E/EEPROMs

<table>
<thead>
<tr>
<th></th>
<th>Sharp</th>
<th>Macronix</th>
<th>Toshiba</th>
<th>Windbond</th>
<th>Sgs-Thomson</th>
<th>Nec</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LH28F032SUTD-70 32Mb (2 16M dice) Flash EEPROM 9652</td>
<td>27C8100PC-10 8Mb NAND EEPROM 9717</td>
<td>TC58A040F 4Mb NAND EEPROM 9610</td>
<td>W27E512-12 512Kb EEPROM 9647</td>
<td>M28C64-12L 64K Parallel EEPROM 9621</td>
<td>MPR-18853 32Mb Serial-Parallel NAND MROM 9644</td>
</tr>
</tbody>
</table>

#### Final passivation

- Glass on nitride
- Glass on nitride on SOG on nitride
- Undoped glass
- Nitride on glass
- Nitride on glass
- Glass

#### Metal 2

- Titanium-nitride
- Aluminum
- Titanium

#### Metal 1

- Titanium-nitride
- Aluminum
- Titanium-nitride
- Titanium

#### Plugs

- Tungsten
- N/A
- N/A
- N/A
- N/A
- N/A

#### Intermetal dielectric

- Glass
- N/A
- N/A
- N/A
- N/A
- N/A

#### Reflow glass

- BPSG
- BPSG
- BPSG
- BPSG
- BPSG
- BPSG

#### Polycide metal

- Tungsten
- Tungsten
- Tungsten
- N/A
- Tungsten
- Tungsten

Table 3-3
TECHNOLOGY DESCRIPTION

SHARP LH28F032SUTD-70
32Mbit CMOS FLASH EEPROM

Introduction

These devices were packaged in 56-pin, plastic, TSOP packages. They were in fact two 16Mb dice in one package. They operate from a single 5V supply voltage (or 3.3V Vcc and 5V Vpp), offer an access time of 70nsec, and can be user configured for x 8 or x 16 operation. Devices were date coded 9652 (week 52 of 1996).

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Important/Unique Features

- Two 16Mb dice in one package.
- Intel type Flash EEPROM design (2 poly).

Quality

Quality of the process implementation was good. We found no items of serious concern.

In the area of layer patterning, etch definition was good and control was normal.

Alignment and registration were also good.

Technology

These devices were manufactured by a recessed oxide (LOCOS), twin-well CMOS process in a P-epi on a P substrate. Two levels of metal and two levels of poly were employed.

Passivation consisted of a thick layer of multi-layered glass over a thick layer of nitride. It had not been planarized and did not use a die coat.
Two levels of metal interconnect were used. They were defined by standard dry-etch techniques (no damascene). Metal 2 consisted of aluminum with a titanium-nitride cap and titanium barrier. Metal 1 was aluminum with titanium-nitride cap and barrier on a titanium adhesion layer.

Standard vias were used to connect metal 2 to metal 1, but tungsten plugs were used for all vertical interconnects between metal 1 and silicon. Plugs were lined with titanium-nitride liners, and covered with the titanium-nitride metal 1 barrier. The via cuts penetrated the metal 1 cap so connection here is between the titanium metal 2 barrier and the metal 1 aluminum underneath.

The intermetal dielectric consisted of 2 layers of silicon-dioxide (TEOS?) with a sacrificial layer between. The sacrificial layer had been subjected to a planarizing sputter etch but overall planarization was minimal. CMP was not used and no evidence of an SOG was found.

Pre-metal dielectric was a single layer of reflow glass (BPSG) over deposited densified oxides. This layer was reflowed prior to contact cuts.

Two levels of polysilicon were used. Poly 2 provided all standard gates on the die. It was also employed for the word/program lines in the array and in a few locations to form UPROM (?) gates (floating poly 2 on connected poly 1). Poly 1 was primarily used for floating gates. The interpoly dielectric was an oxide-nitride-oxide (ONO). Direct poly to diffusion (buried) contacts were not used. Oxide sidewall spacers were present and were left in place.

Standard implanted source/drain diffusions were used. A deeper source diffusion was present in the array for programming.

Three thin dielectric layers were employed. They were: gate oxide under poly 1, ONO under poly 2 in the array, and gate oxide under poly 2 in the periphery.

Field oxide isolation consisted of a standard recessed oxide (LOCOS) that was backetched to be almost planar with the silicon surface. No step in this oxide was present at well boundaries but we believe twin-wells were used. An epi layer was also present.

Redundancy fuses were not used.

Overall minimum feature sizes measured anywhere on these dice were the 0.75 micron gates and 0.65 diameter contacts.
Memory Cell Structures

The Flash cell design employed two levels of poly, a deep (program) diffusion, and an ONO for the thin dielectrics. It was noted that the thick recessed field oxide was quite deep and in fact the process looked pretty much identical to Intel’s process. Polycide (poly 2) formed word/program lines and used metal 2 as “piggyback” lines. Metal 1 provided the bit lines. Cell size was 3.4 microns$^2$.

In addition to the Flash cells, two small SRAM arrays were present on the die. They used a special 10 transistor design but standard processing.

Packaging/Assembly

The similarity to Intel’s 32Mb Flash device was present here also. As mentioned, these devices achieved 32Mb capacity by assembling two 16Mb dice in one 56-pin plastic TSOP package. Dice were mounted on both sides of the paddle/flag and attached with silver epoxy.

Standard thermosonic wirebonds were made from both sides of the leadframe to the two dice. Pads on the die had a pitch of 190 microns with 60 micron spacing, and were all placed along two opposing sides of each die. Pads were 130 microns wide with 100 micron windows.

No die coat was present.
Die photograph of the Sharp LH28F032SUTD-70 32Mbit FLASH EEPROM. Mag. 16x.
glass etch,
Mag. 8400x

Mag. 11,000x

Mag. 13,000x

SEM views illustrating general device structures.
SEM views of metal interconnect and dual poly gates.

Mag. 6500x

Mag. 3500x

Mag. 8000x
Topological SEM views of an SRAM cell with schematic. Mag. 4400x, 0°.
SEM views of Flash EEPROM cells.
TECHNOLOGY DESCRIPTION

MACRONIX 27C8100PC-10
8Mbit NAND CMOS EPROM (OTP)

Introduction

These parts were packages in 42-pin Plastic Dual In-Line Packages (PDIPs). They were fully functional production devices organized in a 1M x 8 design. They offer an access time of 100nsec and static operation. They operate from a 5V power source but require a 12.5V programming voltage. These parts were coded 9717 (week 17 of 1997).

See tables for specific dimension and materials identification and see figures for examples of physical structures.

Important/Unique Features

- Relatively complex process including etch equalization patterns.
- Unique cell design using three levels of poly.

Quality

Quality of the process implementation was less than desirable. Metal thinning consumed 100 percent of the aluminum in some areas, leaving only the barrier to provide continuity.

In the area of layer patterning, etch definition and control were both good.

Alignment and registration were also good.

Technology

These devices were manufactured by an N-well, recessed oxidation CMOS process on a P substrate (no epi). A single level of metal and three levels of poly were used.

Passivation consisted of four layers of nitride and glass and was planarized using a spin-on-glass (SOG) between the two nitride layers. Passivation layer 4 was a thick silicon-dioxide. Layers 3 and 1 appeared to be nitrides, while layer 2 was the SOG.
They incorporated a single level of metal defined by a standard dry-etch technique. The metal consisted of aluminum with a titanium-nitride cap and barrier. A thin titanium adhesion layer was used under the barrier. Of special note was the presence of etch equalization patterns in the open areas on the die.

Standard contacts (no plugs) were used for all vertical interconnect.

Pre-metal dielectric was a single layer of reflow glass (BPSG) over deposited densified oxides. This layer was reflowed after contact cuts to provide the planarization. This was adequate in most areas except at a few contacts to polyide (near the edge of the polyide), where excessive metal thinning was present.

Three levels of polysilicon were used. Poly 3 (poly with tungsten silicide) was used to form all peripheral gates and the program lines in the EPROM cell array. All gates used oxide sidewall spacers that were left in place. Poly 1 and 2 (no silicide) were used exclusively in the memory cells to form the floating gates (see below).

Standard implanted source/drain diffusions were used in the peripheral circuits. Lighter implants were employed in the array. Salicide was not used.

Interpoly and buried contacts were used only in the cell array but there they were present between poly 2 and poly 1 and between polyide (poly 3) and poly 1 (see below).

Two thin oxide and one oxide-nitride dielectrics were used. One gate oxide under poly 1 in the memory array, one gate oxide under all gates in the peripheral circuits, and an oxide-nitride dielectric between poly 3 and poly 2 in the array.

Redundancy fuses were employed and used polyide (poly 3). Cutouts in the passivation were present and several fuses had been activated.

Overall minimum feature size measured anywhere on these dice was the 0.6 micron poly 3, and poly 2 on poly 1 memory cell gates.

**Memory Cell Structures**

Memory cells employed a unique stacked EPROM design. Metal was used for the dual bit lines and GND. Poly 1 was used as part of the floating gates and for the control gates. At control gates polyide 3 contacted poly 1 directly (through poly 2?) thus guarantying identical gate oxide at these gates as in the NAND cells where pieces of poly 2 (floating gates) were laid directly on small squares of poly 1 which were laid on the actual gate oxide. The resulting cell size was 2.76 microns². This is quite small for a complex cell such as this.
Packaging/Assembly

As mentioned, the parts were packages in 42-pin Plastic Dual In-Line Packages (PDIPs). The die was mounted to the paddle/flag with silver epoxy die attach.

Standard thermosonic wirebonding was employed using gold wire. Wirebond pads on the die had a pitch of 120 microns with 20 micron spacing. Pads were 100 microns wide with 90 micron windows.

No die coat was present.
Die photograph of the Macronix 27C8100PC-10, 8Mbit EPROM. Mag. 25x.
SEM views illustrating general structures.
SEM views of poly 3 gates.
SEM views of the NAND EPROM cells.
SEM section views of the NAND EPROM cells.
TECHNOLOGY DESCRIPTION

TOSHIBA TC58A040F
4Mbit CMOS FLASH AUDIO NAND EEPROM

Introduction  Ref. report SCA 9709-550

This part was packaged in a 28-pin plastic Thin Small Outline Package (TSOP). It was a fully functional production part. It is a serial audio device capable of storing up to 15 minutes of audio data. It is organized as 4Mb x 1 with 4Kbyte block size. It operates from a single 5V power source. The package was date coded 9610 (week 10 of 1996).

See tables for specific dimensions and materials identification and see figures for examples of physical features.

Important/Unique Features

- Unusual contact structures.
- National Semiconductor mask set.
- Large percentage of die area devoted to logic circuitry.

Quality

Quality of the process implementation was poor due to excessive metal thinning at contacts where aluminum thinning greater that 95 percent was noted.

In the area of layer patterning, etch definition and control were both good.

Alignment and registration were also good.

Technology

These devices were manufactured by a twin-well, recessed oxidation CMOS process employing a P substrate (no epi), one level of metal, and three levels of poly.

Passivation consisted of a layer of nitride over a layer of glass. It was not planarized and varied greatly in thickness due to the large metal steps. The first layer had large voids due to cusping at these locations. It was not covered by a die coat.
The single level of metal interconnect was defined by a standard dry-etch technique (no damascene) and consisted of aluminum with a titanium-nitride barrier (no cap was visible). It should be noted that poly 3 (tungsten polycide) functioned as a metal interconnect.

Standard contacts were employed throughout (no plugs), and represent the primary cause for the quality concern noted. This device used some unique contact structures (see photos). Contact cuts are in some cases made to cover both poly 3 and poly 2 so that metal contacts both. Typically the metal is incapable of covering these steps, but adequate metal surround of the contacts should prevent problems in these areas.

Pre-metal dielectric 2 (between metal and poly 3) appeared to be a layer of BPSG reflow glass and was used for planarization. A first thick layer of BPSG reflow glass (pre-metal dielectric 1) was used for planarization under poly 3. No spin-on-glass (SOG) was used anywhere. Reflow was done prior to contact patterning.

Three levels of polysilicon were used. Polycide 3 (poly and tungsten silicide) was used as a metal substitute in both the array and peripheral circuit areas. Poly 2 formed all gates for the peripheral circuits and the word (control) lines in the cell array. Poly 1 was employed only in the cell array for all floating gates. A separate (third) gate oxide was used under all poly 2 gates in the periphery. Sidewall spacers had been used throughout and removed. Direct poly to diffusion (buried) contacts were used only in the cell array for the polycide (poly 3) bit line contacts.

Implanted source/drain diffusions appeared normal. Diffusions were not silicided.

At least three separate gate oxides plus the interpoly ONO were used. The gate oxides are: under poly 1 storage cells, under poly 1 edge cells (of NAND string), and under poly 2 in the peripheral circuits.

Standard recessed field oxide isolation (LOCOS) was used and backetched normally. A small step was present at the top of the LOCOS only so it is probable only nested wells were used.

Poly 3 redundancy fuses were also present. Passivation cutouts were located over the fuses. No activated fuses were found.

Overall minimum feature size measured anywhere on the die was the 0.5 micron poly 1 and 2 (gates in memory cells).
Memory Cell Structures

The EEPROM array used the standard dual gate stacked cell implemented in a NAND configuration. Separate program lines were present at the edge of each word string (for “Flash” programming?). These program gates used a continuous poly 1 line under the poly 2 program lines, a different gate oxide under the poly 1, the same ONO between poly 1 and 2, and wider poly 1 and 2 (gate length) than the memory gates. Polycide (poly 3) was used for all bit lines. The memory cell gates themselves were arranged in strings of 16 cells, use a different gate oxide than either the control cells or the peripheral circuit gates, use an ONO between poly 1 and poly 2 and are the shortest gates anywhere on the die. The EEPROM cell size was 2.8 micron2.

Packaging/Assembly

As mentioned, the part was packaged in a 28-pin plastic Thin Small Outline Package (TSOP) date coded 9610. It used a hollow center leadframe paddle/flag, silver epoxy die attach, and standard thermosonic wirebonding employing gold wire. Only six pins were connected to the die!

Wirebond pads on the die had a minimum pitch of 195 microns with 95 micron spacing. Pads were 100 microns wide with 90 micron windows.

No die coat was present.
Die photograph of the Toshiba TC58A040F 4Mbit NAND EEPROM. Mag. 31x.
SEM views illustrating general structures.
SEM views of metal-to-poly contacts.

Mag. 20,000x, 60°

Mag. 14,000x, 60°

metal-to-poly 3 and N+, Mag. 13,000x
SEM views of the memory cells.

Mag. 15,000x, 60°

Mag. 15,000x, 60°

Mag. 40,000x
TECHNOLOGY DESCRIPTION

WINBOND W27E512-12
512Kbit CMOS EEPROM

Introduction

These devices were packaged in 28-pin Plastic Dual In-line (PDIP) packages date coded 9647. They are high speed devices organized as 64K x 8 and use 14V erase and 12V program voltages. Operation is from a 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Important/Unique Features

- Unique two poly EEPROM cell design.

Quality

Quality of the process implementation was acceptable. We found no items of serious concern, although metal thinned up to 90 percent at some contacts.

In the area of layer patterning, etch definition and control were both good.

Alignment and registration were also good.

Technology

These devices were manufactured by a recessed field oxide, N-well CMOS process on a P substrate (no epi). They employ a single level of metal interconnect and two levels of poly.

Passivation consisted of a layer of nitride over a layer of silicon-dioxide and was not planarized. It was not covered by a die coat.

The single level of metal was defined by a standard dry-etch technique (no damascene). Metal consisted of aluminum with a titanium-nitride cap and barrier. A thin titanium adhesion layer was present underneath the barrier.

Standard vias (not plugs) were used for all vertical interconnect.
Pre-metal dielectric was a single layer of reflow glass (BPSG) over deposited densified oxides. This layer was reflowed prior to contact cuts, and provided the only planarization. No SOG was used anywhere in the process.

Two layers of poly (no silicide) were used. Poly 2 was used to form all standard gates on the die and word lines in the memory array. Poly 1 was very thin and used exclusively for floating gates in the memory cells. Oxide sidewall spacers were present and were left in place. Direct poly to diffusion (buried) contacts were not used.

Normal source/drain diffusions were implanted in peripheral circuits. Special source and drain implants were used in the memory cells but could not be delineated well enough to characterize. Diffusions were not silicided.

Field oxide isolation consisted of a standard recessed oxide (LOCOS)backetched normally. No step was present at well boundaries and no other sign of the presence of twin-wells was found. An epi layer was also not used.

Redundancy fuses were not present.

Overall minimum feature size measured anywhere on these dice was the 0.7 micron poly 2 and poly 1, and the 0.9 micron gates.

**Memory Cell Structures**

The unique (1½ transistor) memory cell design consisted of poly 2 word lines and select gates, and very thin poly 1 floating gates that appear to use Fowler-Nordheim tunneling for programming. Metal formed the bit lines. Cell size was 7.8 microns$^2$.

**Packaging/Assembly**

As mentioned, these devices were packaged in standard 28-pin through hole mounting plastic DIPs. Silver epoxy die attach was used.

The standard thermosonic wirebonds on the die were made to pads on the die that had a pitch of 290 microns with 150 micron spacing. Pads were 140 microns wide with 90 micron windows.

No die coat was present.
Die photograph of the Winbond W27E512 512Kbit EEPROM. Mag. 48x.
SEM views illustrating general structure.
SEM views of typical gates.
SEM views of the EEPROM cell design.
TECHNOLOGY DESCRIPTION

SGS-THOMSON M28C64-12l
64Kbit CMOS EEPROM

Introduction

Ref. report SCA 9710-559

The parts were packaged in 28-pin Plastic Dual In-line Packages (PDIPs). They were fully functional production devices organized in an 8K x 8 parallel EEPROM design. They offer an access time of 90nsec., at 5V (120nsec. at 3V) and software data protection. They operate from a 5V or 3V power source. The date code could not be determined but is assumed to be early 1997.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Important/Unique Features

- Unique metal structure.

- Very large cell size (117 micron2).

Quality

Quality of the process implementation was good. We found no areas of concern.

In the area of layer patterning, etch definition and control were both good.

Alignment and registration were also good.

Technology

These devices were manufactured by an N-well, recessed oxidation CMOS process on a P substrate (no epi). Single levels of metal and poly were used.

Passivation consisted of two layers of silicon-dioxide and was not planarized, and not covered with a die coat.
They incorporated a single level of metal defined by a standard dry-etch techniques (no damascene). Metal consisted of aluminum with a titanium-nitride cap and titanium over titanium-nitride on titanium barrier. The presence of the titanium layer over the titanium-nitride barrier is somewhat unique to S/T.

Standard contacts (no plugs) were used.

Pre-metal dielectric was a single layer of reflow glass (BPSG) over densified deposited oxides. This layer was reflowed after contact cuts, and thus provided all the planarization needed.

A single level of polysilicon (no polyicide) was used to form all gates on the die and all the elements in the EEPROM cell array. All gates used oxide sidewall spacers that were left in place. Buried contacts were not used, nor was any other special interconnect such as a local interconnect.

Standard implanted source/drain diffusions were used and not silicided. Other implants were present in the memory array (see below).

The process appears to use only two different thin oxide dielectrics. One for gate oxides and one for the tunnel-oxide windows in the cell array.

Standard LOCOS isolation was employed and etched back normally. No step was present, confirming the absence of twin-wells.

Redundancy fuses were also not present.

Overall minimum feature sizes measured anywhere on these dice were the 0.8 micron contacts and 1.0 micron metal.

**Memory Cell Structures**

Memory cells consisted of a tunnel oxide (window), single poly EEPROM design. Metal was used for the bit lines. Poly was used to form the word/select lines, tunnel oxide devices and capacitor elements. The select gates used in the memory cells were very large, measuring 1.9 micron long. The resulting cell size was 117 microns\(^2\), which is the largest cell size we’ve seen for many years.
Packaging/Assembly

As mentioned, the parts were packaged in 28-pin Plastic Dual In-line Packages (PDIPs). The die was mounted to the paddle/flag with silver epoxy die attach.

Thermosonic wirebonds were employed, using standard gold wire. Wirebond pads on the die had a pitch of 185 microns with 75 micron spacing. Pads were 110 microns wide with 90 micron windows.

No die coat was present.
Die photograph of the S/T M28C64-12L 64Kbit EEPROM. Mag. 34x.
SEM views of general structures.
SEM views of poly gates.
SEM views of cell structures.

Mag. 3200x, 60°

Mag. 6500x

Mag. 26,000x
TECHNOLOGY DESCRIPTION

*NEC D23C32000A*

*32Mbit CMOS NAND MROM*

**Introduction**

These parts were packaged in 44-pin plastic Small Outline Integrated Circuit Packages (SOICs). They were fully functional devices, offer a 120nsec. maximum access time and are organized as 4M x 8 or 2M x 16 (selectable) serial-parallel NAND format. They operate from a single 5V power source. They were date coded 9644 (week 44 of 1996).

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

**Important/Unique Features**

- Very small gates in the cell array (0.18\(\mu\)m effective channel length).

**Quality**

Quality of the process implementation was good, except at some metal contacts where aluminum thinning up to 90 percent was noted.

In the area of layer patterning, etch definition and control were both normal.

Alignment and registration were good.

**Technology**

The devices were manufactured by a twin-well, recessed oxidation CMOS process employing a P substrate (no epi) using one level of metal and one level of poly.

Passivation consisted of a single layer of glass that was not planarized and not covered with a die coat.

The single level of metal was defined by a standard dry-etch technique (no damascene). Metal consisted of aluminum with a titanium-nitride cap and barrier. A thin titanium adhesion layer was present under the barrier.

Standard contacts were employed throughout (no plugs). Contact cuts were made after
pre-metal glass reflow so some steep edges were present.

Pre-metal dielectric was a BPSG reflow glass and provided the only planarization. No spin-on-glass (SOG) was used anywhere.

A single level of polycide (poly and tungsten-silicide) was used. It formed all gates on the die. Definition of this layer was less than perfect showing what appeared to be evidence of standing wave patterns (see photos). Sidewall spacers had been used throughout and left in place. Direct poly to diffusion contacts (buried contacts) were not used.

Implanted source/drain diffusions appeared to be normal. Diffusions were not silicided.

Standard recessed field oxide isolation (LOCOS) was used and was backetched in the normal manner. A step was present in the LOCOS confirming the presence of twin-wells.

Redundancy fuses were not present.

Overall minimum feature size measures anywhere on these dice was the 0.2 micron poly (gates) in the cell array.

**Memory Cell Structures**

The memory cell design used standard polycide for word lines but patterned to form 0.2 micron gates. Metal formed the bit lines connecting to the dual diffusion bit lines. Programming is achieved by (depletion) implanted diffusions.

**Packaging/Assembly**

As mentioned, these parts were packaged in 44-pin plastic SOICs. They used silver epoxy die attach, and standard thermosonic wirebonding employing gold wire.

Wirebond pads on the die had a minimum pitch of 180 microns with 70 micron spacing. Pads were 110 microns wide with 100 micron windows.

No die coat was present.
Die photograph of the NEC D23C32000A 32Mbit MROM. Mag. 26x.
SEM views illustrating general structures.
SEM views of polycide gates.
SEM views of the NAND ROM cells.