Construction Analysis

Samsung KM44C4000J-7
16 Megabit DRAM

Report Number: SCA 9311-300I
## INDEX TO TEXT

<table>
<thead>
<tr>
<th>TITLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>MAJOR FINDINGS</td>
<td>1</td>
</tr>
<tr>
<td>TECHNOLOGY DESCRIPTION</td>
<td></td>
</tr>
<tr>
<td>Assembly</td>
<td>2</td>
</tr>
<tr>
<td>Die Process and Design</td>
<td>2 - 3</td>
</tr>
<tr>
<td>ANALYSIS RESULTS I</td>
<td></td>
</tr>
<tr>
<td>Assembly</td>
<td>4</td>
</tr>
<tr>
<td>ANALYSIS RESULTS II</td>
<td></td>
</tr>
<tr>
<td>Die Process and Design</td>
<td>5 - 7</td>
</tr>
<tr>
<td>ANALYSIS PROCEDURE</td>
<td>8</td>
</tr>
<tr>
<td>TABLES</td>
<td></td>
</tr>
<tr>
<td>Overall Evaluation</td>
<td>9</td>
</tr>
<tr>
<td>Package Markings</td>
<td>10</td>
</tr>
<tr>
<td>Wirebond Strength</td>
<td>10</td>
</tr>
<tr>
<td>Die Material Analysis (EDX and WDX)</td>
<td>10</td>
</tr>
<tr>
<td>Horizontal Dimensions</td>
<td>11</td>
</tr>
<tr>
<td>Vertical Dimensions</td>
<td>12</td>
</tr>
</tbody>
</table>
INTRODUCTION

This report describes a construction analysis of the Samsung KM44C4000J-7 16-megabit CMOS Dynamic RAM. Four samples molded in 24-pin plastic SOJ packages and date coded 9313 were supplied for the analysis. Analysis of the packaging and assembly is included.

MAJOR FINDINGS

Questionable Items:¹

- Silicon nodules occupied up to 75 percent² of metal 2 line widths (Figure 16).

Special Features:

- Twin-well process with sub-micron geometries (0.3 micron poly 1 and 0.5 micron metal 1).
- Two levels of metal, four levels of poly.
- Metal 1 contacts were completely filled with aluminum (aluminum reflow).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²The seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

Assembly:

• 24-pin (28 pin format) plastic small-outline J-lead package (SOJ).

• Iron-nickel (FeNi) leadframe.

• External leads were coated with tin-lead (SnPb) solder.

• Internal leadframe plating consisted of spot-plated silver (Ag) over a thin copper (Cu) flash. No plating was present on top of the header.

• Lead-locking provisions (anchors) were present at all pins.

• A dimpled header was employed.

• All pins were connected.

• Die attach was by silver (Ag)-epoxy.

• Dicing was by the sawn method.

• Wirebonding was by the thermosonic ball bond method using 1.3 mil O.D. gold wire.

Die Process and Design:

• Fabrication process: Selective oxidation CMOS process with twin wells in a P(?) substrate.

• Die coat: A patterned (to clear bond pads) polyimide die coat was present to protect against alpha particle-induced leakage.

• Overlay passivation: A layer of silicon-nitride over two layers of silicon-dioxide. The second layer of silicon-dioxide was multilayered.
TECHNOLOGY DESCRIPTION (continued)

• Metallization: Two levels of metal conductors were used. Metal 2 consisted of aluminum only. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier. Both metal levels were defined using a dry-etch technique.

• Interlevel dielectric: Three layers of silicon-dioxide plus a filler glass (SOG) between interlevel glasses 2 and 3.

• Intermediate glass: Two layers of boron- and phosphorus-doped glass in addition to the various densified oxides. Intermediate glass layers (between poly 3 and polycide, and polycide and metal 1) had been reflowed prior to deposition of subsequent layers and contact cut definition.

• Polysilicon: Four levels of dry-etched polysilicon were used. Poly 4 employed a tungsten silicide (polycide) and was used for the bit lines in the cell array and interconnect in the decode areas. Poly 3 (sheet) was used for the common passive capacitor plate and poly 2 was used for the individual active capacitor plates in the cell array. Poly 1 was used for all the gates on the die.

• Diffusions: Standard N+ and P+ implanted source/drain diffusions formed N- and P-channel transistors. Transistors were formed using an LDD process with oxide sidewall spacers.

• Wells: Twin wells in an P substrate.

• Memory cells: The memory cell used an NMOS DRAM cell design consisting of a select gate and a stacked capacitor. Polycide formed the bit lines. Poly 1 formed the word lines and was "piggybacked" by metal 1. Stacked capacitors were formed by poly 2 pads covered by a poly 3 sheet separated by a thin oxide/nitride dielectric.

• Fuses: Redundancy was implemented using polycide fuses. Laser blown fuses were noted on all samples. Oxide cuts were present above fuse locations and were then covered by the overlay passivation. No separate guardbands were found around the fuses.
ANALYSIS RESULTS I

Assembly

Figures 1 - 7

Questionable Items\(^1\): None.

General Items:

- Devices were packaged in 24-pin (28 pin format) plastic SOJs.

- Overall package quality: Normal. No serious defects were found on the external or internal portions of the packages. Some small voids were noted in the plastic packaging material; however, overall package integrity was normal. Small gaps were present at the lead exits. Although they did not penetrate far into the package the internal plating was relatively close to the edge of the package. This could be monitored to ensure silver does not become exposed (and subject to dendrite growth).

- Wirebonding: Thermosonic ball bond method using 1.3 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were good (see page 10). Normal intermetallic was present at ball bonds. Wire spacing and bond placement was good.

- Die attach: A silver-epoxy compound was used. Die attach quality was good with no voids observed.

- Die dicing: Die separation was by sawing (90+ percent) with normal quality workmanship.

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

Die Process and Design  

Figures 8 - 39

Questionable Items:¹

- Silicon nodules occupied up to 75 percent of metal 2 line widths (Figure 16).

Special Features:

- Twin-well process with sub-micron geometries (0.3 micron poly 1 and 0.5 micron metal 1).
- Two levels of metal, four levels of poly.
- Metal 1 contacts were completely filled with aluminum (aluminum reflow).

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an N substrate.
- Design and layout: Die layout was clean and efficient. Alignment was good at all levels.
- Die coat: A patterned (to clear bond pads) polyimide die coat was present to protect against alpha particle-induced leakage. Coverage was good.
- Die surface defects: No damage, process defects, or contamination was found.
- Overlay passivation: A layer of silicon-nitride over two layers of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II (continued)

• Metallization: Metal 2 consisted of silicon-doped aluminum only. Metal 1 consisted of undoped aluminum with a titanium-nitride cap and barrier.

• Metal patterning: Both metal layers were defined by dry-etch techniques. Definition was very good and no significant overetch was present.

• Metal defects: Some notches were noted in the metal 2 (Figure 15). No notches occupied more than 30 percent of the line width and the entire metal thickness. The condition present is not of real concern but should possibly be monitored. Silicon nodules noted following removal of metal 2 occupied up to 75 percent of the line width. Silicon nodules of 50 percent or greater will lead to current crowding, which may lead to electromigration and is thus of concern. No silicon nodules were noted on the barrier following the removal of aluminum 1.

• Metal step coverage: Metal 2 thinning up to 65 percent was noted at vias. MIL-STD-883D allows up to 70 percent thinning for contacts of this size. The metal 1 cap was not present in vias (metal 2-to-metal 1), thus was removed during via cuts. All metal 1 contacts were completely filled with aluminum providing a very good current path. Integrity of the metal 1 barrier was good.

• Contacts: Contact cuts were probably defined by a two-step process (dry etch followed by wet etch). No over-etching of the contacts was present.

• Interlevel dielectric: The dielectric between metal 1 and metal 2 consisted of three layers of silicon-dioxide. Interlevel oxides 2 and 3 were separated by a filler (SOG) glass. No problems were found.

• Intermediate glass: Two layers of boron- and phosphorus-doped glass in addition to the various densified oxides. Glass layer 2 (between polycide and metal 1) and 1 (between poly 3 and polycide) had been reflowed prior to deposition of subsequent layers and contact cuts.
ANALYSIS RESULTS II (continued)

• Polysilicon: Four levels of polysilicon were used. Poly 4 employed a tungsten silicide (polycide) and was used to form the bit lines in the array and as interconnect in the decode areas. Poly 3 (sheet) was used to form the common passive plate of the capacitors and poly 2 was used to form the individual active capacitor plates. Poly 1 formed all gates on the die. Definition of all poly layers was by a dry-etch technique of good quality. No stringers or spurs were noted.

• Isolation: Local oxide (LOCOS). No problems were present at the birdsbeak or elsewhere.

• Diffusions: Standard implanted N+ and P+ diffusions were used for sources and drains. No problems were found. Oxide sidewall spacers were used to reduce internal capacitance and hot-carrier effects (LDD process).

• Wells: Twin-wells were employed. Definition was normal.

• Epi: No epi layer was employed. No defects were found in the substrate silicon.

• Fuses: Redundancy was implemented by laser blowing polycide fuses. Blown fuses were present on all samples. Oxide cuts were present above fuse locations and were covered by the passivation.

• Memory cells: A stacked capacitor DRAM cell design was employed. Cell pitch was 1.4 x 2.8 microns (3.9 microns²). Polycide formed the bit lines, poly 3 and poly 2 formed the capacitor plates, and poly 1 formed the word lines and was "piggybacked" by metal 1. Poly 3 underlaps the poly 2 capacitor plates for increased area (Figure 38).

Special Features:

• Samples 1 and 2 were subjected to ESD sensitivity tests. Results revealed that all pin combinations passed ±4000V.

• Samples 3 and 4 were subjected to latch-up sensitivity tests. Pins were tested from -200ma to 200ma. Tests revealed no pins latched-up on either sample.
PROCEDURE

The devices were subjected to the following analysis procedures.

External inspection
ESD sensitivity
Latch-up sensitivity
X-ray
Package section and material (EDX)
Decapsulation
Internal optical inspection
SEM inspection of assembly features and passivation
Passivation integrity test
Wirepull test
Passivation removal
SEM inspection of metal 2
Metal 2 removal and inspect for silicon nodules and vias
Delayer to metal 1 and inspect
Metal 1 removal and inspect barrier
Delayer to poly/substrate and inspect poly structures and die surface
Die sectioning (90° for SEM)*
Measure horizontal dimensions
Measure vertical dimensions
Die material analysis (EDX and WDX)

*Delineation of cross sections is by silicon etch unless otherwise indicated.
OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity N
Package markings G
Die placement G
Die attach quality G
Wire spacing G
Wirebond placement G
Wirebond quality G
Dicing quality G
Wirebond method Thermosonic ball bonds using 1.3 mil gold wire.
Die attach method Silver-epoxy
Dicing method Sawing (90+ percent)

Die surface integrity:
  Tool marks (absence) G
  Particles (absence) G
  Contamination (absence) G
  Process defects (absence) G
General workmanship G
Passivation integrity G
Metal definition G
Metal integrity NP
Contact coverage G
Contact registration G

1Silicon nodules occupied up to 75 percent of metal 2 line widths.

G = Good, P = Poor, N = Normal, NP = Normal/Poor
PACKAGE MARKINGS

TOP

(Logo) KOREA
313
KM44C4000J-7

BOTTOM

4YL
C03ZAA

WIREBOND STRENGTH

Wire material: 1.3 mil O.D. gold
Die pad material: aluminum
Material at package lands: silver

# of wires tested: 13
Bond lifts: 0
Force to break - high: 18.0g
- low: 11.0g
- avg.: 14.5g
- std. dev.: 2.4

DIE MATERIAL ANALYSIS (EDX and WDX)

Passivation: Silicon-nitride over two layers of silicon-dioxide.

Metal 2: Silicon-doped aluminum.

Interlevel dielectric: Three levels of silicon-dioxide with a filler glass between layers 2 and 3.

Metal 1: Undoped aluminum with a titanium-nitride cap and barrier.

Intermediate glass: CVD glass containing an average of 5.2 wt. percent boron and 3.9 wt. percent phosphorus over various densified oxides.

Polycide: Tungsten silicide.
**HORIZONTAL DIMENSIONS**

Die size: 5.8 x 16.6 mm (230 x 656 mils)

Die area: 97 mm$^2$ (150,880 mils$^2$)

Min pad size: 0.11 x 0.12 mm (4.5 x 4.7 mils)

Min pad window: 0.1 x 0.11 mm (3.8 x 4.2 mils)

Min pad space: 0.12 mm (4.7 mils)

Min metal 2 width: 1.3 microns

Min metal 2 space: 1.2 microns

Min metal 1 width: 0.5 micron

Min metal 1 space: 0.7 micron

Min via (metal 2-to-metal 1): 1.2 microns

Min contact: 0.7 micron

Min polycide width: 0.5 micron

Min polycide space: 0.65 micron

Min poly 2 space: 0.5 micron

Min poly 1 width: 0.3 micron

Min poly 1 space: 0.5 micron

Min gate length (N-channel): 0.5 micron

(P-channel): 0.8 micron

Cell pitch: 3.64 microns$^2$

Cell size: 1.4 x 2.6 microns
### VERTICAL DIMENSIONS

Die thickness: 13.5 mils (0.3 mm)

**Layers:**

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die coat</td>
<td>9.5 microns</td>
</tr>
<tr>
<td>Passivation 3</td>
<td>0.55 micron</td>
</tr>
<tr>
<td>Passivation 2</td>
<td>0.3 micron</td>
</tr>
<tr>
<td>Passivation 1</td>
<td>0.1 micron</td>
</tr>
<tr>
<td>Metal 2 - aluminum</td>
<td>0.9 micron</td>
</tr>
<tr>
<td>Interlevel dielectric - glass 3</td>
<td>0.4 micron</td>
</tr>
<tr>
<td>- glass 2</td>
<td>0.4 micron</td>
</tr>
<tr>
<td>- glass 1</td>
<td>0.08 micron (approx.)</td>
</tr>
<tr>
<td>Metal 1 - cap</td>
<td>0.04 micron (approx.)</td>
</tr>
<tr>
<td>- aluminum</td>
<td>0.55 micron</td>
</tr>
<tr>
<td>- barrier</td>
<td>0.15 micron</td>
</tr>
<tr>
<td>Intermediate glass 2</td>
<td>0.5 micron</td>
</tr>
<tr>
<td>Polycide - silicide</td>
<td>0.2 micron</td>
</tr>
<tr>
<td>- poly 4</td>
<td>0.05 micron (approx.)</td>
</tr>
<tr>
<td>Intermediate glass 1</td>
<td>0.2 micron</td>
</tr>
<tr>
<td>Oxide on poly 3</td>
<td>0.1 micron</td>
</tr>
<tr>
<td>Poly 3</td>
<td>0.1 micron</td>
</tr>
<tr>
<td>Capacitor dielectric</td>
<td>150 Å (approx.)</td>
</tr>
<tr>
<td>Poly 2</td>
<td>0.15 micron</td>
</tr>
<tr>
<td>Interpoly oxide - total</td>
<td>0.35 micron</td>
</tr>
<tr>
<td>- nitride</td>
<td>0.04 micron (approx.)</td>
</tr>
<tr>
<td>Poly 1</td>
<td>0.2 micron</td>
</tr>
<tr>
<td>Local oxide (under poly 1)</td>
<td>0.3 micron</td>
</tr>
<tr>
<td>Oxide on N+</td>
<td>0.08 micron (approx.)</td>
</tr>
<tr>
<td>Oxide on P+</td>
<td>0.06 micron (approx.)</td>
</tr>
<tr>
<td>N+ source/drain</td>
<td>0.2 micron</td>
</tr>
<tr>
<td>P+ source/drain</td>
<td>0.3 micron</td>
</tr>
<tr>
<td>N- well:*</td>
<td>4.5 microns</td>
</tr>
</tbody>
</table>

*It was not possible to determine well and substrate polarity with certainty.*
## INDEX TO FIGURES

<table>
<thead>
<tr>
<th>Category</th>
<th>Figures</th>
</tr>
</thead>
<tbody>
<tr>
<td>PACKAGING AND ASSEMBLY</td>
<td>1 - 7</td>
</tr>
<tr>
<td>DIE LAYOUT AND IDENTIFICATION</td>
<td>8 - 9</td>
</tr>
<tr>
<td>PHYSICAL DIE STRUCTURES</td>
<td>10 - 38</td>
</tr>
<tr>
<td>COLOR DRAWING OF GENERAL DEVICE STRUCTURE</td>
<td>32</td>
</tr>
<tr>
<td>FUSES</td>
<td>33 - 34</td>
</tr>
<tr>
<td>MEMORY CELL STRUCTURES</td>
<td>35 - 38</td>
</tr>
<tr>
<td>CIRCUIT LAYOUTS</td>
<td>39</td>
</tr>
</tbody>
</table>

- ii -
Figure 1. Package photograph and pinout diagram of the Samsung KM44C4000. Mag. 5x.
Figure 2. Topological and side x-ray views. Mag. 6x.
Figure 3. Section view of the package illustrating general construction. Mag. 17x.
Figure 4. Section views illustrating lead forming and lead exit.
Figure 5. Section views illustrating dicing, die attach and die coat.
Figure 6. SEM views of a die corner and edge seal. 60°.
Figure 7. SEM and section views of typical wirebonds.
Figure 8. Portion of the Samsung KM44C4000 die photograph. Mag. 30x.
Figure 8a. Remaining portion of the Samsung KM44C4000 die photograph. Mag. 30x.
Figure 9. Die identification markings. Mag. 800x.
Figure 10. SEM views of general passivation coverage. 60°.

Mag. 4000x

Mag. 13,500x
Figure 11. SEM section views illustrating general device structure.
Figure 12. SEM section view of a metal 2 line profile. Mag. 25,000x.

Figure 13. Topological SEM views of metal 2 patterning. Mag. 3500x, 0°.
Figure 14. SEM views of general metal 2 integrity. 60°.
Figure 15. SEM views illustrating notches in the metal 2.
Figure 16. Topological SEM views of silicon nodules (following removal of metal 2). 0°.
Figure 17. SEM views of typical vias.

Mag. 17,500x

Mag. 27,000x, 45°
Figure 18. SEM section view of metal 1 line profiles. Mag. 40,000x.

Figure 19. Topological SEM views of metal 1 patterning. Mag. 4000x, 0°.
Figure 20. SEM views of general metal 1 integrity. 60°.
Figure 21. SEM views of general barrier coverage. 50°.

Mag. 8000x

Mag. 25,000x
Figure 22. SEM section views of metal 1-to-poly contacts. Mag. 35,000x.
Figure 23. SEM section views of metal 1-to-diffusion contacts. Mag. 35,000x.
Figure 24. SEM view of general polycide coverage. Mag. 15,000x, 60°.

Figure 25. SEM section view of a polycide-to-N+ contact. Mag. 50,000x.
polycide-to-poly 3

polycide-to-poly 1

Figure 26. SEM section views of various polycide contacts. Mag. 50,000x.
Figure 27. Topological SEM views of poly 1 patterning. 0°.
Figure 28. SEM views of general poly 1 coverage. 60°.
Figure 29. SEM section views of typical transistors.

P-channel,
Mag. 35,000x

N-channel,
Mag. 50,000x

glass etch,
Mag. 40,000x
Figure 30. SEM section view of a local oxide birdsbeak. Mag. 50,000x.

Figure 31. Section views illustrating the well structure.

Mag. 30,000x

Mag. 1600x
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate

Figure 32. Color cross section drawing illustrating device structure.
Figure 33. Topological SEM views of fuses. Mag. 8000x, 0°.
Figure 34. Perspective SEM views of fuses. Mag. 6500x, 60°.
Figure 35. Topological SEM views of DRAM cells. Mag. 15,000x, 0°.
unlayered, Mag. 15,000x, 0°

Figure 35a. Topological SEM view of DRAM cells along with the schematic.
Figure 36. Perspective SEM views of the cell array. Mag. 8500x, 60°.
Figure 37. SEM section views of DRAM cells (parallel to bit lines).
Figure 38. Detail section views of DRAM cells.

Mag. 45,000x

Mag. 50,000x

glass etch,
Mag. 50,000x
input protection, intact,
Mag. 500x

intact, Mag. 800x

metal 1, Mag. 800x

Figure 39. Optical views illustrating typical input protection and circuit layout.