Motorola XC56002PV80
Digital Signal Processor

Report Number: SCA 9608-509
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INTRODUCTION

This report describes a construction analysis of the Motorola XC56002PV80 Digital Signal Processor. Five devices packaged in 144-pin Square Quad Flat Packs (SQFPs) were received for the analysis. Devices were date coded 9552. An analysis of the assembly is also included.

MAJOR FINDINGS

Questionable Items:¹

- Metal 2 aluminum thinning up to 90 percent² at metal 2-to-metal 1 vias (Figure 18).
- Metal 1 aluminum thinning up to 85 percent² at metal 1 contacts (Figure 23).

Special Features:

- Sub-micron gate lengths (0.6 micron N-channel and 0.7 micron P-channel).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

Assembly:

- Devices were packaged in 144-pin Square Quad Flat Packs (SQFPs) for surface mount applications (cavity down).

- The leadframe was constructed of copper and plated externally with tin-lead solder. Internal plating consisted of silver and was present on the internal portion of the leadframe and the sides of the header. The silver plating was not present on top of the header. A dimpled header was added for package strength.

- Die separation was by sawing (full depth). Silver-filled epoxy was used to attach the die to the header.

- Wirebonding was by the thermosonic ball bond method using 1.0 mil O.D. gold wire.

- Numerous pins were not connected. No multiple bonding was noted.

Die Process:

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.

- No die coat was present.

- Passivation consisted of a layer of silicon-nitride over a layer of silicon-dioxide.

- Metallization consisted of two layers of metal. Metal 2 consisted of aluminum with titanium-nitride cap and no barrier. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier. Standard contacts and vias were used at both levels (no plugs).
TECHNOLOGY DESCRIPTION (continued)

- Interlevel dielectric (between metals) consisted of two layers of silicon-dioxide.

- Pre-metal dielectric consisted of borophosphosilicate glass (BPSG) over various densified oxides. The glass was refloved prior to contact cuts only.

- A single layer of poly (no silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with nitride sidewall spacers left in place.

- Local oxide (LOCOS) isolation. A step was present in the oxide at the well boundary, which indicates a twin-well process was used.

- The memory cell array utilized a 6T SRAM cell design. Metal 2 was used to form the bit lines and distribute GND (via Metal 1). Metal 1 was used to form “piggyback” word lines, provide cell interconnect and distribute Vcc. Poly was used to form word lines and all gates.

- Redundancy fuses were not present.
ANALYSIS RESULTS I

Package and Assembly:  

Questionable Items:¹ None.

General Items:

• Devices were packaged in 144-pin Square Quad Flat Packs (SQFPs) for surface mount applications (cavity down).

• Overall package quality: Good. No significant defects were noted on the external or internal portions of the package. The package was subjected to a dye penetrant test. No dye penetrant was noted at leadframe exits, header or die.

• Leadframe: The leadframe was constructed of copper (Cu) and plated externally with tin-lead (SnPb) solder. Internal plating consisted of silver and was present on the internal portion of the leadframe and the sides of the header. The silver plating was not present on top of the header. No problems were noted. A dimpled header was added for package strength. No gaps were noted at lead exits.

• Die dicing: Die separation was by sawing (full depth) of normal quality. No large cracks or chips were present.

• Die attach: A silver-filled epoxy was used to attach the die to the header. No voids were noted.

• Wirebonding: Wirebonding was by the thermosonic ball bond method using 1.0 mil O.D. gold wire. Some incomplete intermetallic formation was noted; however, bond pull strengths were normal (see page 10) and no bond lifts occurred. Ball bonds were overcompressed slightly; however, no problems are foreseen.

• Numerous pins were not connected. No multiple bonding was noted.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

Die Process:  

Questionable Items:¹

• Metal 2 aluminum thinning up to 90 percent² at metal 2-to-metal 1 vias (Figure 18).

• Metal 1 aluminum thinning up to 85 percent² at metal 1 contacts (Figure 23).

Special Features:

• Sub-micron gate lengths (0.6 micron N-channel and 0.7 micron P-channel).

General Items:

• Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.

• Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found. Slots and beveled corners were present in Metal 1 and Metal 2 bus lines.

• Die coat: No die coat was present.

• Overlay passivation: Consisted of a layer of nitride over a layer of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good as the passivation extended into the scribe lane.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.
ANALYSIS RESULTS II (continued)

• Metallization: Two layers of metal. Metal 2 consisted of aluminum with a titanium-nitride cap and no barrier. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier. Standard contacts and vias were used at both levels (no plugs were used).

• Metal patterning: Both metal layers were patterned by a dry etch of normal quality. Both metal were widened around vias and contacts.

• Metal defects: No voiding, notching, or neckdown was noted in either of the metal layers. All contacts and vias were completely surrounded by metal. No silicon nodules were noted following the removal of either metal layer.

• Metal step coverage: Metal 2 aluminum thinned up to 90 percent at via edges. Total Metal 2 thinning was reduced to 85 percent with the addition of the cap metal. Metal 1 aluminum thinned up to 85 percent at contact edges. Total Metal 1 thinning was reduced to 75 percent with the addition of the cap and barrier metals.

• Interlevel dielectric: Interlevel dielectric consisted of two layers of silicon-dioxide. The first layer (Glass 1) had been backetched to aid in planarization. No problems were found in any of these layers (the apparent voids shown in the photos are delineation artifacts).

• Pre-metal dielectric: Borophosphosilicate glass (BPSG) over various densified oxides was used under Metal 1. Reflow was performed prior to contact cuts only. No problems were found.

• Contact defects: Via and contact cuts appeared to be defined by a two step process. No over-etching of the contacts or vias was noted.
ANALYSIS RESULTS II (continued)

• A single layer of poly (no silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by dry-etch of normal quality.

• Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with nitride sidewall spacers left in place. No problems were found.

• Local oxide (LOCOS) isolation was used. The step present at the well boundary indicates a twin-well process was employed.

• The memory cell array utilized a 6T SRAM cell. Metal 2 was used to form the bit lines and distribute GND (via Metal 1). Metal 1 was used to form “piggyback” word lines, provide cell interconnect, and distribute Vcc. Poly was used to form word lines and all gates. Cell pitch was 9.5 x 13 microns.

• Redundancy fuses were not present on the die.
PROCEDURE

The devices were subjected to the following analysis procedures:

- External inspection
- X-ray
- Package section and EDX
- Decapsulate
- Internal optical inspection
- SEM of passivation and assembly features
- Passivation integrity test
- Wirepull test
- Passivation removal
- Delayer to metal 2 and inspect
- Metal 2 removal and inspect barrier
- Delayer to metal 1 and inspect
- Metal 1 removal and inspect barrier
- Delayer to silicon and inspect poly/die surface
- Die sectioning (90° for SEM)*
- Die material analysis
- Measure horizontal dimensions
- Measure vertical dimensions

*Delineation of cross-sections is by silicon etch unless otherwise indicated.
**OVERALL QUALITY EVALUATION:** Overall Rating: Normal/Poor

**DETAIL OF EVALUATION**

<table>
<thead>
<tr>
<th>Category</th>
<th>Rating</th>
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</thead>
<tbody>
<tr>
<td>Package integrity</td>
<td>N</td>
</tr>
<tr>
<td>Package markings</td>
<td>N</td>
</tr>
<tr>
<td>Die placement</td>
<td>N</td>
</tr>
<tr>
<td>Wirebond placement</td>
<td>N</td>
</tr>
<tr>
<td>Wire spacing</td>
<td>N</td>
</tr>
<tr>
<td>Wirebond quality</td>
<td>N</td>
</tr>
<tr>
<td>Die attach quality</td>
<td>N</td>
</tr>
<tr>
<td>Dicing quality</td>
<td>N</td>
</tr>
<tr>
<td>Die attach method</td>
<td>Silver-epoxy</td>
</tr>
<tr>
<td>Dicing method</td>
<td>Sawn (full depth)</td>
</tr>
<tr>
<td>Wirebond method</td>
<td>Thermosonic ball bonds using 1.0 mil gold wire.</td>
</tr>
<tr>
<td>Die surface integrity:</td>
<td></td>
</tr>
<tr>
<td>Toolmarks (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Particles (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Contamination (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Process defects (absence)</td>
<td>G</td>
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<tr>
<td>General workmanship</td>
<td>N</td>
</tr>
<tr>
<td>Passivation integrity</td>
<td>G</td>
</tr>
<tr>
<td>Metal definition</td>
<td>N</td>
</tr>
<tr>
<td>Metal integrity</td>
<td>P(^1)</td>
</tr>
<tr>
<td>Metal registration</td>
<td>N</td>
</tr>
<tr>
<td>Contact coverage</td>
<td>N</td>
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<tr>
<td>Contact registration</td>
<td>N</td>
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\(^1\)Metal 2 aluminum thinning up to 90 percent, Metal 1 aluminum thinning up to 85 percent.

\(G = \text{Good}, \ P = \text{Poor}, \ N = \text{Normal}, \ NP = \text{Normal/Poor}\)
PACKAGE MARKINGS (TOP)

XC56002PV80
1F87L
HEA09552

(BOTTOM)

HONG KONG

WIREBOND STRENGTH

Wire material: 1.0 mil O.D. gold
Die pad material: aluminum

<table>
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<tr>
<th>Sample #</th>
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<th>2</th>
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<tr>
<td># of wires pulled:</td>
<td>31</td>
<td>31</td>
</tr>
<tr>
<td>Bond lifts:</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Force to break - high:</td>
<td>9g</td>
<td>10g</td>
</tr>
<tr>
<td>- low:</td>
<td>5g</td>
<td>4g</td>
</tr>
<tr>
<td>- avg.:</td>
<td>6.8g</td>
<td>5.7g</td>
</tr>
<tr>
<td>- std. dev.:</td>
<td>1.1</td>
<td>1.3</td>
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</table>
PACKAGE MATERIAL ANALYSIS (EDX)

Leadframe: Copper (Cu)  
Internal plating: Silver (Ag)  
External plating: Tin-lead (SnPb) solder  
Die attach: Silver (Ag) epoxy  

DIE MATERIAL ANALYSIS

Overlay passivation: A layer of silicon-nitride over a layer of silicon-dioxide.  
Metallization 2: Aluminum (Al) with a titanium-nitride (TiN) cap with no barrier.  
Interlevel dielectric: Two layers of silicon.  
Metallization 1: Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.  
Pre-metal dielectric: BPSG containing 6.7 wt. % phosphorus and 2.6 wt. % boron.
**HORIZONTAL DIMENSIONS**

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die size</td>
<td>6.5 x 6.5 mm (254 x 254 mils)</td>
</tr>
<tr>
<td>Die area</td>
<td>42.3 mm² (64,515 mils²)</td>
</tr>
<tr>
<td>Min pad size</td>
<td>0.12 x 0.15 mm (4.7 x 5.9 mils)</td>
</tr>
<tr>
<td>Min pad window</td>
<td>0.11 x 0.11 mm (4.2 x 4.2 mils)</td>
</tr>
<tr>
<td>Min pad space</td>
<td>45 microns</td>
</tr>
<tr>
<td>Min metal 2 width</td>
<td>1.1 micron</td>
</tr>
<tr>
<td>Min metal 2 space</td>
<td>0.9 micron</td>
</tr>
<tr>
<td>Min metal 2 pitch</td>
<td>2.0 microns</td>
</tr>
<tr>
<td>Min metal 1 width</td>
<td>0.7 micron</td>
</tr>
<tr>
<td>Min metal 1 space</td>
<td>0.7 micron</td>
</tr>
<tr>
<td>Min metal 1 pitch</td>
<td>1.4 micron</td>
</tr>
<tr>
<td>Min via (M2 - M1)</td>
<td>1.1 micron (diameter)</td>
</tr>
<tr>
<td>Min contact</td>
<td>0.9 micron</td>
</tr>
<tr>
<td>Min poly width</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>Min poly space</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>Min gate length - (N-channel):*</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>- (P-channel)</td>
<td>0.7 micron</td>
</tr>
<tr>
<td>Cell pitch</td>
<td>9.5 x 13 microns</td>
</tr>
<tr>
<td>Cell size</td>
<td>124 microns</td>
</tr>
</tbody>
</table>

*Physical gate length*
VERTICAL DIMENSIONS

Die thickness: 0.35 mm (13.8 mils)

Layers:

Passivation 2: 0.6 micron
Passivation 1: 0.4 micron
Metal 2 - cap: 0.06 micron (approximate)
    - aluminum: 1.0 micron
Interlevel dielectric - glass 2: 0.25 micron
    - glass 1: 0.25 - 0.65 micron
Metal 1 - cap: 0.05 micron (approximate)
    - aluminum: 0.7 micron
    - barrier: 0.1 micron
Pre-metal dielectric: 0.2 - 0.55 micron
Oxide on poly: 0.15 micron
Poly: 0.25 micron
Local oxide: 0.5 micron
N+ S/D: 0.3 micron
P + S/D: 0.4 micron
N-well: 5.5 microns (approximate)
P-well: Could not delineate
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Mag. 26,000x

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Mag. 13,000x

Mag. 26,000x
Mag. 26,000x

Mag. 40,000x

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metal 1-to-N+

metal 1-to-P+

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