Construction Analysis

SGS-Thomson 93C46CB1
1K EEPROM

Report Number: SCA 9612-519
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INTRODUCTION

This report describes a construction analysis of the SGS-Thomson 93C46CB1 1K EEPROM. Four devices packaged in 8-pin Plastic Dual In-line Packages (PDIPs) were received for the analysis. Date codes were not identifiable (possibly 9618).

MAJOR FINDINGS

Questionable Items: ¹ None.

Special Features:

- Twin-well CMOS process with single poly and tunnel oxide windows.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
TECHNOLOGY DESCRIPTION

Assembly:

- Devices were packaged in 8-pin Plastic Dual In-line Packages (PDIPs).

- The dice were mounted to the paddles using a silver-filled polyimide die attach.

- Die separation was by sawing.

- Wirebonding was by the thermosonic ball bond method using 1.1 mil O.D. gold wire.

- All pins were connected. Lead-locking provisions (anchors) at all pins.

Die Process:

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.

- No die coat was present.

- Passivation consisted of a layer of oxy-nitride over a layer of silicon-dioxide.

- Metallization consisted of a single layer of dry-etched aluminum and did not use a cap or barrier. Standard contacts were used (no plugs).

- Pre-metal dielectric consisted of a layer of borophosphosilicate glass (BPSG) over densified oxides. The glass was refloved following contact cuts.

- A single layer of poly (no silicide) was used to form all gates on the die, the word lines and one plate of the capacitors in the EEPROM cell array. Direct poly-to-diffusion (buried) contacts were not used. Definition of the poly was by a dry etch.
TECHNOLOGY DESCRIPTION (continued)

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Local oxide (LOCOS) isolation. A slight step was present in the oxide at the edge of the well boundaries indicating a twin-well process was used.

- The memory cell consisted of a 3T, single capacitor, EEPROM design. Metal was used to form the bit lines. Poly was used to form the word/select lines, one plate of the capacitor and the tunnel-oxide device.

- Two separate small MROM arrays were also present. One of these used poly mask programming, the other field oxide mask (i.e., diffusion) programming.

- Redundancy fuses were not present.
ANALYSIS RESULTS I

Package and Assembly:  
Figures 1 - 6

Questionable Items: ¹ None.

Special Features:  None.

General Items:

- Devices were packaged in 8-pin Plastic Dual In-line Packages (PDIPs).

- Overall package quality: Good. No significant defects were noted on the external or internal portions of the package. No cracks or voids were noted in the plastic.

- Leadframe: The leadframe was constructed of copper.

- Die dicing: Die separation was by sawing of normal quality. No large cracks or chips were present.

- Die attach: A silver-filled polyimide of normal quality was used to attach the die to the paddle.

- Wirebonding was by the thermosonic ball bond method using 1.1 mil O.D. gold wire. Bonds were well formed and placement was good. Wirepull strengths were normal with no bond lifts (see page 10).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

Die Process:  

Figures 7 - 33

Questionable Items:¹ None.

Special Features:

• Single poly, tunnel oxide windows.

General Items:

• Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.

• Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.

• Die coat: No die coat was present.

• Overlay passivation: A layer of oxy-nitride over a layer of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good as it extended into the scribe lane to seal the metallization.

• Metallization: A single layer of metal consisting of aluminum. No cap or barrier metals were used.

• Metal patterning: The metal layer was patterned by a dry etch of normal quality. All contacts were completely surrounded by aluminum.

• Metal defects: No voiding, notching, or neckdown was noted in the metal layer. No silicon nodules were noted following the removal of the aluminum layer.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II (continued)

• Metal step coverage: Worst case aluminum thinning was 65 percent at contact edges. Typical aluminum thinning was 50 percent. MIL-STD allows up to 70 percent metal thinning for contacts of this size.

• Pre-metal dielectric: A layer of borophosphosilicate glass (BPSG) over densified oxides was used under the metal. Reflow was performed following contact cuts. No problems were found.

• Contact defects: None. Alignment was good and no significant over-etching of the contacts was noted.

• Polysilicon: A single layer of poly (no silicide) was used to form all gates, word lines, and one plate of the capacitors in the EEPROM cell array. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

• Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No silicide was present over diffusions.

• Local oxide (LOCOS) isolation was used. No problems were noted. The slight step present in the oxide at the well boundary indicates a twin-well process was employed. The P-well could not be delineated in cross section.

• ROM arrays: Two different MROM array types were present on the device. Both were located at one end of the die. One array was programmed at the poly level (see Figures 21 and 22) and the other array was programmed at the diffusion level (see Figures 23 and 24).

• EEPROM: The EEPROM memory cells used three transistor, single capacitor EEPROM design. Metal was used to form the bit lines. Poly was used to form the word/select lines, one plate of the capacitor, and the tunnel oxide device. Cell pitch was 7.8 x 18.4 microns.

• Redundancy fuses were not present on the die.
**PROCEDURE**

The devices were subjected to the following analysis procedures:

- External inspection
- X-ray
- Decapsulate
- Internal optical inspection
- SEM of passivation and assembly features
- Passivation integrity test
- Wirepull test
- Passivation removal
- SEM inspection of metal
- Metal removal
- Delayer to silicon and inspect poly/die surface
- Die sectioning (90° for SEM)*
- Die material analysis
- Measure horizontal dimensions
- Measure vertical dimensions

*Delineation of cross-sections is by silicon etch unless otherwise indicated.*
OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package integrity N
Package markings N
Die placement N
Wirebond placement N
Wire spacing N
Wirebond quality N
Die attach quality N
Dicing quality N
Die attach method Silver-filled polyimide
Dicing method Sawn
Wirebond method Thermosonic ball bonds using 1.1 mil gold wire.

Die surface integrity:
  Toolmarks (absence) G
  Particles (absence) G
  Contamination (absence) G
  Process defects (absence) G
General workmanship G
Passivation integrity G
Metal definition N
Metal integrity N
Contact coverage G
Contact registration G

G = Good, P = Poor, N = Normal, NP = Normal/Poor
PACKAGE MARKINGS (TOP)

93C46CB1
91E618
(LOGO ) MAL

(BOTTOM)

NONE

WIREBOND STRENGTH

Wire material: 1.1 mil O.D. gold
Die pad material: aluminum

Sample #

1

# of wires pulled: 8
Bond lifts: 0
Force to break - high: 9.5g
- low: 4.5g
- avg.: 7.5g
- std. dev.: 1.6

DIE MATERIAL ANALYSIS

Overlay passivation: A layer of oxy-nitride over a layer of silicon-dioxide.

Metallization:* Aluminum (Al).

Pre-metal dielectric: A layer of borophosphosilicate glass (BPSG) containing 3.4 wt. % phosphorus and 3.6 wt. % boron over various densified oxides.

*There is no known method for determining the exact amount of silicon or copper in the aluminum of a finished die.
HORIZONTAL DIMENSIONS

Die size: 1.4 x 1.8 mm (56 x 72 mils)
Die area: 2.6 mm² (4,032 mils²)
Min pad size: 0.12 x 0.12 mm (4.7 x 4.7 mils)
Min pad window: 0.11 x 0.11 mm (4.3 x 4.3 mils)
Min pad space: 0.08 mm (3.1 mils)
Min metal width: 1.7 micron
Min metal space: 1.6 micron
Min metal pitch: 3.3 microns
Min contact: 1.1 micron
Min poly width: 1.2 micron
Min poly space: 1.4 micron
Min gate length - (N-channel):* 1.2 micron
- (P-channel): 1.3 micron
Cell size: 143 microns²
Cell pitch: 7.8 x 18.4 microns

VERTICAL DIMENSIONS

Die thickness: 0.5 mm (19.5 mils)

Layers:

Passivation 2: 0.6 micron
Passivation 1: 0.4 micron
Metal: 0.85 micron
Pre-metal dielectric: 0.4 micron (avg.)
Oxide on poly: 0.25 micron
Poly: 0.4 micron
Local oxide: 0.6 micron
N+ S/D: 0.3 micron
P + S/D: 0.5 micron
N-well: 3 microns
P-well: Could not delineate

*Physical gate length
Figure 1. Package photograph and pinout diagram of the SGS-Thomson 93C46CB1 1Kbit EEPROM. Mag. 7.5x.
Figure 2. X-ray views of the package. Mag. 8x.
Figure 3.  Perspective SEM view of a typical ball bond.  Mag. 600x. 60°.

Figure 4.  SEM section views of the bond pad.
Figure 5. SEM views of die corner and edge seal. 60°.
Figure 6. SEM views of the edge seal.
Figure 7. Whole die photograph of the SGS-Thomson 93C46CB1 EEPROM. Mag. 120x.
Figure 8. Identification markings from the die surface. Mag. 400x.
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Mag. 6200x

Mag. 13,000x
Figure 10. SEM views of overlay passivation coverage. 60°.
Figure 11. SEM section views of metal line profiles.
Figure 12. Topological SEM views illustrating metal patterning. 0°.
Figure 13. Perspective SEM views illustrating metal coverage. 60°.
metal-to-N+, Mag. 20,000x

metal-to-P+, Mag. 20,000x

metal-to-poly, Mag. 26,000x

Figure 14. SEM section views of metal contacts.
Figure 14a. Perspective SEM views of circular devices. 60°.
Figure 15. Topological SEM views illustrating poly patterning. 0°.
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Figure 17. SEM section views illustrating typical gates. Mag. 26,000x.
Figure 18. SEM section view of a local oxide birdsbeak profile. Mag. 26,000x.

Figure 19. Optical and SEM views illustrating well structure.
Figure 20. Color cross section drawing illustrating device structure.

Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate
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Figure 32. SEM section views of EEPROM cells (perpendicular to bit lines).
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