Construction Analysis

Hitachi HM5293206FP10 8Mbit SGRAM

Report Number: SCA 9702-529
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INTRODUCTION

This report describes a construction analysis of the Hitachi HM5283206FP10, 8 Meg SGRAM. One device packaged in a 100-pin plastic QFP package was received for the analysis. The package was date coded 9625.

MAJOR FINDINGS

Questionable Items: These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

None.

Special Features:

• Sub-micron gate lengths (0.35 micron, in array).

• Stacked capacitor DRAM cell design.

• Four layers of poly (three layers effective).

• Tungsten metal 1.
TECHNOLOGY DESCRIPTION

Die Process and Design

• Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-substrate (no epi was used).

• Final passivation: A thick layer of nitride over a layer of glass.

• Metallization: Metal 2 and 3 consisted of aluminum defined by a dry-etch technique. Both metals employed a titanium-nitride cap and barrier. Metal 1 consisted of tungsten with a titanium-nitride barrier. Tungsten plugs were used at Metal 3 and Metal 2 vias. Standard contacts were used in the periphery and poly plugs were used at metal 1 bit contacts in the array. Metal 3 employed beveled corners and multiple contact arrays.

• Intermetal dielectric 1 and 2: Both intermetal dielectrics (IMD 1 and IMD 2) consisted of the same dielectric structure. A layer of glass followed by a spin-on-glass (SOG) and another layer of glass. The SOG layer had been subjected to an etchback.

• Pre-metal dielectric: A single thick layer of reflow glass over a densified oxide.

• Polysilicon: Four layers of polysilicon (three effective) were employed. Poly 3 (sheet) and Poly 2 (which uses two poly depositions) were used exclusively in the cell array and formed the plates of the capacitors. Poly 1 formed all gates and word lines on the die. No silicides were used with any of the poly layers.
TECHNOLOGY DESCRIPTION (continued)

• Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Combination nitride/oxide sidewall spacers were used for the LDD process. Nitride sidewalls were partially removed.

• Wells: Twin-wells in a P-substrate (no epi). A step in the local oxide was noted at the edge of the well boundaries. This step indicates a twin-well process was employed although, the P-well could not be delineated.

• Fuses: All Poly 1 redundancy fuses had passivation and oxide cutouts over them. No blown fuses were present. Guardband diffusions were present around the fuse blocks.

• Memory cells: Stacked capacitor DRAM design. Metal 2 formed “piggyback” word lines and metal 1 distributed the bit lines. Metal 3 was not used directly with the cells. Three layers of polysilicon were employed. Poly 3 (sheet) was used to form the common plate of the capacitors and was tied to memory enable. Poly 2 formed the individual plate of the capacitors. As mentioned, Poly 2 is made using two separate depositions (one for each “wing” of the cell plate); but we refer to all of it as Poly 2 for convenience. Poly 1 provided word lines/select gates.
ANALYSIS RESULTS

Die Process and Design: 

Figures 1 - 46b

Questionable Items:¹ None.

Special Features:

• Sub-micron gate lengths (0.35 micron, in array).

• Stacked capacitor DRAM cell design.

• Four layers of poly (counted as three).

• Tungsten metal 1.

General Items:

• Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-substrate (no epi was used). No significant problems were found in the process.

• Design implementation: Die layout was clean and efficient. Alignment was good at all levels.

• Surface defects: No toolmarks, masking defects, or contamination areas were found.

• Final passivation: A thick layer of nitride over a layer of glass. Passivation integrity tests indicated defect-free passivation. Edge seal was also good.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS (continued)

• Metallization: Metal 2 and 3 consisted of aluminum defined by a dry-etch technique. Both metals employed a titanium cap and barrier. Metal 1 consisted of tungsten with a titanium-nitride barrier. Tungsten plugs were used at Metal 3 and Metal 2 vias. Standard contacts were used in the periphery and poly plugs were used at Metal 1 bit contacts in the array.

• Metal patterning: All three metal layers were defined by a dry-etch of good quality.

• Metal defects: None. No notching of voiding of the metal layers was found. No silicon nodules were found following removal of the aluminum.

• Metal step coverage: No significant thinning of Metal 2 or 3 was noted, due to the use of tungsten plugs. Virtually no Metal 1 tungsten thinning was present at contacts in the periphery and no thinning was present in the array due to the use of poly plugs.

• Vias and contacts: Via and contact cuts appeared to be defined by a dry etch. No over-etching or other contact problems were found. Multiple contact arrays were employed.

• Intermetal dielectrics 1 and 2: Both intermetal dielectrics (between M3-M2 and M2-M1) consisted of a layer of glass followed by a spin-on-glass (SOG) for planarization, and another layer of glass. The SOG layer had been subjected to an etchback. No problems were found with these layers.

• Pre-metal dielectric: A single layer of reflow glass (BPSG) over a densified oxide in peripheral circuit areas and in the memory array.
ANALYSIS RESULTS (continued)

- Polysilicon: Four layers of polysilicon were employed. Poly 3 (sheet) and Poly 2 (two layers) were used exclusively in the cell array and formed the plates of the capacitors. Poly 1 formed all gates and word lines on the die. No silicides were used with any layers. Poly 1 “neckdown” was noted at the gate/local oxide transition. Although this indicates somewhat poor definition control no problems are anticipated.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was present in the local oxide at the well boundaries. This indicates a twin-well process was employed.

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Combination oxide/nitride sidewall spacers were used for the LDD process. Nitride sidewalls were partially removed. No problems were found in any of these areas.

- Wells: Twin-wells were used in a P substrate (no epi was present). The P-well could not be delineated. No problems were found.

- Fuses: All Poly 1 redundancy fuses had passivation and oxide cutouts over them. No blown fuses were present. Guardband diffusions were present around the fuse blocks.

- Memory cells: Stacked capacitor DRAM design. Metal 2 formed “piggyback” word lines and Metal 1 distributed the bit lines. Three layers of polysilicon were employed. Poly 3 was used to form the common plate of the capacitors (sheet) and was tied to memory enable. Poly 2 formed the dual individual plates of the capacitors. As mentioned, Poly 2 consisted of two separate layers connected together. Poly 1 formed all gates and word lines. Definition was good and no problems were noted. Cell pitch was 1.1 x 1.9 micron (2.1 microns^2).
PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection
X-ray
Decapsulate
Internal optical inspection
SEM inspection of passivation
Passivation integrity test
Delayer to metal 3 and inspect
Aluminum removal (metal 3)
Delayer to metal 2 and inspect
Aluminum removal (metal 2)
Delayer to metal 1 and inspect
Delayer to poly/substrate and inspect poly and substrate
Die sectioning (90° for SEM)*
Measure horizontal dimensions
Measure vertical dimensions
Die material analysis

*Delineation of cross-sections is by silicon etch unless otherwise indicated.
OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Die surface integrity:

- Toolmarks (absence) G
- Particles (absence) G
- Contamination (absence) G
- Process defects (absence) NP*

General workmanship G
Passivation integrity G
Metal definition N
Metal integrity N
Metal registration G
Contact coverage G
Contact registration G

*Neckdown of poly 1 gates.

G = Good, P = Poor, N = Normal, NP = Normal/Poor
PACKAGE MARKINGS

TOP

(logo) HM5283206FP10
JAPAN 9625
0003933

BOTTOM (Molded)

32 DC

DIE MATERIAL ANALYSIS

Overlay passivation: A thick layer of nitride over a layer of glass.
Metallization 2 and 3: Aluminum with a titanium-nitride cap and barrier.
Intermetal dielectrics (IMD1 and IMD2): Two layers of silicon-dioxide with a filler glass (SOG) between.
Metallization 1: Tungsten with a titanium-nitride (TiN) barrier.
Pre-metal glass: A single layer of reflow glass over a densified oxide.
HORIZONTAL DIMENSIONS

Die size: 7.5 x 7.8 mm (295 x 308 mils)
Die area: 58 mm² (90,860 mils²)
Min pad size: 0.11 x 0.11 mm (4.5 x 4.5 mils)
Min pad window: 0.1 x 0.1 mm (4.1 x 4.1 mils)
Min pad space: 0.05 mm (2 mils)
Min metal 3 width: 1.0 micron
Min metal 3 space: 1.0 micron
Min metal 3 pitch: 2.0 microns
Min via 2: 0.6 micron
Min metal 2 width: 0.6 micron
Min metal 2 space: 0.6 micron
Min metal 2 pitch: 1.2 micron
Min via 1: 0.6 micron
Min metal 1 width: 0.3 micron
Min metal 1 space: 0.6 micron
Min metal 1 pitch: 0.9 micron
Min contact: 0.5 micron
Min poly 2 width: 0.6 micron
Min poly 2 space: 0.5 micron
Min poly 1 width - (cell): 0.35 micron
Min poly 1 space: 0.45 micron
Min gate length* - (N-channel): 0.35 micron (in cell)
- (N-channel): 0.5 micron (in periphery)
- (P-channel): 0.5 micron
Cell area: 2.1 microns²
Cell size: 1.1 x 1.9 micron

*Physical gate length.
## VERTICAL DIMENSIONS

### Layers

<table>
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<tr>
<td>Passivation 2:</td>
<td>1.2 micron</td>
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<tr>
<td>Passivation 1:</td>
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<tr>
<td>Metal 3 - cap:</td>
<td>0.07 micron</td>
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<tr>
<td>- aluminum</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>- barrier</td>
<td>0.1 micron</td>
</tr>
<tr>
<td>- plugs</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>Intermetal dielectric 2 - glass 2:</td>
<td>0.35 micron</td>
</tr>
<tr>
<td>- SOG:</td>
<td>0 - 0.55 micron</td>
</tr>
<tr>
<td>- glass 1:</td>
<td>0.35 micron</td>
</tr>
<tr>
<td>Metal 2 - cap:</td>
<td>0.1 micron</td>
</tr>
<tr>
<td>- aluminum:</td>
<td>0.35 micron</td>
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<tr>
<td>- barrier:</td>
<td>0.1 micron</td>
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<tr>
<td>- plugs:</td>
<td>0.7 micron</td>
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<tr>
<td>Intermetal dielectric 1 - glass 2:</td>
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</tr>
<tr>
<td>- SOG:</td>
<td>0 - 0.4 micron</td>
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<td>- glass 1:</td>
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<td>Metal 1 - tungsten</td>
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<td>- barrier:</td>
<td>0.1 micron</td>
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<td>Reflow glass:</td>
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<td>Poly 3 (sheet):</td>
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<td>Poly 2 - 2nd layer:</td>
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<td>- 1st layer:</td>
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<td>Poly 1:</td>
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<td>Local oxide:</td>
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<td>N+ S/D diffusion:</td>
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<tr>
<td>P+ S/D diffusion:</td>
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<tr>
<td>N-well:</td>
<td>5 microns</td>
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Mag. 26,000x

Mag. 52,000x
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Mag. 31,000x
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poly 3

poly 1 and 2

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