Construction Analysis

Samsung KM4132G271Q-10
8Mb SGRAM

Report Number: SCA 9702-530
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INTRODUCTION

This report describes a construction analysis of the Samsung KM4132G271Q-10, 8 Meg SGRAM. One device packaged in a 120-pin plastic PQFP package was received for the analysis. Package was date coded 546Y (9546).

MAJOR FINDINGS

Questionable Items:\(^1\)

- Metal 2 aluminum thinning up to 85 percent\(^2\) at vias (Figure 14).

Special Features:

- Sub-micron gate lengths (0.45 micron).
- Stacked capacitor DRAM cell design.
- Five layers of poly (four layers effective).
- Reflowed aluminum 1 contacts.

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
TECHNOLOGY DESCRIPTION

Die Process and Design

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P-substrate (no epi was used). No evidence of P-wells was found but this does not rule out their possible presence.

- Final passivation: A layer of nitride over a thin layer of glass.

- Metallization: Metal 2 consisted of silicon-doped aluminum defined by a dry-etch technique. Metal 2 did not use a cap or barrier. Metal 1 consisted of aluminum and employed a titanium-nitride cap and barrier. Standard vias and aluminum-filled (reflowed) contacts were employed. Special patterning of metal 2 and 1 bus lines was used at the corners of the die. Both metals employed slotted lines, beveled (angled) lines at corners and multiple contact arrays. Metal 2 also contained some cutouts.

- Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of a multilayered glass followed by a spin-on glass (SOG) and another layer of glass.

- Pre-metal dielectric: A single layer of reflow glass over a densified oxide.

- Polysilicon: Five layers of polysilicon were employed. Polycide 4 (poly 4 and tungsten silicide) was used to form bit lines and general interconnect in the peripheral circuitry. Polycide 4 contacted poly 1 and N+ diffusions. Poly 3 (sheet) and Poly 2 (which uses 2 poly depositions) were used exclusively in the cell array and formed the plates of the capacitors. Poly 1 formed all gates and word lines on the die.
TECHNOLOGY DESCRIPTION (continued)

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Oxide sidewall spacers were used and were left in place.

- Wells: N-wells in a P-substrate (no epi). No step in the oxide was noted at the edge of N-wells. Although this is not an absolute indication of a single polarity well process it means we have no proof of twin-wells although it is probable a P-well exist in the cell array.

- Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present. (Figures 39 and 40).

- Memory cells: Four layers of polysilicon were employed. Polycide 4 (poly 4 and tungsten silicide) was used to form the bit lines. Poly 3 (sheet) was used to form the common plate of the capacitors and was tied to memory enable. Poly 2 formed the individual plate of the capacitors. As mentioned, Poly 2 is made using two separate depositions (one for each “wing” of the cell plate); but we refer to all of it as Poly 2 for convenience. Poly 1 provided word lines/select gates.
ANALYSIS RESULTS

Die Process and Design: Figures 8 - 43

Questionable Items:

1. Metal 2 aluminum thinning up to 85 percent at vias (Figure 14).

Special Features:

• Sub-micron gate lengths (0.45 micron).

• Stacked capacitor DRAM cell design.

• Five layers of poly (counted as 4).

• Reflowed aluminum 1 contacts.

General Items:

• Fabrication process: Selective oxidation CMOS process employing N-wells in a P-substrate (no epi was used). No evidence of P-wells was found but this does not rule out their possible presence. No significant problems were found in the process.

• Design implementation: Die layout was clean and efficient. Alignment was good at all levels.

• Surface defects: No toolmarks, masking defects, or contamination areas were found.

These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

Seriousness depends on design margins
ANALYSIS RESULTS (continued)

• Final passivation: A layer of nitride over a thin layer of glass. Passivation integrity tests indicated defect-free passivation. Edge seal was also good.

• Metallization: Metal 2 consisted of silicon-doped aluminum defined by a dry-etch technique. It did not use a cap or barrier. Metal 1 consisted of aluminum and employed a titanium-nitride cap and barrier. Standard vias (M2-to-M1) and reflowed aluminum contacts (M1-to-silicon) were employed. Both metals employed beveled/angled corners and multiple contact arrays on the corners and edges of the die. Metal 2 and 1 patterned structures were used around the bonding pads.

• Metal patterning: Both metal layers were defined by a dry-etch of good quality.

• Metal defects: None. No notching of voiding of the metal layers was found. No silicon nodules were found following removal of the aluminum.

• Metal step coverage: Metal 2 aluminum thinned up to 85 percent at vias. Typical metal 2 thinning was 80 percent. Military standards allow up to 70 percent metal thinning at contacts of this size. Virtually no metal 1 thinning was present due to the use of aluminum reflow at contacts.

• Vias and contacts: Via and contact cuts appeared to be defined by a two-step etch. No excessive over-etching or other problems were found. Both metals employed multiple contact arrays.

• Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of a multilayered glass followed by a spin-on glass (SOG) for planarization, and another layer of glass. No problems were found with these layers.
ANALYSIS RESULTS (continued)

• Pre-metal dielectric: A single layer of reflow glass (BPSG) over a densified oxide in peripheral circuit areas and in the memory array.

• Polysilicon: Five layers of polysilicon were employed. Polycide 4 (poly 4 and tungsten silicide) was used to form bit lines in the array and general interconnect in the peripheral circuitry. Polycide 4 contacted poly 1 and N+ diffusions. Poly 3 (sheet) and Poly 2 (two layers) were used exclusively in the cell array and formed the plates of the capacitors. Poly 1 formed all gates and word lines on the die. Definition was good at all layers and no problems were noted.

• Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. No step was present in the local oxide at the well boundaries.

• Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Sidewall spacers were used and left in place. No problems were found in any of these areas.

• Wells: N-wells were used in a P substrate (no epi was present). No step in the oxide was noted at the edge of the N-wells (indication of twin-well process) and no problems were found. A P-well if present could not be delineated.

• Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present.

• Memory cells: Five layers of polysilicon were employed. Polycide 4 was used to form the bit lines. Poly 3 was used to form the common plate of the capacitors (sheet) and was tied to memory enable. Poly 2 formed the dual individual plates of the capacitors. (As mentioned, poly 2 consisted of two separate layers connected together.) Poly 1 formed all gates and word lines. Definition was good and no problems were noted. Cell pitch was 1.1 x 2.5 microns (2.75 microns²).
PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection
X-ray
Decapsulate
Internal optical inspection
SEM inspection of passivation
Passivation integrity test
Delayer to metal 2 and inspect
Aluminum removal (metal 2)
Delayer to metal 1 and inspect
Aluminum removal (metal 1)
Delayer to poly/substrate and inspect poly and substrate
Die sectioning (90° for SEM)*
Measure horizontal dimensions
Measure vertical dimensions
Die material analysis

*Delineation of cross-sections is by silicon etch unless otherwise indicated.
OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Die surface integrity:

- Toolmarks (absence) G
- Particles (absence) G
- Contamination (absence) G
- Process defects (absence) G

General workmanship G
Passivation integrity G
Metal definition N
Metal integrity NP*
Metal registration G
Contact coverage G
Contact registration G

*85 percent metal 2 aluminum thinning.

G = Good, P = Poor, N = Normal, NP = Normal/Poor
PACKAGE MARKINGS

TOP

SEC KOREA
546Y
KM4132G271Q-10

BOTTOM

5PG017THF

DIE MATERIAL ANALYSIS

Overlay passivation: A layer of nitride over a thin layer of glass.

Metallization 2: Aluminum.

Intermetal dielectric (IMD): Two layers of silicon-dioxide with a filler glass (SOG) between.

Metallization 1: Aluminum with a titanium-nitride (TiN) cap and barrier.

Pre-metal glass: A single layer of reflow glass over a densified oxide.

Polycide: Tungsten-silicide.
## HORIZONTAL DIMENSIONS

<table>
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<tr>
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<tr>
<td>Die size:</td>
<td>6.8 x 9.0 mm (267 x 354 mils)</td>
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<tr>
<td>Die area:</td>
<td>61 mm² (94,518 mils²)</td>
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<tr>
<td>Min pad size:</td>
<td>0.11 x 0.11 mm (4.5 x 4.5 mils)</td>
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<tr>
<td>Min pad window:</td>
<td>0.1 x 0.1 mm (4 x 4 mils)</td>
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<td>Min pad space:</td>
<td>0.1 mm (4 mils)</td>
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<tr>
<td>Min metal 2 space:</td>
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</tr>
<tr>
<td>Min via:</td>
<td>1.0 micron</td>
</tr>
<tr>
<td>Min via space:</td>
<td>1.3 micron</td>
</tr>
<tr>
<td>Min via pitch:</td>
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</tr>
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<td>Min metal 1 width:</td>
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</tr>
<tr>
<td>Min metal 1 space:</td>
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<tr>
<td>Min metal 1 pitch:</td>
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</tr>
<tr>
<td>Min contact:</td>
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<td>Min contact pitch:</td>
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<tr>
<td>Min polycide 4 width:</td>
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<td>Min poly 3 width:</td>
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<td>Min poly 2 space:</td>
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<td>Min poly 1 width - (cell):</td>
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<tr>
<td>Min poly 1 pitch:</td>
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<tr>
<td>Min gate length* - (N-channel):</td>
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<td>- (P-channel):</td>
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<tr>
<td>Cell size:</td>
<td>2.75 microns²</td>
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<tr>
<td>Cell pitch:</td>
<td>1.1 x 2.5 microns</td>
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</tbody>
</table>

*Physical gate length.
VERTICAL DIMENSIONS

Die thickness: 0.3 mm (11 mils)

Layers

Passivation 2: 0.55 micron
Passivation 1: 0.15 micron
Metal 2 - aluminum: 0.8 micron
Intermetal dielectric - glass 3: 0.4 micron
- glass 2 (SOG): 0 - 0.7 micron
- glass 1: 0.45 micron
Metal 1 - cap: 0.05 micron (approximate)
- aluminum: 0.6 micron
- barrier: 0.1 micron
Reflow glass: 0.6 micron
Polycide 4: 0.25 micron
Poly 3 (sheet): 0.1 micron (approximate)
Poly 2 - 2nd layer: 0.06 micron
- 1st layer: 0.15 micron
Poly 1: 0.15 micron
Local oxide: 0.35 micron
N+ S/D diffusion: 0.2 micron
P+ S/D diffusion: 0.25 micron
N-well: 2 microns
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