Construction Analysis

Mosel Vitelic MS62256CLL-70PC
256Kbit SRAM

Report Number: SCA 9703-499
# INDEX TO TEXT

<table>
<thead>
<tr>
<th>TITLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>MAJOR FINDINGS</td>
<td>1</td>
</tr>
<tr>
<td>TECHNOLOGY DESCRIPTION</td>
<td></td>
</tr>
<tr>
<td>Assembly</td>
<td>2</td>
</tr>
<tr>
<td>Die Process</td>
<td>2 - 3</td>
</tr>
<tr>
<td>ANALYSIS RESULTS I</td>
<td></td>
</tr>
<tr>
<td>Assembly</td>
<td>4</td>
</tr>
<tr>
<td>ANALYSIS RESULTS II</td>
<td></td>
</tr>
<tr>
<td>Die Process and Design</td>
<td>5 - 7</td>
</tr>
<tr>
<td>ANALYSIS PROCEDURE</td>
<td>8</td>
</tr>
<tr>
<td>TABLES</td>
<td></td>
</tr>
<tr>
<td>Overall Evaluation</td>
<td>9</td>
</tr>
<tr>
<td>Package Markings</td>
<td>10</td>
</tr>
<tr>
<td>Wirebond Strength</td>
<td>10</td>
</tr>
<tr>
<td>Die Material Analysis</td>
<td>10</td>
</tr>
<tr>
<td>Horizontal Dimensions</td>
<td>11</td>
</tr>
<tr>
<td>Vertical Dimensions</td>
<td>12</td>
</tr>
</tbody>
</table>
INTRODUCTION

This report describes a construction analysis of the MOSEL VITELIC MS62256CLL-70PC, 256Kbit SRAM. Two devices packaged in 28-pin Plastic Dual In-Line Packages (PDIPs) were received for the analysis. Devices were date coded 9543.

MAJOR FINDINGS

Questionable Items:

• Aluminum thinned up to 95 percent\(^1\) at contact edges. Barrier maintained contact and reduced overall thinning to 90 percent (Figure 14).

• Silicon nodules were noted occupying 53 percent\(^2\) of metal line width (Fig. 16). Nodules of equal size were also noted in contacts occupying 100 percent\(^1\) of the aluminum thickness (Fig. 16).

• Overlay passivation cussped over contact holes creating voids (Fig. 15).

Special Features:

• Sub-micron gate lengths (0.7 micron N- and 0.7 micron P-channel).

• Poly 2 contact pads over N+ diffusions.

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

\(^2\)Seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

**Assembly:**

- Devices were packaged in 28-pin Plastic Dual In-Line Packages (PDIPs).

- The leadframe was constructed of copper and plated externally with tin-lead solder and internally with silver.

- Die separation was by sawing (90 percent sawn). No cracks or chips were present at the die surface. Silver-filled epoxy was used to attach the die to the paddle.

- Lead-locking leadframe design (anchors) at all pins.

- Wirebonding was by the thermosonic ball bond method employing 1.1 mil O.D. gold wire.

- No multiple bond wires were present.

**Die Process:**

- Devices were fabricated using a selective oxidation, twin-well CMOS process in an N substrate. No epi was used.

- No die coat was present.

- Passivation consisted of a layer of nitride over a layer of glass. Overlay integrity tests indicated a defect-free passivation.

- A single level of aluminum on titanium-nitride on titanium was used for metal interconnect.
TECHNOLOGY DESCRIPTION (continued)

- Pre-metal dielectric consisted of a layer of reflow glass (probably BPSG) over densified oxides. The glass was reflowed prior to contact cuts only.

- Two layers of polysilicon were used on the die. Polycide 1 (poly 1 and tungsten silicide) was used to form all standard gates. Poly 2 was used in the cell array to form “pull-up” resistors and distribute Vcc. Poly 2 was also used to form fuse structures (Figures 22-24), and to form poly contact pads on N+ diffusions (Fig. 14). Direct poly 2-to-N+ diffusion (buried) contacts were used throughout the die. Definition of both poly layers was by a dry etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Local oxide (LOCOS) isolation. There was no evidence of a step at the well boundary but according to manufacturer’s data sheet, a twin-well process was employed on the device.

- A standard 4T NMOS SRAM cell design was used. Metal lines were used to form the bit lines, and to distribute Gnd. Poly 2 was used to form “pull-up” resistors and distribute Vcc. Polycide 1 was used to form all gates.

- Poly 2 fuses were present. No cutout was present over fuses, and the design appears to possibly use current to blow the fuses although this appearance may simply be misleading. No blown fuses were found.
ANALYSIS RESULTS

Package and Assembly:  

Figure 1 - 5

Questionable Items: None.

General Items:

- Devices were packaged in 28-pin Plastic Dual In-Line Packages (PDIPs).

- The leadframe was constructed of copper and plated externally with tin-lead solder and internally with silver. All pins were well formed and there were no gaps at the lead exits.

- Die separation was by sawing (90 percent sawn). No cracks or chips were present at the die surface. Silver-filled epoxy was used to attach the die to the header/paddle. No problems were found.

- Lead-locking leadframe design (anchors) at all pins.

- Wirebonding was by the thermosonic ball bond method employing 1.1 mil O.D. gold wire. Bonds were well formed and placement was good. No bond lifts occurred and bond pull strengths were good.

- No multiple bond wires were present.

- No die coat was employed.

These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

**Die Process:**

**Figures 6 - 32**

**Questionable Items:**

1. Aluminum thinned up to 95 percent\(^2\) at contact edges. Barrier maintained contact and reduced overall thinning to 90 percent (Figure 14).

2. Silicon nodules were noted occupying 53 percent\(^2\) of metal line width (Fig. 16). Nodules of equal size were also noted in contacts occupying 100 percent\(^1\) of the aluminum thickness (Fig. 16).

3. Overlay passivation cusped over contact holes creating voids (Fig. 15).

**Special Features:**

1. Sub-micron gate lengths (0.7 micron N- and 0.7 micron P-channel).

2. Poly 2 contact pads on N+ diffusions.

**General Items:**

1. Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in an N substrate. No epi was used.

2. Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

\(^2\)Seriousness depends on design margins.
ANALYSIS RESULTS II (continued)

- Die coat: No die coat was present.

- Overlay passivation: A layer of nitride over a layer of glass. Overlay integrity test indicated defect-free passivation. Edge seal was good.

- Metal integrity: The single layer of metal consisted of aluminum on a titanium-nitride on titanium barrier. No cap layer was used. The aluminum thinned up to 95 percent at some contact steps but the condition did not appear dangerous.

- Metal patterning: metal was patterned by a dry etch of normal quality. No special stress reducing designs were present at die corners.

- Metal defects: Silicon nodules were noted occupying 53 percent of line width and 56 percent of line thickness. Silicon nodules were also found in metal contacts occupying 100 percent of the aluminum thickness. Hillocks in the metal lines were also noted. Improvements in control of the metal process are desirable.

- Metal step coverage: Aluminum thinned up to 95 percent at contact edges. Total metal thinning (including barrier) was typically 80 percent.

- Pre-metal dielectric: A layer of reflow glass (probably BPSG) over various densified oxides was used. Reflow was performed prior to contact cuts only. No problems were found.

- Contact defects: Contact cuts were defined by a two step process. No over-etching of the contacts was noted.
ANALYSIS RESULTS II (continued)

- Two layers of polysilicon were used on the die. Polycide 1 (poly 1 and tungsten silicide) was used to form all standard gates. Poly 2 was used in the cell array to form “pull-up” resistors and distribute Vcc. Poly 2 was also used to form fuse structures (Figures 22-24), and to form poly pads over N+ diffusions. Direct poly 2-to-N+ diffusion (buried) contacts were used throughout the die. Definition of both poly layers was by a dry etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No problems were found.

- Local oxide (LOCOS) isolation was used. There was no evidence of a step present at the well boundary but the manufacturer states that a twin-well process is used.

- A standard 4T NMOS SRAM cell design was used. Metal lines were used to form the bit lines, and to distribute Gnd. Poly 2 was used to form “pull-up” resistors and distribute Vcc. Polycide 1 was used to form all gates. No problem areas were identified.

- Poly 2 fuses were present on the die. An oxide cutout was not present over fuses. No blown fuses were noted. As noted previously, the design may be intended to blow fuses by current instead of laser.
The devices were subjected to the following analysis procedures:

- External inspection
- X-Ray
- Decapsulation
- Internal optical inspection
- SEM of assembly features
- SEM of passivation
- Passivation integrity test
- Passivation removal
- Delayer to metal 1 and inspect
- Metal 1 removal and inspect barrier
- Delayer to silicon and inspect poly/die surface
- Die sectioning (90° for SEM)*
- Die material analysis
- Measure horizontal dimensions
- Measure vertical dimensions

*Delineation of cross-sections is by silicon etch unless otherwise indicated.*
**OVERALL QUALITY EVALUATION:** Overall Rating: Normal/Poor

**DETAIL OF EVALUATION**

<table>
<thead>
<tr>
<th>Category</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package integrity</td>
<td>N</td>
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<tr>
<td>Package markings</td>
<td>G</td>
</tr>
<tr>
<td>Die placement</td>
<td>N</td>
</tr>
<tr>
<td>Wirebond placement</td>
<td>G</td>
</tr>
<tr>
<td>Wire spacing</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond quality</td>
<td>N</td>
</tr>
<tr>
<td>Die attach quality</td>
<td>N</td>
</tr>
<tr>
<td>Dicing quality</td>
<td>N</td>
</tr>
<tr>
<td>Die attach method</td>
<td>Silver-epoxy</td>
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<tr>
<td>Dicing method</td>
<td>Sawn (90 percent)</td>
</tr>
<tr>
<td>Wirebond method</td>
<td>Thermosonic ball bonds using 1.1 mil O.D. gold wire</td>
</tr>
</tbody>
</table>

Die surface integrity:

<table>
<thead>
<tr>
<th>Category</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toolmarks (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Particles (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Contamination (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Process defects (absence)</td>
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<td>General workmanship</td>
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<td>Passivation integrity</td>
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</tr>
<tr>
<td>Metal definition</td>
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<tr>
<td>Metal integrity</td>
<td>P*</td>
</tr>
<tr>
<td>Metal registration</td>
<td>N</td>
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<tr>
<td>Contact coverage</td>
<td>N</td>
</tr>
<tr>
<td>Contact registration</td>
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</tr>
</tbody>
</table>

* *  Thinning and large silicon nodules.

* $G = Good$, $P = Poor$, $N = Normal$, $NP = Normal/Poor$
PACKAGE MARKINGS

TOP

(LOGO)
MS62256CLL-70PC
9543

BOTTOM

F50929NA
TWN

WIREBOND STRENGTH

Wire material: 1.1 mil diameter gold
Die pad material: Aluminum
Material at package lands: Silver

# of wires pulled: 15
Bond lifts: 0
Force to break - high: 12.0g
- low: 9.0g
- avg.: 10.3g
- std. dev.: 0.93

DIE MATERIAL ANALYSIS

Overlay passivation: A layer of nitride over a layer of glass.
Metallization: Silicon-doped aluminum (Al) with a titanium-nitride (TiN) barrier.
Polycide metal: Tungsten.
HORIZONTAL DIMENSIONS

Die size: 6.6 x 3.6 mm (260 x 143 mils)

Die area: 24.0 mm² (37,180 mils²)

Min pad size: 0.14 x 0.14 mm (5.5 x 5.5 mils)

Min pad window: 0.12 x 0.12 mm (4.7 x 4.7 mils)

Min pad space: 34.0 microns (1.3 mils)

Min metal width: 1.5 micron

Min metal space: 1.4 micron

Min metal pitch: 2.9 micron

Min contact size: 0.9 micron

Min poly 2 width (array): 0.6 micron

Min polycide 1 width: 0.7 micron

Min polycide 1 space: 1.0 micron

Min gate length* - (N-channel): 0.7 micron

- (P-channel): 0.7 micron

Min diffusion space: 1.0 micron

*Physical gate length
VERTICAL DIMENSIONS

Die thickness: 0.5 mm (19 mils)

Layers:

- Passivation 2: 0.5 micron
- Passivation 1: 0.2 micron
- Metal 1 - aluminum: 0.9 micron
  - barrier: 0.11 micron
- Pre-metal dielectric: 0.35 micron (average)
- Oxide on poly 2: 0.15 micron
- Poly 2: 0.1 micron (approximate)
- Interpoly oxide: 0.15 micron
- Polycide 1 - silicide: 0.13 micron
  - poly: 0.12 micron
- Local oxide: 0.4 micron
- N+ S/D: 0.2 micron
- P + S/D: 0.4 micron
- P-well: 4.5 microns (approximate)
## INDEX TO FIGURES

<table>
<thead>
<tr>
<th>Category</th>
<th>Figures</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASSEMBLY</td>
<td>1 - 5</td>
</tr>
<tr>
<td>DIE LAYOUT AND IDENTIFICATION</td>
<td>6 - 8</td>
</tr>
<tr>
<td>PHYSICAL DIE STRUCTURES</td>
<td>9 - 32</td>
</tr>
<tr>
<td>FUSES</td>
<td>22 - 24</td>
</tr>
<tr>
<td>COLOR DRAWING OF DIE STRUCTURE</td>
<td>25</td>
</tr>
<tr>
<td>SRAM MEMORY CELL STRUCTURES</td>
<td>26 - 31</td>
</tr>
<tr>
<td>CIRCUIT LAYOUT AND I/O</td>
<td>32</td>
</tr>
</tbody>
</table>
Figure 1. Package photographs and pinout of the Mosel Vitelic MS62256CLL-70PC. Mag. 2.7x.
Figure 2. X-ray views of the package. Mag. 3x.
Figure 3. SEM views of typical wirebonding. 60°.
Figure 4. SEM views of dicing and edge seal. 60°.
Figure 5. SEM section views of the edge seal.
Figure 6. Whole die photograph of the Mosel Vitelic MS62256CLL-70PC. Mag. 32x.
Figure 7. Optical views of die markings.
Figure 8. Optical views of die corners. Mag. 150x.
Figure 9. SEM section views illustrating general structure. Mag. 13,000x.
Figure 10. Perspective SEM views illustrating overlay passivation coverage. 60°.
Figure 11. SEM section views of metal line profiles.
Figure 12. Topological SEM views of metal patterning. 0°.
Figure 13. Perspective SEM views illustrating metal step coverage. 60°.
Figure 14. SEM section views illustrating typical metal contacts.
Figure 15. SEM section views illustrating a hillock and a metal contact.
Figure 16. SEM views illustrating silicon nodules.
Figure 17. Topological SEM views of polycide 1 patterning. Mag. 3200x, 0°.
Figure 18. Perspective SEM views illustrating polycide 1 coverage. 60°.
Figure 19. SEM section views of typical transistors. Mag. 52,000x.
Figure 20. SEM section views illustrating a birdsbeak and field oxide isolation. Mag. 52,000x.
Figure 21. Section views illustrating well structure.
passivation removed, Mag. 6500x, $0^\circ$

Mag. 800x

Figure 22. Topological views illustrating fuse structures.
Figure 23. SEM section views illustrating a fuse.
Figure 24. Additional SEM section views of a fuse.
Figure 25. Color cross-section drawing illustrating device structure.

Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate.
Figure 26. Perspective SEM views of the SRAM cell. Mag. 6500x, 60°.
Figure 27. Detailed SEM views of the SRAM cell at poly. Mag. 30,000x, 60°.
Figure 28. Topological SEM views of the SRAM cell array. Mag. 3200x, 0°.
Figure 29. Detailed topological SEM views and schematic of the SRAM cell. Mag. 6500x, 0°.
Figure 30. SEM section views of the SRAM cell array.
Figure 31. Additional SEM section views of the SRAM cell array.
Figure 32. Optical views of the input protection and typical device circuit layout.