Construction Analysis

NEC D481850GE-A10
8Mb SGRAM

Report Number: SCA 9703-531
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INTRODUCTION

This report describes a construction analysis of the NEC D41850GE-A10, 8 Meg SGRAM. One decapsulated was received for the analysis. No date code was visible but parts were undoubtedly made in 1996.

MAJOR FINDINGS

Questionable Items:¹ None.

Special Features:

• Sub-micron gate lengths (0.45 micron).

• Stacked capacitor DRAM cell design.

• Four layers of poly.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
TECHNOLOGY DESCRIPTION

Die Process and Design

- Fabrication process: Selective oxidation CMOS process employing twin wells in a P-substrate (no epi was used).

- Final passivation: A single thick layer of nitride.

- Metallization: Metal 2 and metal 1 consisted of silicon-doped aluminum defined by a dry-etch technique. Both metal layers employed a titanium-nitride cap and barrier. Standard vias and tungsten plug contacts were employed.

- Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of a layer of glass followed by a spin-on-glass (SOG) and another layer of glass.

- Pre-metal dielectric: A single layer of reflow glass over a densified oxide.

- Polysilicon: Four layers of polysilicon were employed. Poly 4 was used to form the common plate of the DRAM capacitors. Poly 3 was used to form the individual plates of the DRAM capacitors. Polycide 2 (poly 2 and tungsten silicide) was used to form interconnect and bit lines in the cell. Polycide 1 (poly 1 and tungsten silicide) was used to form all gates and word lines on the die.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Oxide sidewall spacers were used and were left in place.

- Wells: Twin wells in a P-substrate (no epi). A step in the local oxide was noted at the edge of N-wells.
TECHNOLOGY DESCRIPTION (continued)

- Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present.

- Memory cells: A stacked cell design using all four layers of poly as described above. Neither of the metal layers was used directly in the cells (i.e., used as “piggyback” word lines only). Cell size measured 3.1 microns$^2$. 
ANALYSIS RESULTS

Die Process and Design:  

Questionable Items:¹ None.

Special Features:

• Sub-micron gate lengths (0.45 micron).

• Stacked capacitor DRAM cell design.

• Four layers of poly.

General Items:

• Fabrication process: Selective oxidation CMOS process employing twin wells in a P-substrate (no epi was used). No significant problems were found in the process.

• Design implementation: Die layout was clean and efficient. Alignment was good at all levels.

• Surface defects: No toolmarks, masking defects, or contamination areas were found.

• Final passivation: A single thick layer of nitride.

• Metallization: Metal 2 and metal 1 consisted of silicon-doped aluminum defined by a dry-etch technique. Both metal layers employed a titanium-nitride cap and barrier. Standard vias and tungsten plug contacts were employed. No problems were noted.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
• Metal patterning: Both metal layers were defined by a dry-etch of good quality.

• Metal defects: None. No notching of voiding of the metal layers was found. No silicon nodules were found following removal of the aluminum.

• Metal step coverage: Metal 2 aluminum thinned up to 85 percent at vias. Typical metal 2 thinning was 80 percent. Military standards allow up to 70 percent metal thinning at contacts of this size. Virtually no metal 1 thinning was present due to the use of tungsten plugs at contacts.

• Vias and contacts: Via and contact cuts appeared to be defined by a two-step etch. No excessive over-etching or other problems were found.

• Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of a layer of glass followed by a spin-on glass (SOG) for planarization, and another layer of glass. No problems were found with these layers.

• Pre-metal dielectric: Three layers of reflow glass (BPSG) over a densified oxide in peripheral circuit areas and in the memory array (see Figure 13).

• Polysilicon: Four layers of polysilicon were employed. Poly 4 was in the form of a sheet and used to form the common plate of the DRAM capacitors. Poly 3 was used to form the individual plates of the DRAM capacitors. Polycide 2 (poly 2 and tungsten silicide) was used to form interconnect and bit lines in the cell. Polycide 1 (poly 1 and tungsten silicide) was used to form all gates and word lines on the die. Definition was good at all layers and no problems were noted.

• Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was present in the local oxide at the well boundaries.
ANALYSIS RESULTS (continued)

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Sidewall spacers were used and left in place. No problems were found in any of these areas.

- Wells: Twin wells were used in a P substrate (no epi was present). A step in the oxide was noted at the edge of the wells (indication of twin-well process) and no problems were found. The P-well could not be delineated.

- Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present.

- Memory cells: A stacked cell design using all four layers of poly as described above. Capacitors were formed over the bit line. Neither of the metal layers was used directly in the cells (i.e., used as “piggyback” word lines only). Cell pitch was 1.3 x 2.4 microns (3.12 microns²).
The devices were subjected to the following analysis procedures:

- Internal optical inspection and photography
- SEM inspection of passivation
- Delayer to metal 2 and inspect
- Aluminum removal (metal 2) and inspect
- Delayer to metal 1 and inspect
- Aluminum removal (metal 1) and inspect
- Delayer to poly 4, poly 3, poly 2 and inspect
- Delayer to poly 1/substrate and inspect poly and substrate
- Die sectioning (90° for SEM)*
- Measure horizontal dimensions
- Measure vertical dimensions
- Die material analysis

* *Delineation of cross-sections is by silicon etch unless otherwise indicated.*
OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Die surface integrity:
  Toolmarks (absence) G
  Particles (absence) G
  Contamination (absence) G
  Process defects (absence) G

General workmanship G
Passivation integrity G
Metal definition N
Metal integrity N
Metal registration G
Contact coverage G
Contact registration G

G = Good, P = Poor, N = Normal, NP = Normal/Poor
<table>
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<tr>
<td>Overlay passivation:</td>
</tr>
<tr>
<td>Nitride.</td>
</tr>
<tr>
<td>Metallization 2:</td>
</tr>
<tr>
<td>Aluminum with a titanium-nitride (TiN) cap and</td>
</tr>
<tr>
<td>barrier.</td>
</tr>
<tr>
<td>Intermetal dielectric (IMD):</td>
</tr>
<tr>
<td>Two layers of silicon-dioxide with a planarizing</td>
</tr>
<tr>
<td>glass (SOG) between.</td>
</tr>
<tr>
<td>Metallization 1:</td>
</tr>
<tr>
<td>Aluminum with a titanium-nitride (TiN) cap and</td>
</tr>
<tr>
<td>barrier.</td>
</tr>
<tr>
<td>Pre-metal glass:</td>
</tr>
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<td>Three layers of reflow glass over a densified oxide.</td>
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<td>Polycide:</td>
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## HORIZONTAL DIMENSIONS

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<tr>
<td>Die size:</td>
<td>6.8 x 9.9 mm (271 x 393 mils)</td>
</tr>
<tr>
<td>Die area:</td>
<td>69 mm² (106,503 mils²)</td>
</tr>
<tr>
<td>Min pad size:</td>
<td>0.11 x 0.11 mm (4.3 x 4.3 mils)</td>
</tr>
<tr>
<td>Min pad window:</td>
<td>0.09 x 0.09 mm (3.8 x 3.8 mils)</td>
</tr>
<tr>
<td>Min pad space:</td>
<td>0.05 mm (2.0 mils)</td>
</tr>
<tr>
<td>Min metal 2 width:</td>
<td>1.3 micron</td>
</tr>
<tr>
<td>Min metal 2 space:</td>
<td>1.5 micron</td>
</tr>
<tr>
<td>Min metal 2 pitch:</td>
<td>2.8 microns</td>
</tr>
<tr>
<td>Min via:</td>
<td>1.1 micron</td>
</tr>
<tr>
<td>Min via pitch:</td>
<td>2.0 microns</td>
</tr>
<tr>
<td>Min metal 1 width:</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>Min metal 1 space:</td>
<td>0.5 micron</td>
</tr>
<tr>
<td>Min metal 1 pitch:</td>
<td>1.1 micron</td>
</tr>
<tr>
<td>Min contact:</td>
<td>0.7 micron</td>
</tr>
<tr>
<td>Min contact pitch:</td>
<td>1.4 micron</td>
</tr>
<tr>
<td>Min poly 3 width:</td>
<td>0.8 micron</td>
</tr>
<tr>
<td>Min poly 3 space:</td>
<td>0.4 micron</td>
</tr>
<tr>
<td>Min polycide 2 width:</td>
<td>0.2 micron</td>
</tr>
<tr>
<td>Min polycide 2 space:</td>
<td>0.7 micron</td>
</tr>
<tr>
<td>Min polycide 1 width - (cell):</td>
<td>0.2 micron</td>
</tr>
<tr>
<td>Min polycide 1 space:</td>
<td>0.5 micron</td>
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<tr>
<td>Min gate length* - (N-channel):</td>
<td>0.6 micron</td>
</tr>
<tr>
<td></td>
<td>- (P-channel): 0.8 micron</td>
</tr>
<tr>
<td>Cell size:</td>
<td>3.12 microns²</td>
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<tr>
<td>Cell pitch:</td>
<td>1.3 x 2.4 microns</td>
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*Physical gate length.*
**VERTICAL DIMENSIONS**

Die thickness: 0.4 mm (15.5 mils)

**Layers**

Passivation: 0.8 micron
Metal 1 - cap: 0.05 micron (approximate)
  - aluminum: 0.9 micron
  - barrier: 0.1 micron
Intermetal dielectric - glass 3: 0.4 micron
  - glass 2 (SOG): 0 - 0.6 micron
  - glass 1: 0.5 micron
Metal 1 - cap: 0.05 micron (approximate)
  - aluminum: 0.4 micron
  - barrier: 0.1 micron
Reflow glass 3: 0.5 - 0.9 micron
Reflow glass 2: 0.3 - 0.5 micron
Reflow glass 1: 0.1 - 0.3 micron
Poly 4 (sheet): 1.3 micron
Poly 3: 0.35 micron
Polycide 2: 0.1 micron
Polycide 1: 0.2 micron
Local oxide: 0.25 micron
N+ S/D diffusion: 0.25 micron
P+ S/D diffusion: 0.3 micron (approximate)
N-well: 5 microns
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Mag. 13,000x

Mag. 26,000x
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glass etch
metal 1-to-poly 1

metal 1-to-poly 2

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