Construction Analysis

Winbond W2E512/W27E257
EEPROM

Report Number: SCA 9703-533
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INTRODUCTION

This report describes a competitive analysis of the WINBOND 512K and 256K EEPROM. Two devices of each type were received for the analysis. Since the processes used were almost identical, only minimal analysis of the 256K device is included, and in all cases identified as such. The devices were packaged in 28-pin Dual In-line Packages (DIPs). Possible date codes were 9647 for the 512K, and 9627 for the 256K devices.

MAJOR FINDINGS

Questionable Items:

1. Aluminum thinning up to 90 percent² (Figure 21). Barrier metal maintained continuity. With the addition of a cap and barrier metal, overall metal thinning was 85 percent.

Special Features:

• Unique (WINBOND) cell design.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

Assembly:

- Devices were encapsulated in plastic 28-pin Dual In-line Packages (DIPs).

- Lead-locking provisions (holes and anchors) at all pins.

- Thermosonic ball bond method employing 1.1 mil O.D. gold wire.

- All pins were connected. Double bonding wires were used on pin 14 (GND) and pin 28 (VCC) on both devices.

- Sawn dicing (full depth).

- Silver-filled epoxy die attach.

Die Process

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P-substrate (no epi was noted).

- Overlay passivation: A layer of silicon-nitride over a layer of silicon-dioxide.

- Metallization: Metal consisted of a single layer of aluminum doped with silicon. Titanium-nitride (TiN) cap and barrier metals were present. A thin layer of titanium (Ti) was present beneath the barrier. The construction of the metal on both devices was the same except that the 256K device did not appear to use a cap metal. The metallization was defined by a dry-etch technique.
TECHNOLOGY DESCRIPTION (continued)

- Pre-metal dielectric: A layer of borophosphosilicate glass (BPSG) over various densified oxides. This layer appeared to have been reflowed following contact cuts on the 256K device and before contact cuts on the 512K device.

- Polysilicon: Two layers of dry-etched polysilicon (no silicide). Poly 2 was used to form word lines in the array and all gates in the periphery. Poly 1 was used exclusively to form floating gates in the cell array.

- Isolation: Local oxide (LOCOS).

- Diffusions: Standard implanted N+ and P+ diffusions were used for source and drains. Oxide sidewall spacers were present on the gates indicating an LDD process may have been used.

- Wells: N-wells in a P substrate. No step was noted in the oxide at the well boundary. No epi was visible.

- Memory cells: The memory cell design consisted of poly 2 word lines and select gates, and poly 1 floating gates. Metal formed the bit lines. Programming is achieved by injecting electrons to and from the floating gate through Fowler-Nordheim tunneling. Cell pitch was 2.6 x 3 microns.
ANALYSIS RESULTS I

Assembly:  

Questionable Items:¹ None.

General Items:

• Devices were packaged in plastic 28-pin Dual In-line Packages (DIPs).

• Overall package quality: Normal. No defects were found on the external or internal portions of the packages.

• Lead-locking provisions (anchors and holes) were present.

• Wirebonding: Thermosonic ball bond method using 1.1 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were good (see page 10). Wire spacing and placement was normal. Double bonding wires were used for pins 14 and 28 on both devices. All pins were connected.

• Die attach: Silver-filled epoxy of normal quantity and quality.

• Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

Die Process and Design:  

Questionable Items:¹  

- Aluminum thinning up to 90 percent² (Figure 21). Barrier metal maintained continuity.  
  With the addition of a cap and barrier metal, overall metal thinning was 85 percent.

Special Features:  

- Unique (WINBOND) cell design, ultra-thin tunnel oxide used for programming.

General Items:  

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P-substrate (no epi).

- Design and layout: Die layout was clean and efficient. Alignment was good at all levels.

- Die surface defects: None. No contamination, toolmarks or processing defects were noted.

- Overlay passivation: A layer of silicon-nitride over a layer of silicon-dioxide.  
  Overlay integrity tests indicated defect-free passivation. Edge seal was good.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.
ANALYSIS RESULTS II (continued)

- Metallization: Metal consisted of a single layer of aluminum doped with silicon. A titanium-nitride (TiN) cap and barrier metal were used. A thin layer of titanium (Ti) was present beneath the barrier for adhesion purposes. The construction of the metal on both devices was the same except that the 256K device did not have a cap metal.

- Metal patterning: The metal was patterned by a dry etch of normal quality.

- Metal defects: None. No voiding or notching of the metal was found. Small silicon nodules were noted following removal of the metal, but no problems were present.

- Metal step coverage: Aluminum thinned up to 95 percent at contacts. Total metal thinning was reduced to 85 percent with the addition of the cap and barrier on the 512K device.

- Contacts: No significant over-etching of the contacts was present, and all contacts were completely surrounded with metal.

- Pre-metal dielectric: A layer of borophosphosilicate glass (BPSG) over various densified oxides. This layer was reflowed following contact cuts on the 256K device and before contact cuts on the 512K device. No problems were found.

- Polysilicon: Two layers of dry-etched polysilicon (no silicide). Poly 2 was used to form the word lines in the array and all gates in the periphery. Poly 1 which was very thin, was used exclusively to form floating gates in the cell array. Definition was by a dry etch of good quality.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere.
ANALYSIS RESULTS II (continued)

• Diffusions: Standard implanted N+ and P+ diffusions were used for source and drains. Oxide sidewall spacers were present on the gates indicating an LDD process may have been used.

• Wells: N-wells in a P substrate. No step was noted in the oxide at the well boundary. No epi was visible.

• Buried contacts: Direct poly-to-diffusion (buried) contacts were not used.

• Memory cells: The memory cell design consisted of poly 2 word lines and select gates, and poly 1 floating gates. Metal formed the bit lines. Programming is achieved by injecting electrons to and from the floating gate through Fowler-Nordheim tunneling. Cell pitch was 2.6 x 3 microns.

• I/O structure: Transistor gate lengths were longer at the I/O structure than in the periphery. Source/drain diffusion depths were the same as in the periphery.
PROCEDURE

The devices were subjected to the following analysis procedures:

- External inspection
- X-ray
- Decapsulation
- Internal optical inspection
- SEM inspection of assembly features and passivation
- Passivation integrity tests
- Wirepull tests
- Passivation removal
- SEM inspection of metal
- Metal removal and inspect for silicon nodules
- Delayer to poly and inspect poly structures and die surface
- Die sectioning (90° for SEM)*
- Measure horizontal dimensions
- Measure vertical dimensions
- Die material analysis

*Delineation of cross-sections is by silicon etch unless otherwise indicated.*
**OVERALL QUALITY EVALUATION:** Overall Rating: Normal

**DETAIL OF EVALUATION**

<table>
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<tr>
<th>Category</th>
<th>Rating</th>
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<tr>
<td>Package integrity</td>
<td>G</td>
</tr>
<tr>
<td>Package markings</td>
<td>G</td>
</tr>
<tr>
<td>Die placement</td>
<td>G</td>
</tr>
<tr>
<td>Die attach quality</td>
<td>G</td>
</tr>
<tr>
<td>Wire spacing</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond placement</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond quality</td>
<td>G</td>
</tr>
<tr>
<td>Dicing quality</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond method</td>
<td>Thermosonic ball bonds using 1.1 mil gold wire.</td>
</tr>
<tr>
<td>Die attach method</td>
<td>Silver-filled epoxy</td>
</tr>
<tr>
<td>Dicing method</td>
<td>Sawn (full depth)</td>
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Die surface integrity:
- Tool marks (absence) G
- Particles (absence) G
- Contamination (absence) G
- Process defects (absence) G

General workmanship: N
Passivation integrity: G
Metal definition: G
Metal integrity\(^1\): NP
Contact coverage: G
Contact registration: G
Contact defects: N

\(^1\)90 percent aluminum thinning on the 512K device.

G = Good, P = Poor, N = Normal, NP = Normal/Poor
PACKAGE MARKINGS 512K

Top

(LOGO) Winbond
W27E512-12
647QC263874601PA

Bottom

TAIWAN PA1
QC26387460

PACKAGE MARKINGS 256K

Top

(LOGO) Winbond
W27E257-12
627AJ16207400208B

Bottom

TAIWAN 0B2
AJ16207400

WIREBOND STRENGTH

Wire material: 1.1 mil diameter gold
Die pad material: aluminum
Material at package post: silver

Sample #

<table>
<thead>
<tr>
<th>512K</th>
<th>256K</th>
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<tbody>
<tr>
<td># of wires tested:</td>
<td>14</td>
</tr>
<tr>
<td>Bond lifts:</td>
<td>0</td>
</tr>
<tr>
<td>Force to break - high:</td>
<td>8.5g</td>
</tr>
<tr>
<td>- low:</td>
<td>6g</td>
</tr>
<tr>
<td>- avg.:</td>
<td>7.2g</td>
</tr>
<tr>
<td>- std. dev.:</td>
<td>1.9</td>
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DIE MATERIAL ANALYSIS

Passivation: Silicon-nitride over silicon-dioxide.

Metallization: Silicon-doped aluminum with a titanium-nitride cap and barrier.*

*There is no known method for accurately determining the amount of silicon in the aluminum on a finished die.
HORIZONTAL DIMENSIONS 256K

Die size: 3.4 x 4.3 mm (132 x 169 mils)
Die area: 14.6 mm² (22,308 mils²)
Min pad size: 0.14 x 0.16 mm (5.4 x 6.6 mils)
Min pad window: 0.09 x 0.11 mm (3.4 x 4.5 mils)
Min pad space: 0.15 mm (5.9 mils)
Min contact: 1.3 micron
Min gate length - (N-channel): 1.1 micron

512K

Die size: 3.6 x 3.6 mm (140 x 140 mils)
Die area: 13 mm² (19,600 mils²)
Min pad size: 0.1 x 0.11 mm (4.0 x 4.2 mils)
Min pad window: 0.09 x 0.09 mm (4.0 x 4.0 mils)
Min pad space: 0.13 mm (5.3 mils)
Min metal width: 1.5 micron
Min metal space: 1.1 micron
Min metal pitch: 2.6 microns
Min contact: 0.95 micron
Min contact pitch: 1.9 micron
Min poly 2 width: 0.9 micron
Min poly 2 space: 1.5 micron
Min poly 1 width: 0.7 micron
Min poly 1 space: 1.0 micron
Min poly 1 pitch: 1.7 micron
Min gate length - (N-channel): 0.9 micron
- (P-channel): 1.0 micron
EEPROM cell size: 7.8 microns²
EEPROM cell pitch: 2.6 x 3 microns
VERTICAL DIMENSIONS

Die thickness: 0.6 mm (26 mils)

Layers

Passivation 2: 0.45 micron
Passivation 1: 0.3 micron
Metallization - cap 0.07 micron (approximate)
  - aluminum 1.0 micron
  - barrier 0.15 micron
Pre-metal glass: 0.65 micron
Poly 2: 0.3 micron
Poly 1: 0.06 micron (approximate)
Local oxide: 0.6 micron
N+ diffusion: 0.2 micron
P+ diffusion: 0.4 micron
N-well: 6 microns
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Mag. 2.6x.
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Mag. 2.6x
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Mag. 1600x

Mag. 6500x
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Mag. 13,000x

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- metal-to-P+, silicon etch
- metal-to-N+, silicon etch
- metal-to-poly 2, glass etch
metal-to-N+

metal-to-poly 2

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