Construction Analysis

Lattice 3256A-90LM PLD

Report Number: SCA 9705-538
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INTRODUCTION

This report describes a construction analysis of the Lattice 3256A-90LM Programmable Logic Device (PLD). One decapped device was received for the analysis. The device was date coded 9650.

MAJOR FINDINGS

Questionable Items:\(^1\)

- Aluminum 1 thinning up to 100 percent\(^2\) (Figure 15). Total metal 1 thinning was reduced to 90 percent with the addition of the cap and barrier.

Special Features:

- Sub-micron gate lengths (0.5 micron N-channel and 0.6 micron P-channel).

Design Features:

- Slotted and beveled metal 2 bus lines.

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

\(^2\)Seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

Die Process and Design:

- The device was fabricated using a selective oxidation, twin-well CMOS process in a P-substrate. No epi was used.

- Passivation consisted of a layer of nitride over a layer of silicon-dioxide.

- Metallization employed two levels of metal. Both consisted of aluminum with a titanium-nitride (TiN) cap and barrier. A thin titanium (Ti) adhesion layer was used under metal 1. Standard vias and contacts were used (no plugs).

- The interlevel dielectric consisted of two layers of glass with a spin-on-glass (SOG) between the two layers.

- Pre-metal glass consisted of a layer of reflow glass over various densified oxides. Glass was reflowed prior to contact cuts only.

- A single layer of polycide (tungsten silicide) was used to form one plate of the capacitors and all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Local oxide (LOCOS) isolation. A step was present at the edge of the well which indicates a twin-well process was used. No problems were noted.

- Two EEPROM cell arrays were used on the device. Both devices are programmed through an ultra thin (tunnel) oxide window. Metal 2 was used to form the bit lines and distribute ground on array B. Metal 1 was used for interconnect and to distribute ground on array A. Poly was used to form the gates and one plate of the capacitors and gates.
ANALYSIS RESULTS I

Die Process:  

Figure 1 - 36

Questionable Items:  

- Aluminum 1 thinning up to 100 percent (Figure 15). Total metal 1 thinning was reduced to 90 percent with the addition of the cap and barrier.

Special Features:

- Sub-micron gate lengths (0.5 micron N-channel and 0.6 micron P-channel).

Design features:

- Slotted and beveled metal 2 bus lines.

General items:

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P-substrate. No epi was used.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage of contamination was found.

- Die coat: No die coat was present.

- Overlay passivation: A layer of nitride over a layer of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good.

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1These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

2Seriousness depends on design margins.
ANALYSIS RESULTS I (continued)

- Metallization: Two levels of metal. Both consisted of aluminum with titanium-nitride (TiN) caps and barriers. A thin titanium (Ti) adhesion layer was present beneath metal 1. Standard vias and contacts were used (no plugs).

- Metal patterning: Both metal levels were patterned by a dry etch of normal quality.

- Metal defects: No voiding, notching, or neckdown was noted in the metal of either layer. Contacts and vias were completely surrounded by metal. No silicon nodules were noted following removal of either metal layer.

- Metal step coverage: Metal 2 aluminum thinned up to 75 percent at vias. Total metal 2 thinning was reduced to 65 percent with the addition of the cap and barrier. Metal 1 aluminum thinned up to 100 percent at some contacts. Total metal 1 thinning was reduced to 90 percent with the addition of the cap and barrier.

- Interlevel dielectric: Two layers of silicon-dioxide were present under metal 2 (interlevel dielectric). The first layer had been subjected to an etchback process. A layer of spin-on-glass (SOG) was present between the layers for planarization purposes.

- Pre-metal glass: A layer of reflow glass over various densified oxides was used under metal 1. Reflow was performed prior to contact cuts only. No problems were found.

- Contact defects: Contact and via cuts were defined by a two-step process. No over-etching of the contacts or vias was noted.

- A single layer of polycide (tungsten silicide) was used to form all gates on the die and one plate of the capacitors. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry-etch of normal quality.
ANALYSIS RESULTS I (continued)

• Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No problems were found.

• Local oxide (LOCOS) isolation was used with a step present at the well boundary indicating that a twin-well process was employed.

• Two EEPROM cell arrays were used on the device. Both use the same design (but different layout) and are programmed through an ultra thin (tunnel) oxide window. Metal 2 was used to form the bit lines and distribute ground on array B. Metal 1 was used for interconnect and to distribute ground in array A. Poly was used to form the gates and one plate of the capacitors. Cell size (array A): 9.0 x 9.5 microns. Cell size (array B): 13 x 36 microns

• Redundancy fuses were not present on the die.
PROCEDURE

The devices were subjected to the following analysis procedures:

- Internal optical inspection
- SEM of passivation
- Passivation integrity test
- Passivation removal
- SEM inspection of metal 2
- Metal 2 removal and inspect barrier
- Delayer to metal 1 and inspect
- Metal 1 removal and inspect barrier
- Delayer to silicon and inspect poly/die surface
- Die sectioning (90° for SEM)*
- Die material analysis
- Measure horizontal dimensions
- Measure vertical dimensions

*Delineation of cross-sections is by silicon etch unless otherwise indicated.
OVERALL QUALITY EVALUATION:  Overall Rating:  Normal

DETAIL OF EVALUATION

Die surface integrity:

  Toolmarks (absence)    G
  Particles (absence)    G
  Contamination (absence) G
  Process defects        G

General workmanship   N
Passivation integrity G
Metal definition       N
Metal integrity*       N
Metal registration     N
Contact coverage       N
Contact registration   N

*Even with the isolated spots where metal 1 thins 100 percent we judge adequate metal remains around the contact perimeter.

G = Good, P = Poor, N = Normal, NP = Normal/Poor


**DIE MATERIAL ANALYSIS**

Final passivation: A layer of silicon-nitride over a layer of glass.

Metallization 2: Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.

Metallization 1: Aluminum (Al) with a titanium-nitride (TiN) cap and barrier on a thin titanium (Ti) adhesion layer.

Silicide (poly): Tungsten (W).
# Horizontal Dimensions

<table>
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<tr>
<th>Dimension</th>
<th>Value</th>
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<tr>
<td>Die size:</td>
<td>7.4 x 9.2 mm (290 x 364 mils)</td>
</tr>
<tr>
<td>Die area:</td>
<td>68 mm² (105,560 mils²)</td>
</tr>
<tr>
<td>Min pad size:</td>
<td>0.1 x 0.1 mm (4.0 x 4.0 mils)</td>
</tr>
<tr>
<td>Min pad window:</td>
<td>0.09 x 0.09 mm (3.8 x 3.8 mils)</td>
</tr>
<tr>
<td>Min pad space:</td>
<td>28 microns</td>
</tr>
<tr>
<td>Min metal 2 width:</td>
<td>1.1 micron</td>
</tr>
<tr>
<td>Min metal 2 space:</td>
<td>1.1 micron</td>
</tr>
<tr>
<td>Min metal 2 pitch:</td>
<td>2.2 microns</td>
</tr>
<tr>
<td>Min metal 1 width:</td>
<td>0.8 micron</td>
</tr>
<tr>
<td>Min metal 1 space:</td>
<td>0.8 micron</td>
</tr>
<tr>
<td>Min metal 1 pitch:</td>
<td>1.6 micron</td>
</tr>
<tr>
<td>Min via:</td>
<td>0.85 micron</td>
</tr>
<tr>
<td>Min contact:</td>
<td>0.8 micron</td>
</tr>
<tr>
<td>Min polycide width:</td>
<td>0.5 micron</td>
</tr>
<tr>
<td>Min polycide space:</td>
<td>0.7 micron</td>
</tr>
<tr>
<td>Min gate length* - (N-channel):</td>
<td>0.5 micron</td>
</tr>
<tr>
<td>- (P-channel):</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>Cell pitch (array A):</td>
<td>9.0 x 9.5 microns</td>
</tr>
<tr>
<td>Cell size (array A):</td>
<td>85.5 microns²</td>
</tr>
<tr>
<td>Cell pitch (array B):</td>
<td>13 x 35 microns</td>
</tr>
<tr>
<td>Cell size (array B):</td>
<td>455 microns²</td>
</tr>
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*Physical gate length
VERTICAL DIMENSIONS

Die thickness: 0.5 mm (20 mils)

Layers:

Passivation 2: 0.45 micron
Passivation 1: 0.25 micron
Metal 2 - cap: 0.05 micron (approximate)
  - aluminum: 0.8 micron
  - barrier: 0.12 micron
Interlevel dielectric- glass 2: 0.4 micron
  - glass 1: 0.3 micron (average)
Metal 1 - cap: 0.07 micron (approximate)
  - aluminum: 0.5 micron
  - barrier: 0.12 micron
Pre-metal dielectric: 0.75 micron (average)
Oxide on polycide: 0.15 micron
Polycide - silicide: 0.1 micron
  - poly: 0.12 micron
Local oxide: 0.45 micron
N+ S/D: 0.13 micron
P+ S/D: 0.2 micron
N-well: 4.0 microns
P-well: 4.0 microns
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Figure 9. Topological SEM views of metal 2 patterning.
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Figure 1. SEM section views of metal 1 line profiles.

Mag. 40,000x

Mag. 52,000x
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Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate

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Array B.
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