Construction Analysis

Atmel AT89C2051 & AT89S8252 Microcontrollers

Report Number: SCA 9706-543
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INTRODUCTION

This report describes a construction analysis of the Atmel AT89C2051 and the AT89S8252 8-Bit Microcontrollers. Ten AT89C2051 devices encapsulated in 20-pin Dual-In-line Packages (DIPs) and two AT89S8252 devices in 40-pin Dual-In-line Packages were used for the analysis. The AT89C2051 devices were date coded 9642 and the AT89S8252 had a date code of 9709.

MAJOR FINDINGS

Questionable Items: 1

• Metal 1 aluminum thinning up to 90 percent 2 at some contact edges on the AT89C2051 (Figure 13).

Special Features: None.

Noteworthy Items:

• Both devices are of similar structure; however, there are distinct differences. The Flash cell design is the same on both devices; however, the cell of the AT89S8252 is smaller. The AT89S8252 also has an EEPROM memory. Cell design is identical and the only distinction between the Flash and the EEPROM memory appears to be the method in which the cells are erased. The other significant difference is that the AT89S8252 employs a second metal layer which is used sparsely, mainly to connect circuit blocks.

1 These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

2 Seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

Assembly (AT89C2051 device only unless indicated):

- 20-pin plastic Dual-In-line Package (DIP).
- 40-pin plastic Dual-In-line Package (DIP) AT89S8252.
- External leads plated with tin-lead (SnPb) and internally spot-plated with silver (Ag).
- A silver-epoxy die attach was employed on both die.
- Die coat was not employed on either die.
- Lead-locking provisions (holes) were present at all pins.
- Multiple wirebonds were used at Vcc and GND pins to provide extra current-carrying capacity. A bonding wire was connected from ground to the paddle for biasing purposes.
- Thermosonic wirebonding using 1.2 mil O.D. gold wire.
- Dicing was by sawing (full depth) on both die.

Die Process and Design

- Note: Process description is same on both devices except where noted.
- Fabrication process: CMOS process employing twin-wells, on a P-substrate.
- Final passivation: Two thick layers of silicon-dioxide.
TECHNOLOGY DESCRIPTION (continued)

- Metallization: Single level metallization was used on the AT89C2051 device. No cap was used; however a titanium-nitride barrier was employed. The metal was defined by a standard dry etch. Two levels of metallization were used on the AT89S8252 device. Metal 2 employed a titanium-nitride barrier and metal 1 employed a titanium-nitride cap and barrier. Metal 2 was sparsely used and appeared to mainly connect circuit blocks together.

- Interlevel dielectric (AT89S8252 device only): The dielectric consisted of two layers of glass. The first layer appeared to have been subjected to an etchback.

- Pre-metal: A single layer of reflow glass over grown oxides. The glass appeared to have been reflowed following the contact cuts.

- Polysilicon: Two layers of standard poly silicon were employed. Poly 2 was used to form all gates on the die and word lines and program lines in the EEPROM arrays. Poly 1 was used exclusively in the EEPROM arrays where it formed the floating gates.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. No sidewall spacers were present on the gates and no evidence of LDD structures was found.

- Isolation: LOCOS, a step was noted in the local oxide at the well boundary indicating a twin-well process was employed.

- Wells: Twin-wells in an P substrate.

- Fuses: No fuses were employed on this device.

- Buried contacts: No buried contacts were used.
TECHNOLOGY DESCRIPTION (continued)

- SRAM: The memory cell consisted of a 6T SRAM design. Metal 1 formed the bit lines and distributed Vcc and GND. Poly 2 formed the word lines, storage gates and pull-up devices.

- EEPROM: The memory cell design consisted of a poly 2 word line and program line and a poly 1 floating gate. Metal one formed the bit lines. Programming is achieved through ultra-thin tunnel oxide windows. Interpoly dielectric consisted of an ONO dielectric. Both of the devices AT89S8252 and AT89C2051 have the same layout design for both EEPROM (AT89S8252 only) and Flash memory. However, the cell size of the AT89S8252 was about half the size of the cell on the AT89C2051. On the AT89S8252 both EEPROM and Flash had the same design on the AT89S8252 device, but the way the cells are erased distinguishes the two types.

- MROM: An MROM cell array was employed on both devices. The cell was programmed by the metal 1 layer. No detailed analysis of this memory was performed since structures are the same as the peripheral circuits.
ANALYSIS RESULTS I

Assembly:  
Figures 1 - 4

Questionable Items: 1 None.

Special Features: None.

General Items:

• Overall package quality: Good. No significant defects were found on the external or internal portions of the packages on both die. No voids or cracks were noted in the plastic package on both die.

• Wirebonding: Thermosonic ball bond method using 1.2 mil gold wire. Bonds were well formed and placement was good. All bond pull strengths were normal and no bond lifts occurred (see page 11).

• Die attach: Silver-epoxy of normal quality. No problems were found.

• Die dicing: Die separation was by sawing (full depth) and showed normal quality workmanship. No large chips or cracks were present at the die surface.

1These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

Die Process and Design:  

**Figures 5 - 31**

Questionable Items:

- Metal 1 aluminum thinning up to 90 percent\(^2\) at some contact edges on the AT89C2051 (Figure 13).

Special Features:  None.

Noteworthy Items:

- Both devices are of similar structure; however, there are distinct differences. The Flash cell design is the same on both devices; however, the cell of the AT89S8252 is smaller. The AT89S8252 also has an EEPROM memory. Cell design is identical and the only distinction between the Flash and the EEPROM memory appears to be the method in which the cells are erased. The other significant difference is that the AT89S8252 employs a second metal which is used sparsely, mainly to connect circuit blocks.

General Items:

- Fabrication process: CMOS process employing twin-wells in a P substrate. All P-channel devices were formed in N-wells. All N-channel devices were formed in P-wells. No epi was employed on these devices.

- Design implementation: Die layout was clean. Alignment was good at all levels.

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

\(^2\)Seriousness depends on design margins.
ANALYSIS RESULTS II (continued)

• Surface defects: No contamination, processing defects or tool marks were found.

• Final passivation: Two thick layers of silicon-dioxide.

• Metallization: A single level metallization was used on the AT89C2051 device. No cap was used; however a titanium-nitride barrier was employed. Two levels of metallization were used on the AT89S8252 device. Metal 2 employed a titanium-nitride barrier and metal 1 employed a titanium-nitride cap and barrier. Metal 2 was used mainly to connect circuit blocks together.

• Metal patterning: The metal layers were defined by standard dry etch. Metal completely surrounded all contacts. Standard contacts were employed (no plugs).

• Metal defects: No notching or voiding was found. No silicon nodules were observed following removal of the aluminum layers.

• Metal step coverage: Metal 1 aluminum thinning was up to 90 percent thinning (Figure 13) at some contacts. The amount of thinning is excessive a manufacturer’s design specifications should be verified (AT89C2051 only).

• Contacts: Contacts were overetched slightly into the substrate and polysilicon; however, no problems are foreseen.

• Interlevel dielectric (AT89S8252 device only): The dielectric consisted of two layers of glass. The first layer appeared to have been subjected to an etchback. No problems were noted.

• Pre-metal: A single layer of reflow glass over grown oxides. The glass was reflowed following the contact cuts. No problems were found.
ANALYSIS RESULTS II (continued)

• Polysilicon: Two layers of standard polysilicon were employed. Poly 2 was used to form all gates on the die and word lines and program lines in the EEPROM array. Poly 1 was used exclusively in the EEPROM array where it formed the floating gates.

• Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was present in the local oxide at the well boundaries.

• Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. No sidewall spacers were used and no evidence of LDD structures were found.

• Wells: Twin-wells in an P substrate.

• Fuses: No fuses were employed on this device.

• Buried contacts: No buried contacts were used.

• SRAM: The memory cell consisted of a 6T SRAM design. Metal 1 formed the bit lines and distributed Vcc and GND. Poly 2 formed the word lines, storage gates and pull-up devices.

• EEPROM: The memory cell design consisted of a poly 2 word line and program line and a poly 1 floating gate. Metal one formed the bit lines. Programming is achieved through ultra-thin tunnel oxide windows. Interpoly dielectric consisted of an ONO dielectric. Both of the devices AT89S8252 and AT89C2051 have the same layout design for both EEPROM (AT89S8252 only) and Flash memory. However, the cell size of the AT89S8252 was about half the size of the cell on the AT89C2051. On the AT89S8252 both EEPROM and Flash had the same design. The way the cells are erased distinguishes the two types.

• MROM: An MROM cell array was employed on both devices. The cell was programmed through metal 1 layer. No detailed analysis of this memory was performed since structures are the same as peripheral circuits.
The devices were subjected to the following analysis procedures:

- External inspection
- Decapsulation
- Optical inspection
- Wirepull test
- SEM of passivation and assembly features
- Passivation removal and inspect metal
- Aluminum removal
- Delayer to poly and inspect
- Die sectioning (90° for SEM)*
- Measure horizontal dimensions
- Measure vertical dimensions
- Die material analysis

*Delineation of cross-sections is by silicon etch unless otherwise indicated.*
OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity  G
Package markings  G
Die placement  G
Wirebond placement  G
Wire spacing  G
Wirebond quality  G
Die attach quality  N
Dicing quality  N
Dicing method  Sawn (full depth)
Wirebond method  Thermosonic ball bonds using 1.2 mil gold wire.

Die surface integrity:
  Toolmarks (absence)  G
  Particles (absence)  G
  Contamination (absence)  G
  Process defects (absence)  G
General workmanship  G
Passivation integrity  G
Metal definition  G
Metal integrity  NP*
Metal registration  G
Contact coverage  G
Contact registration  G

*Metal 1 aluminum thinning up to 90 percent.

G = Good, P = Poor, N = Normal, NP = Normal/Poor
PACKAGE MARKINGS

AT89C2051

<table>
<thead>
<tr>
<th>TOP</th>
<th>BOTTOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Logo)</td>
<td>6C203-1</td>
</tr>
<tr>
<td>AT89C2051</td>
<td>9056F</td>
</tr>
<tr>
<td>9642</td>
<td>1-F 6C9642</td>
</tr>
<tr>
<td>12PC</td>
<td></td>
</tr>
</tbody>
</table>

AT89S8252

<table>
<thead>
<tr>
<th>TOP</th>
<th>BOTTOM</th>
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<tbody>
<tr>
<td>(Logo)</td>
<td>6D0412-2</td>
</tr>
<tr>
<td>AT89S8252</td>
<td>19552H</td>
</tr>
<tr>
<td>24PC</td>
<td>1 KOREA</td>
</tr>
<tr>
<td>9709</td>
<td>6D9706</td>
</tr>
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WIREBOND STRENGTH (AT89C2051)

Wire material: 1.2 mil diameter gold
Die pad material: aluminum

Sample # 1

# of wires pulled: 15
Bond lifts: 0
Force to break - high: 19.0g
- low: 14.0g
- avg.: 16.1g
- std. dev.: 1.7
## DIE MATERIALS

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<thead>
<tr>
<th>Material</th>
<th>Description</th>
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<tr>
<td>Passivation:</td>
<td>Two layers of silicon-dioxide.</td>
</tr>
<tr>
<td>Metal 2 (AT89S8252 device only):</td>
<td>Aluminum with a titanium-nitride barrier.</td>
</tr>
<tr>
<td>Metal 1:</td>
<td>Aluminum with a titanium-nitride barrier. Metal 1 also employed a titanium-nitride cap on the AT89S8252 device.</td>
</tr>
<tr>
<td>Interlevel dielectric (AT89S8252 device only):</td>
<td>Two layers of silicon-dioxide.</td>
</tr>
<tr>
<td>Pre-metal dielectric:</td>
<td>BPSG glass.</td>
</tr>
</tbody>
</table>
HORIZONTAL DIMENSIONS

Note: All dimensions taken from the AT89C2051 device, except where noted.

Die size: 4.7 x 3.8mm (187.5 x 152 mils)
6.1 x 5.2mm (240 x 206 mils) AT89S8252

Die area: 18mm² (28,500 mils²)
31.7mm² (49,440 mils²) AT89S8252

Min pad size: 0.1 x 0.11mm (4 x 4.5 mils)
Min pad window: 0.11 x 0.13mm (4.5 x 5 mils)
Min pad space: 6.7 mils
Min pad-to-metal: 12.5 microns

Min metal width: 2 microns
Min metal space: 1.5 micron
Min metal pitch: 3.6 microns
Min contact: 1.1 micron
Min poly width: 1.2 micron

Min gate length* - (N-channel): 1.2 micron
- (P-channel): 1.5 micron

Cell size (SRAM on AT89C2051): 474 microns²
Cell pitch (SRAM on AT89C2051): 22.3 x 21.3 microns

Cell size (EEPROM - AT89C2051): 32.5 microns²
Cell pitch (EEPROM - AT89C2051): 8.5 x 3.5 microns

Cell size (EEPROM - AT89S8252): 16.4 microns²
Cell pitch (EEPROM - AT89S8252): 6.3 x 2.6 microns

*Physical gate length.
VERTICAL DIMENSIONS

Note: All dimensions taken from the AT89C2051 device, except where noted.

Die thickness: 0.3 mm (11.5 mils)

Layers

Passivation 2: 0.8 micron
Passivation 1: 0.6 micron
Metal 2 (AT89S8252) - aluminum: 1.0 micron
- barrier: 0.06 micron (approx.)
Metal 1 (AT89C2051) - aluminum: 0.7 micron
- barrier: 0.06 micron (approx.)
Interlevel dielectric (AT89S8252): 1.3 micron (average)
Pre-metal dielectric: 0.55 micron (average)
Oxide on poly 2: 0.15 micron
Poly 1: 0.25 micron
Poly 2: 0.4 micron
Local oxide: 0.8 micron
N+ S/D diffusion: 0.4 micron
P+ S/D diffusion: 0.3 micron
N-well: 5 microns (approx.)
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