Construction Analysis

NKK NR4645LQF-133
64-Bit RISC Microprocessor

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INTRODUCTION

This report describes a construction analysis of the NKK NR4645LQF-133 64-bit RISC Microprocessor (133MHz). One device packaged in a 128-pin Plastic Quad Flat Package (PQFP) was received for the analysis. The device was date coded 9640.

MAJOR FINDINGS

Questionable Items:

1. Metal 3 aluminum thinning up to 100 percent\(^2\) at metal 3-to-metal 2 vias (Figure 12). Barrier maintained continuity.

2. Metal 2 aluminum thinning up to 95 percent\(^2\) at metal 2-to-metal 1 vias (Figure 15).

Special Features:

1. Three level metal, twin-well, epi, CMOS process.

2. Sub-micron gate lengths (0.35 micron).

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended applications.

\(^2\)Seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

Assembly:

- The device was packaged in 128-pin Plastic Quad Flat Package (PQFP) for surface mount applications.

- Die separation was by sawing (full depth). Silver-filled epoxy was used to attach the die to the paddle.

- Wirebonding was by the thermosonic ball bond method using 1.0 mil O.D. gold wire.

- Pins 4, 77 and 80 were not connected. No multiple bonding was noted.

Die Process

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an apparent N-epi on a P substrate.

- No die coat was present.

- Final passivation: A layer of nitride over a layer of silicon-dioxide.

- Metallization: Three levels of metal defined by dry-etch techniques. Metal layers 3 and 2 consisted of aluminum with a titanium-nitride (TiN) cap and a titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride (TiN) cap and barrier. Standard vias were used at metal 3 and metal 2. Metal 1 used tungsten (W) plugs for contacts. A thin titanium (Ti) layer was used under metal 1 for adhesion purposes.

- Interlevel dielectrics: Both interlevel dielectrics (between metal 3 and metal 2 and between metal 2 and metal 1) consisted of two layers of silicon-dioxide. No
spin-on-glass (SOG) was noted. The first layer of glass appeared to have been subjected to an etchback.

- Pre-metal dielectric: This dielectric consisted of a CVD glass (probably BPSG) over various densified oxides. Reflow was performed prior to contact cuts.

- Polysilicon: A single layer of dry-etched poly (no silicide) was used. This layer was used to form all gates on the die and word lines in the SRAM arrays.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing. Diffusions were not silicided.

- Isolation: Local oxide (LOCOS). A step was present in the oxide at the well boundaries indicating a twin well process was employed.

- Wells: Twin wells in what appeared to be an N-epi on a P substrate.

- Memory cells: Two SRAM cell arrays were present. The 6T SRAM cell design used metal 3 to distribute GND and form “piggyback” word lines (via metals 1 and 2), and metal 2 to form the bit lines. Metal 1 distributed GND and Vcc and provided cell interconnect. Poly was used to form the word lines and all gates. The 12T SRAM cell design used metal 3 to distribute input signals, word lines and GND. Metal 2 was used to form the output and bit lines and distribute Vcc and GND. Metal 1 was used to provide cell interconnect. Poly formed the word lines and all gates.
ANALYSIS RESULTS I

Package and Assembly:  

Figures 1 - 4

Questionable Items:¹ None.

General Items:

• The device was packaged in a 128-pin Plastic Quad Flat Package (PQFP) for surface mount applications.

• Overall package quality: Good. No defects were noted on the external portion of the package. Pins were well formed (except previously damaged pins).

• Die dicing: Die separation was by sawing (full depth) of normal quality. No large chips or cracks were present.

• Die attach: A silver-filled epoxy was used to attach the die to the paddle. Some voids were apparent on the x-ray; however, overall coverage was approximately 75 percent and no problems are foreseen.

• Wirebonding: Wirebonding was by the thermosonic ball bond method using 1.0 mil O.D. gold wire. Wirebond formation and placement were normal.

• Pins 4, 77 and 80 were not connected. No multiple bonding was noted.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended applications.
ANALYSIS RESULTS II

Die Process and Design:  

Questionable Items:\(^1\)

- Metal 3 aluminum thinning up to 100 percent\(^2\) at some metal 3-to-metal 2 via locations (Figure 12).

- Metal 2 aluminum thinning up to 95 percent\(^2\) at some metal 2-to-metal 1 via locations (Figure 15).

Special Features:

- Three level metal, twin-well, epi, CMOS process.

- Sub-micron gate lengths (0.35 micron).

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an apparent N-epi on a P substrate.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels.

- Die coat: No die coat was present.

- Die surface defects: None. No contamination, toolmarks or processing defects were noted.

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended applications.

\(^2\)Seriousness depends on design margins.
ANALYSIS RESULTS II (continued)

- Final passivation: Passivation consisted of a layer of nitride over a layer of silicon dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was also good.

- Metallization: Three levels of metal defined by dry-etch techniques. Metal layers 3 and 2 consisted of aluminum with a titanium-nitride (TiN) cap and a titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride (TiN) cap and barrier. Standard vias were used under metal 3 and metal 2. Metal 1 used tungsten (W) plugs for contacts. A thin titanium (Ti) layer was used under metal 1 for adhesion purposes. Tungsten (W) plugs used titanium-nitride (TiN) liners.

- Metal patterning: All metal layers were defined by a standard dry etch of normal quality. Metal lines were widened around vias and contacts at all metal levels.

- Metal defects: None. No voiding, notching or cracking of any metal layers was found. No silicon nodules were found following removal of the aluminum.

- Metal step coverage: Metal 3 aluminum thinned up to 100 percent at some via edge locations (barrier maintained continuity). Total metal 3 thinning was reduced to 95 percent with the addition of the cap and barrier metal. Metal 2 aluminum thinned up to 95 percent at some via edge locations. Total metal 2 thinning was reduced to 85 percent with the addition of the cap and barrier. MIL-STD-883D allows up to 70 percent metal thinning for contacts of this size. Virtually no metal 1 thinning was present due to the use of tungsten plugs. All contacts and vias were completely surrounded by metallization.

- Interlevel dielectrics: Both interlevel dielectrics (between metal 3 and metal 2 and between metal 2 and metal 1) consisted of two layers of silicon-dioxide each. No spin-on-glass (SOG) was used to aid planarization. The first layer of glass appeared to have been subjected to an etchback. Voids were noted in the first layer of glass on both levels. They appear to be a result of the first layer of glass cusping between
minimum spaced lines (see Figures 13 and 16). No serious reliability concerns are foreseen due to this since the metals were completely surrounded by glass.

- Pre-metal dielectric: A CVD glass (probably BPSG) over various densified oxides was used under metal 1. Reflow was performed prior to contact cuts. No problems were found.

- Poly: A single level of poly (no silicide). Poly formed all gates on the die and word lines in the SRAM arrays. Definition was by a dry etch of good quality. Oxide sidewall spacers were used throughout and left in place. No problems were found.

- Isolation: Local oxide (LOCOS) isolation was used. No problems were found.

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Diffusions were not silicided. An LDD process was used employing oxide sidewall spacers on the gates.

- Wells: Twin-wells were used in an apparent N-epi on a P substrate. A step was noted at the well boundary confirming a twin-well process was employed.

- Memory cells: Two SRAM cell arrays were present. The 6T SRAM cell design used metal 3 to distribute GND and form “piggyback” word lines (via metals 1 and 2), and metal 2 to form the bit lines. Metal 1 was used to distribute GND and Vcc and to provide cell interconnect. Poly was used to form word lines and all gates. Cell pitch was 3.7 x 19.0 microns (70 microns², a very large cell). The 12T SRAM cell design used metal 3 to distribute input signals, word lines and GND. Metal 2 was used to form the output and bit lines and distribute Vcc and GND. Metal 1 was used to provide cell interconnect. Poly was used to form the word lines and all gates. Cell pitch was 10 x 19.5 microns (195 microns²).

- No redundancy elements (fuses) were present.
PROCEDURE

The device was subjected to the following analysis procedures:

- External inspection
- X-ray
- Decapsulation
- Internal optical inspection
- SEM of assembly and passivation
- Passivation integrity test (chemical)
- Passivation removal
- SEM inspection of metal 3
- Aluminum 3 removal
- Delayer to metal 2 and inspect
- Aluminum 2 removal
- Delayer to metal 1 and inspect
- Aluminum 1 removal
- Delayer to silicon and inspect poly/die surface
- Die sectioning (90° for SEM)*
- Die material analysis
- Measure horizontal dimensions
- Measure vertical dimensions

*Delineation of cross-sections is by silicon etch unless otherwise indicated.
**OVERALL QUALITY EVALUATION:** Overall Rating: Normal.

**DETAIL OF EVALUATION**

<table>
<thead>
<tr>
<th>Category</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package integrity</td>
<td>N</td>
</tr>
<tr>
<td>Package markings</td>
<td>N</td>
</tr>
<tr>
<td>Die placement</td>
<td>N</td>
</tr>
<tr>
<td>Wirebond placement</td>
<td>N</td>
</tr>
<tr>
<td>Wire spacing</td>
<td>N</td>
</tr>
<tr>
<td>Wirebond quality</td>
<td>N</td>
</tr>
<tr>
<td>Die attach quality</td>
<td>N</td>
</tr>
<tr>
<td>Dicing quality</td>
<td>N</td>
</tr>
<tr>
<td>Die attach method</td>
<td>Silver-epoxy</td>
</tr>
<tr>
<td>Dicing method</td>
<td>Sawn (full depth)</td>
</tr>
<tr>
<td>Wirebond method</td>
<td>Thermosonic ball bonds using 1.0 mil gold wire.</td>
</tr>
</tbody>
</table>

Die surface integrity:
- Toolmarks (absence) G
- Particles (absence) G
- Contamination (absence) G
- Process defects (absence) N

<table>
<thead>
<tr>
<th>Category</th>
<th>Rating</th>
</tr>
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<tbody>
<tr>
<td>General workmanship</td>
<td>N</td>
</tr>
<tr>
<td>Passivation integrity</td>
<td>G</td>
</tr>
<tr>
<td>Metal definition</td>
<td>N</td>
</tr>
<tr>
<td>Metal integrity</td>
<td>NP1</td>
</tr>
<tr>
<td>Metal registration</td>
<td>N</td>
</tr>
<tr>
<td>Contact coverage</td>
<td>N</td>
</tr>
<tr>
<td>Contact registration</td>
<td>N</td>
</tr>
</tbody>
</table>

1Metal 3 aluminum thinning up to 100 percent, metal 2 aluminum thinning up to 95 percent.

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*
### PACKAGE MARKINGS

**TOP**

(LOGO) NKK JAPAN  
NR4645LQF-133  
6135840B 9640

**BOTTOM**

AB 89 (molded)

### DIE MATERIAL IDENTIFICATION

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Material Information</th>
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<tr>
<td>Overlay passivation:</td>
<td>Nitride over silicon-dioxide.</td>
</tr>
<tr>
<td>Metallization 3:</td>
<td>Aluminum (Al) with a titanium-nitride cap and titanium (Ti) barrier.</td>
</tr>
<tr>
<td>Interlevel dielectric 2 (M3-to-M2):</td>
<td>Two layers of silicon-dioxide.</td>
</tr>
<tr>
<td>Metallization 2:</td>
<td>Aluminum (Al) with a titanium-nitride cap and a titanium (Ti) barrier.</td>
</tr>
<tr>
<td>Interlevel dielectric 1 (M2-to-M1):</td>
<td>Two layers of silicon-dioxide.</td>
</tr>
<tr>
<td>Metallization 1:</td>
<td>Aluminum (Al) with a titanium-nitride (TiN) cap and barrier. A thin titanium (Ti) adhesion layer was present under the barrier.</td>
</tr>
<tr>
<td>Plugs (metal 1):</td>
<td>Tungsten on a titanium-nitride (TiN) liner.</td>
</tr>
<tr>
<td>Pre-metal dielectric:</td>
<td>CVD glass (probably BPSG) over various densified oxides.</td>
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### HORIZONTAL DIMENSIONS

<table>
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<tr>
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<th>Value</th>
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<tr>
<td>Die size</td>
<td>7.2 x 7.6 mm (285 x 300 mils)</td>
</tr>
<tr>
<td>Die area</td>
<td>55 mm² (85,500 mils²)</td>
</tr>
<tr>
<td>Min pad size</td>
<td>0.1 x 0.1 mm (4.2 x 4.2 mils)</td>
</tr>
<tr>
<td>Min pad window</td>
<td>0.09 x 0.09 mm (3.9 x 3.9 mils)</td>
</tr>
<tr>
<td>Min pad space</td>
<td>20 microns (0.8 mil)</td>
</tr>
<tr>
<td>Min metal 3 width</td>
<td>0.85 micron</td>
</tr>
<tr>
<td>Min metal 3 space</td>
<td>0.8 micron</td>
</tr>
<tr>
<td>Min metal 3 pitch</td>
<td>1.65 micron</td>
</tr>
<tr>
<td>Min metal 2 width</td>
<td>0.65 micron</td>
</tr>
<tr>
<td>Min metal 2 space</td>
<td>0.7 micron</td>
</tr>
<tr>
<td>Min metal 2 pitch</td>
<td>1.35 micron</td>
</tr>
<tr>
<td>Min metal 1 width</td>
<td>0.55 micron</td>
</tr>
<tr>
<td>Min metal 1 space</td>
<td>0.5 micron</td>
</tr>
<tr>
<td>Min metal 1 pitch</td>
<td>1.05 micron</td>
</tr>
<tr>
<td>Min via (M3-to-M2)</td>
<td>0.8 micron (round)</td>
</tr>
<tr>
<td>Min via (M2-to-M1)</td>
<td>0.85 micron (round)</td>
</tr>
<tr>
<td>Min contact</td>
<td>0.55 micron (round)</td>
</tr>
<tr>
<td>Min poly width</td>
<td>0.35 micron</td>
</tr>
<tr>
<td>Min poly space</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>Min gate length*</td>
<td>0.35 micron</td>
</tr>
<tr>
<td></td>
<td>- (N-channel):</td>
</tr>
<tr>
<td></td>
<td>- (P-channel):</td>
</tr>
<tr>
<td>6T SRAM cell size</td>
<td>70 microns²</td>
</tr>
<tr>
<td>6T SRAM cell pitch</td>
<td>3.7 x 19.0 microns</td>
</tr>
<tr>
<td>12T SRAM cell size</td>
<td>195 microns²</td>
</tr>
<tr>
<td>12T SRAM cell pitch</td>
<td>10.0 x 19.5 microns</td>
</tr>
</tbody>
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*Physical gate length.*
VERTICAL DIMENSIONS

Layers

Passivation 2: 0.6 micron
Passivation 1: 0.65 micron
Metal 3 - cap: 0.05 micron (approx.)
  - aluminum: 1.0 micron
  - barrier: 0.1 micron
Interlevel dielectric 2 - glass 2: 0.35 - 0.4 micron
  - glass 1: 0.45 - 1.3 micron
Metal 2 - cap: 0.04 micron (approx.)
  - aluminum: 0.6 micron
  - barrier: 0.1 micron
Interlevel dielectric 1 - glass 2: 0.4 - 0.5 micron
  - glass 1: 0.4 - 0.9 micron
Metal 1- cap: 0.04 micron (approx.)
  - aluminum: 0.4 micron
  - barrier: 0.06 micron (approx.)
  - plugs: 0.6 - 0.9 micron
Pre metal dielectric: 0.5 - 0.8 micron
Oxide on poly: 0.15 micron
Poly: 0.25 micron
Local oxide: 0.35 micron
N+ S/D diffusion: 0.2 micron
P+ S/D diffusion: 0.2 micron
P well: 4 microns
N-epi: 10 microns
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metal 1-to-N+

metal 1-to P+

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