Motorola
MPA1016FN FPGA

Report Number: SCA 9711-561
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INTRODUCTION

This report describes a construction analysis of the Motorola MPA1016FN FPGA. Two devices packaged in 84-pin Plastic Leaded Chip Carriers (PLCCs) and five scribed dice were received for the analysis. These devices were fabricated by Chartered Semiconductor Manufacturing. The packaged devices were date coded 9640.

MAJOR FINDINGS

Questionable Items:¹ None.

Special Features:

• Three levels of reflowed (“hot”) aluminum.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
TECHNOLOGY DESCRIPTION

Assembly:

- The devices were encapsulated in 84-pin Plastic Leaded Chip Carriers (PLCCs).
- The copper (Cu) leadframe was internally spot-plated with silver (Ag).
- External pins were tinned with tin-lead (SnPb) solder.
- Lead-locking provisions (anchors) at all pins.
- Thermosonic ball bonding using 1.2 mil O.D. gold wire.
- Sawn dicing (full-depth).
- Silver-filled epoxy die attach.

Die Process:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-substrate.
- Final passivation: A layer of nitride over a layer of glass.
- Metallization: Three levels of metal defined by standard dry-etch techniques. Metal 3 and metal 2 consisted of aluminum with a titanium-nitride (TiN) cap and titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride cap and a titanium-nitride/titanium barrier. All three levels of aluminum were reflowed to fill contacts/vias (“hot aluminum”). Standard vias and contacts were used (no plugs).
TECHNOLOGY DESCRIPTION (continued)

- Interlevel dielectrics: Interlevel dielectrics consisted of two layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between them. The SOG had been etched back.

- Polysilicon: A single layer of polycide (poly cap over titanium silicide on poly) was used to form all gates on the die. Definition was by a dry etch of normal quality. Direct poly-to-diffusion (buried) contacts were not used.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Wells: Twin-wells in a P-substrate. A step was present at well boundaries.

- Redundancy: Fuses were not used.

- Memory cells: Programming is achieved through a modified 6T CMOS SRAM cell. Metal 3 was used to form the bit lines (via metal 2 and metal 1). Metal 2 was used to distribute Vcc and GND (via metal 1). Metal 1 was used to provide cell interconnect. Polycide was used to form all gates and word lines.
ANALYSIS RESULTS I

Assembly: Figures 1 - 3

Questionable Items: None.

General Items:

• The devices were encapsulated in 84-pin Plastic Leaded Chip Carriers (PLCCs).

• Overall package quality: Good. Internal spot-plating of the copper leadframe was silver. External pins were tinned with tin-lead (SnPb). No cracks or voids present. No gaps were noted at lead exits.

• Lead-locking provisions (anchors) were present at all pins.

• Wirebonding: Thermosonic ballbond method using 1.2 mil O.D. gold wire. No bond lifts occurred during wirepull tests and bond pull strengths were good.

• Die attach: Silver-filled epoxy of normal quality. No voids were noted in the die attach and no problems are foreseen.

• Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.
ANALYSIS RESULTS II

Die Process and Design:  

Questionable Items:¹ None.

Special Features:

• Three levels of reflowed (“hot”) aluminum.

General items:

• Fabrication process: Devices were fabricated using selective oxidation CMOS process employing twin-wells in a P-substrate.

• Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.

• Die coat: No die coat was present.

• Final passivation: A layer of nitride over a layer of glass. Integrity tests indicated defect-free passivation. Edge seal was good as the passivation extended beyond the metal at the edge of the die.

• Metallization: Three levels of metal defined by standard dry-etch techniques. Metal 3 and metal 2 consisted of aluminum with a titanium-nitride (TiN) cap and titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride cap and a titanium-nitride/titanium barrier. All three levels of aluminum were reflowed to provide excellent step coverage. Standard vias and contacts were used (no plugs).

• Metal patterning: All metal levels were patterned by a dry etch of normal quality.

• Metal defects: No voiding, notching, or neckdown was noted in any of the metal layers. No silicon nodules were noted following removal of the metal layers.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II (continued)

• Metal step coverage: All three levels of aluminum were reflowed to provide excellent step coverage. No metal thinning occurred at any vias or contacts.

• Interlevel dielectrics: Interlevel dielectrics consisted of two layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between them. The SOG had been etched back.

• Pre-metal dielectric: A layer of reflow glass (BPSG) over densified oxide was used under metal 1. Reflow was performed prior to contact cuts only.

• Contact defects: Contact and via cuts were defined by a two-step process. No over-etching of contacts was noted, but significant overetch was present at vias. This is not a problem in this case since the overetched aluminum is filled by the aluminum that fills the via. No problems were found.

• Polysilicon: A single layer of polycide (poly cap over titanium silicide on poly) was used to form all gates on the die. Definition was by a dry-etch of normal quality. Direct poly-to-diffusion (buried) contacts were not used.

• Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No problems were found.

• Isolation: LOCOS (local oxide isolation). A step was present at the well boundaries, confirming the presence of twin-wells.

• Redundancy: Fuses were not present on the die.

• Memory cells: Programming is achieved through a modified 6T CMOS SRAM cell. Metal 3 was used to form the bit lines (via metal 2 and metal 1). Metal 2 was used to distribute Vcc and GND (via metal 1). Metal 1 was used to provide cell interconnect. Polycide was used to form all gates and word lines.
PROCEDURE

The devices were subjected to the following analysis procedures:

- External inspection
- X-ray
- Decapsulate
- Internal optical inspection
- SEM of assembly features and passivation
- Wirepull test
- Passivation integrity test
- Passivation removal
- SEM inspection of metal 3
- Delayer to metal 2 and inspect
- Delayer to metal 1 and inspect
- Metal 1 removal and inspect barrier
- Delayer to silicon and inspect poly/die surface
- Die sectioning (90° for SEM)*
- Die material analysis
- Measure horizontal dimensions
- Measure vertical dimensions

*Delineation of cross-sections is by silicon etch unless otherwise indicated.
**OVERALL QUALITY EVALUATION:** Overall Rating: Good

**DETAIL OF EVALUATION**

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package integrity</td>
<td>G</td>
</tr>
<tr>
<td>Package markings</td>
<td>N</td>
</tr>
<tr>
<td>Die placement</td>
<td>N</td>
</tr>
<tr>
<td>Die attach quality</td>
<td>G</td>
</tr>
<tr>
<td>Wire spacing</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond placement</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond quality</td>
<td>N</td>
</tr>
<tr>
<td>Dicing quality</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond method</td>
<td>Thermosonic ball bond method using 1.2 mil O.D. gold wire.</td>
</tr>
<tr>
<td>Die attach method</td>
<td>Silver-epoxy</td>
</tr>
<tr>
<td>Dicing method</td>
<td>Sawn (full depth)</td>
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**Die surface integrity:**

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tool marks (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Particles (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Contamination (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Process defects</td>
<td>G</td>
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<tr>
<td>General workmanship</td>
<td>N</td>
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<tr>
<td>Passivation integrity</td>
<td>G</td>
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<tr>
<td>Metal definition</td>
<td>N</td>
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<tr>
<td>Metal integrity</td>
<td>G</td>
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<tr>
<td>Metal registration</td>
<td>G</td>
</tr>
<tr>
<td>Contact coverage</td>
<td>G</td>
</tr>
<tr>
<td>Contact registration</td>
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</tr>
</tbody>
</table>

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*
PACKAGE MARKINGS

TOP

(LOGO)
MPA1016FN
ZQUAL9640

WIREBOND STRENGTH

Wire material: 1.2 mil O.D. gold
Die pad material: aluminum
Material at package lands: silver

Sample # 1

# of wires tested: 20
Bond lifts: 0
Force to break - high: 15.0g
  - low: 11.0g
  - avg.: 13.0g
  - std. dev.: 0.3

DIE MATERIAL ANALYSIS

Final passivation: A layer of silicon-nitride over a layer of glass.
Metallization 3: Aluminum (Al) with a titanium-nitride (TiN) cap and titanium (Ti) barrier.
Metallization 2: Aluminum (Al) with a titanium-nitride (TiN) cap and titanium (Ti) barrier.
Metallization 1: Aluminum (Al) with a titanium-nitride (TiN) cap and titanium-nitride/titanium barrier.
Polycide: Polysilicon cap over Titanium (Ti) silicide on poly.
HORIZONTAL DIMENSIONS

Die size: 6.1 x 6.2 mm (241 x 245 mils)
Die area: 38 mm² (59,045 mils²)
Min pad size: 0.1 x 0.1 mm (3.9 x 4.0 mils)
Min pad window: 0.09 x 0.09 mm (3.5 x 3.6 mils)
Min pad space: 0.04 mm (1.4 mils)
Min metal 3 width: 1.0 micron
Min metal 3 space: 1.2 micron
Min metal 3 pitch: 2.2 microns
Min metal 2 width: 0.9 micron
Min metal 2 space: 1.2 micron
Min metal 2 pitch: 2.1 microns
Min metal 1 width: 0.6 micron
Min metal 1 space: 0.8 micron
Min metal 1 pitch: 1.5 micron
Min via (M3-to-M2): 0.6 micron (round)
Min via (M2-to-M1): 0.6 micron (round)
Min contact: 0.8 micron (round)
Min polycide width: 0.5 micron
Min polycide space: 1.0 micron
Min gate length* - (N-channel): 0.5 micron
- (P-channel): 0.5 micron

*Physical gate length.
## VERTICAL DIMENSIONS

**Die thickness:** 0.5 mm (19 mils)

**Layers**

<table>
<thead>
<tr>
<th>Layer Details</th>
<th>Thickness (microns)</th>
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<tbody>
<tr>
<td>Passivation 2</td>
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<tr>
<td>Passivation 1</td>
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<td>Metal 3 - cap</td>
<td>0.05 (approx.)</td>
</tr>
<tr>
<td>- aluminum</td>
<td>0.8</td>
</tr>
<tr>
<td>- barrier</td>
<td>0.12</td>
</tr>
<tr>
<td>Intermetal dielectric 2 - glass 2</td>
<td>0.4 (average)</td>
</tr>
<tr>
<td>- SOG</td>
<td>0 - 0.8</td>
</tr>
<tr>
<td>- glass 1</td>
<td>0.4 (average)</td>
</tr>
<tr>
<td>Metal 2 - cap</td>
<td>0.05 (approx.)</td>
</tr>
<tr>
<td>- aluminum</td>
<td>0.5</td>
</tr>
<tr>
<td>- barrier</td>
<td>0.1</td>
</tr>
<tr>
<td>Intermetal dielectric 1 - glass 2</td>
<td>0.4 (average)</td>
</tr>
<tr>
<td>- SOG</td>
<td>0 - 0.8</td>
</tr>
<tr>
<td>- glass 1</td>
<td>0.4 (average)</td>
</tr>
<tr>
<td>Metal 1 - cap</td>
<td>0.05 (approx.)</td>
</tr>
<tr>
<td>- aluminum</td>
<td>0.5</td>
</tr>
<tr>
<td>- TiN/ Ti barrier</td>
<td>0.17</td>
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<tr>
<td>Pre-metal glass</td>
<td>0.4 (avg.)</td>
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<tr>
<td>Poly - poly cap</td>
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<td>- silicide</td>
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<td>- poly</td>
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<tr>
<td>Local oxide</td>
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<tr>
<td>N+ S/D diffusion</td>
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<tr>
<td>P+ S/D diffusion</td>
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</tr>
<tr>
<td>N-well</td>
<td>2.5 (approx.)</td>
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Mag. 26,000x

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Mag. 26,000x

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