Construction Analysis

Motorola MC68360EM25VC
Communication Controller

Report Number: SCA 9711-562
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INTRODUCTION

This report describes a construction analysis of the Motorola MC68360EM25VC Communication Controller. Four samples were supplied for the analysis. The devices were received in 240-pin PQFPs (Plastic Quad Flat Packs) date coded 9710.

MAJOR FINDINGS

Questionable Items:\textsuperscript{1}

• Metal 2 thinned up to 80 percent\textsuperscript{2} at vias (Figure 22).

Special Features: None.

\textsuperscript{1}These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

\textsuperscript{2}Seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

Assembly

- The devices were packaged in 240-pin Plastic Quad Flat Packs (PQFP) with gull-wing leads.

- The leadframe was constructed of copper and externally tinned with lead-tin solder.

- The die was mounted cavity down on a dimpled header. The edges (and a portion on top) of the header and the internal leadframe were plated with silver.

- Die attach was by silver-epoxy.

- Thermosonic ball bonds using 1.2 mil gold wire. Four pins were not connected.

- Sawn dicing (full depth).

Die Process:

- Fabrication process: Selective oxide isolation, CMOS process employing twin wells in P substrate.

- Die coat: No die coat was used.

- Final passivation: A layer of silicon-nitride over a layer of glass.

- Metallization: Three levels of metal defined by dry-etch techniques. All metals consisted of aluminum with titanium-nitride caps. Metal 1 also employed a titanium-nitride barrier. Standard vias and contacts were employed (no plugs).

- Interlevel dielectrics: Interlevel dielectrics 1 and 2 used the same dielectric structure. A thick glass was deposited first, followed by another layer of glass. The first layer of deposited glass was subjected to an etchback. No spin on glass or CMP planarization was used.
TECHNOLOGY DESCRIPTION (continued)

• Pre-metal glass: A thick layer of BPSG over densified oxides. This glass was reflowed prior to contact cuts.

• Polysilicon: A single layer of dry-etched poly. This layer was used to form all gates on the die. Nitride sidewall spacers were used to provide the LDD spacing. No buried contacts were employed.

• Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. No silicide was used on the diffusions.

• Isolation: Local oxide isolation. A step was noted in the oxide at well boundaries.

• Wells: Twin-wells in a P substrate. The step in the oxide at the well boundaries indicates a twin-well process was employed.

• Memory cells: Two types of MROMs were present on the device (see Figures 34-37). Metal 1 formed the bit lines and poly formed the word lines. Both were programmed at the LOCOS level; however, Array B also appeared to be programmed at the contact cut level. A 6T SRAM array was employed as well as a 8T SRAM array (see Figures 38-40). Metal 2 formed the bit lines and distributed GND throughout the 6T cells. Metal 1 distributed Vcc and provided cell interconnect. Poly formed the word lines. Documentation of the metal layout on the 8T cell was not available for SEM photography.

• No redundancy fuses were found.
ANALYSIS RESULTS

Assembly:  

Questionable Items:\(^1\) None.

Special Features:  None.

General Items:

- Overall package quality: The devices were packaged in 240-pin Plastic Quad Flat Packs (PQFP) with gull-wing leads. No defects were noted on the external or internal portions of the package.

- Leadframe: The leadframe was constructed of copper. The gull-wing leads were well formed and the external tin-lead solder tinning was complete. No gaps were noted at lead exits. The die was mounted cavity down on a dimpled leader. The internal leadframe and the edges (and a portion of the top) of the header were plated with silver.

- Wirebonding: Thermosonic ball bond method using 1.2 mil gold wire. Bonds were well formed and placement was good. Bond pad pitch was relatively tight (136 microns); however, wire spacing was good and no problems were seen. Intermetallic formation was adequate at ball bonds. Wire pull strengths were normal; however, one bond lift was noted on each sample. Both bond lifts had part of the pad metal still adhered to the bond which indicates good adhesion (intermetallic) between the bond and the pad, so no problems are foreseen.

- Die attach: The die was mounted to the underside of the header with silver-epoxy die attach. Some excessive epoxy was noted at the edges of the attach; however, overall quality was normal with no voids noted.

- Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die edges.

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

Die Process and Design:  

Figures 10 - 40

Questionable Items:¹

• Metal 2 thinned up to 80 percent² at vias (Figure 22).

Special Features:  None.

General Items:

• Fabrication process:  Selective oxide isolation, CMOS process employing twin-wells in P substrate.  No problems were found in the process.

• Design implementation:  Die layout was clean and efficient.  Alignment was good at all levels.

• Surface defects:  No toolmarks, masking defects, or contamination areas were found.

• Final passivation:  A layer of nitride over a layer of glass.  Coverage was good and no defects were noted.  Edge seal was also good as the passivation extended to the scribe lane to seal the metallization.  A cutout was present at the die edge to prevent cracks from radiating inward over the active circuitry.

• Metallization:  Three levels of metal interconnect.  All metals consisted of aluminum with titanium-nitride caps.  Metal 1 also employed a titanium-nitride barrier.  Standard vias and contacts were used (no plugs).

¹These items present possible quality or reliability concerns.  They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.
• Metal patterning: All metal levels were defined by a dry etch of good quality. Metal lines were widened at via and contact connections (all levels).

• Metal defects: None. No voiding, notching or cracking of the metal layers. No silicon nodules were found following removal of the metal layers.

• Metal step coverage: Metal 3 (including cap) thinned up to 75 percent at vias and metal 2 (including cap) thinned up to 80 percent at vias. Although the thinning exceeds MIL-STDs (70 percent) it is probably not considered a serious reliability concern. Metal 1 (including cap and barrier) thinning was 65 percent at contacts.

• Vias and contacts: All via and contact cuts were defined by a two step etch. The cap metal was cleared at via sites for adhesion purposes and no significant over etching of the contacts was noted. Vias and contacts were completely surrounded by metal.

• Metal patterning: All metal levels were defined by a dry etch of good quality. Metal lines were widened at via and contact connections (all levels).

• Interlevel dielectrics: Interlevel dielectrics 1 and 2 consisted of the same type of oxide structure. A very thick glass was deposited first, followed by another layer of glass. The first layer was subjected to an etchback. No SOG or CMP planarization was used. No problems were found with any of these layers.

• Pre-metal glass: A thick layer of BPSG over densified oxides. The BPSG was reflowed prior to contact cuts. No problems were found.

• Polysilicon: A single layer of dry etched poly was used. It formed all gates and word lines in the arrays. Definition was by dry etch of good quality. It appears that the poly was deposited in two layers which is evident by the small oxide remnants when the poly was etched out in cross section (see Figures 29 and 30). Nitride sidewall spacers were used throughout and left in place. No problems were found.

• Isolation: The device used local oxide isolation. No problems were present at the birdsbeaks or elsewhere.
ANALYSIS RESULTS II (continued)

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Diffusions were not silicided (salicide process). As mentioned, an LDD process was used employing nitride sidewall spacers.

- Wells: Twin-wells were used in a P substrate. Definition was normal. We could not delineate the P-well in section; however, the step in the oxide indicates a twin-well process was employed.

- Buried contacts: Direct poly to diffusion contacts were not used.

- Memory cells: Two types of MROM arrays were present on the device (see Figures 34-37). Metal 1 formed the bit lines and poly formed the word lines. Both were programmed at the LOCOS level; however, Array B also appeared to be programmed at the contact cut level. A 6T SRAM array was employed as well as a 8T SRAM array (see Figures 38-40). Metal 2 formed the bit lines and distributed GND throughout the 6T cells. Metal 1 distributed Vcc and provided cell interconnect. Poly formed the word lines. Documentation of the metal layout on the 8T cell was not available for SEM photography.

- No redundancy fuses were noted.

Special Items:

- ESD sensitivity test: One sample was subjected to an ESD test which revealed all pins tested pass ± 4000V pulses.
PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection
X-ray
ESD test
Package section and EDX
Die optical inspection
SEM assembly features and passivation
Passivation integrity test
Wirepull test
Delayer to metal 3 and inspect
Delayer to metal 2 and inspect
Delayer to metal 1 and inspect
Delayer to poly substrate and inspect
Die sectioning (90° for SEM)
Measure horizontal dimensions
Measure vertical dimensions
Die material analysis
OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

<table>
<thead>
<tr>
<th>Package integrity</th>
<th>G</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package markings</td>
<td>G</td>
</tr>
<tr>
<td>Die placement</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond placement</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond spacing</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond quality</td>
<td>N</td>
</tr>
<tr>
<td>Dicing quality</td>
<td>N</td>
</tr>
<tr>
<td>Die attach quality</td>
<td>N</td>
</tr>
<tr>
<td>Die attach method</td>
<td>Silver epoxy</td>
</tr>
<tr>
<td>Dicing method</td>
<td>Sawn</td>
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<tr>
<td>Wirebond method</td>
<td>Thermosonic ball bonds using 1.2 mil gold wire.</td>
</tr>
<tr>
<td>Die surface integrity:</td>
<td></td>
</tr>
<tr>
<td>Toolmarks (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Particles (absence)</td>
<td>G</td>
</tr>
<tr>
<td>Contamination (absence)</td>
<td>G</td>
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<td>Process defects (absence)</td>
<td>G</td>
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<tr>
<td>General workmanship</td>
<td>G</td>
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<tr>
<td>Passivation integrity</td>
<td>G</td>
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<tr>
<td>Metal definition</td>
<td>G</td>
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<tr>
<td>Metal integrity</td>
<td>NP*</td>
</tr>
<tr>
<td>Metal registration</td>
<td>G</td>
</tr>
<tr>
<td>Contact coverage</td>
<td>G</td>
</tr>
<tr>
<td>Via/contact registration</td>
<td>N</td>
</tr>
</tbody>
</table>

G = Good, P = Poor, N = Normal, NP = Normal/Poor

*Metal 2 thinning up to 80 percent.
PACKAGE MARKINGS

TOP

(Logo)
MC68360EM25VC
2E68C 1EAD9710 Korea

BOTTOM

Molded markings

WIREBOND STRENGTH

Wire material: 1.2 mil diameter
Die pad material: Aluminum
Material at package land: Silver

<table>
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<tr>
<th>Sample #</th>
<th>1</th>
<th>2</th>
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<tr>
<td># of wires tested:</td>
<td>55</td>
<td>30</td>
</tr>
<tr>
<td>Bond lifts:</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Force to break</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- high:</td>
<td>13.5 g</td>
<td>13 g</td>
</tr>
<tr>
<td>- low:</td>
<td>9 g</td>
<td>10 g</td>
</tr>
<tr>
<td>- average:</td>
<td>11.2 g</td>
<td>10.9 g</td>
</tr>
<tr>
<td>- std. dev.:</td>
<td>1.3</td>
<td>0.9</td>
</tr>
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</table>
**DIE MATERIAL ANALYSIS**

Final passivation: Single layer of silicon-nitride* over a glass layer.

Metals 2 and 3: Aluminum with a titanium-nitride cap.

Interlevel dielectrics 1 and 2: A thick layer of glass followed by another layer of glass.

Metal 1: Aluminum with a titanium-nitride cap and barrier.

Pre-metal glass:* A CVD glass containing 7.6 wt. percent phosphorus and 3.2 wt. percent boron.

*WDX analysis

**PACKAGE MATERIALS**

Leadframe: Copper (Cu)

External tinning: Tin-lead (SnPb) solder

Internal plating: Silver (Ag)

Die attach: Silver (Ag) epoxy
### HORIZONTAL DIMENSIONS

<table>
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<tr>
<td>Die size</td>
<td>9.2 x 9.2 mm (362 x 364 mils)</td>
</tr>
<tr>
<td>Die area</td>
<td>85 mm² (131,768 mils²)</td>
</tr>
<tr>
<td>Min pad size</td>
<td>0.12 x 0.12 mm (4.7 x 4.9 mils)</td>
</tr>
<tr>
<td>Min pad window</td>
<td>0.11 x 0.11 mm (4.3 x 4.3 mils)</td>
</tr>
<tr>
<td>Min pad space</td>
<td>0.7 mils (17 microns)</td>
</tr>
<tr>
<td>Min metal 3 width</td>
<td>1.2 micron</td>
</tr>
<tr>
<td>Min metal 3 space</td>
<td>1.2 micron</td>
</tr>
<tr>
<td>Min metal 2 width</td>
<td>1.2 micron</td>
</tr>
<tr>
<td>Min metal 2 space</td>
<td>1.0 micron</td>
</tr>
<tr>
<td>Min metal 1 width</td>
<td>0.9 micron</td>
</tr>
<tr>
<td>Min metal 1 space</td>
<td>0.65 micron</td>
</tr>
<tr>
<td>Min via (M3-to-M2)</td>
<td>1.4 micron</td>
</tr>
<tr>
<td>Min via (M2-to-M1)</td>
<td>1.3 micron</td>
</tr>
<tr>
<td>Min contact</td>
<td>1.0 micron</td>
</tr>
<tr>
<td>Min poly width</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>Min poly space</td>
<td>0.85 micron</td>
</tr>
<tr>
<td>Min gate length* - (N-channel):</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>- (P-channel):</td>
<td>0.7 micron</td>
</tr>
<tr>
<td>6T SRAM cell size</td>
<td>117 microns²</td>
</tr>
<tr>
<td>6T SRAM cell pitch</td>
<td>9 x 13 microns</td>
</tr>
<tr>
<td>8T SRAM cell size</td>
<td>242 microns²</td>
</tr>
<tr>
<td>8T SRAM cell pitch</td>
<td>11 x 22 microns</td>
</tr>
<tr>
<td>MROM cell size (Array A):</td>
<td>7.3 microns²</td>
</tr>
<tr>
<td>MROM cell pitch (Array A):</td>
<td>2.6 x 2.8 microns</td>
</tr>
<tr>
<td>MROM cell size (Array B):</td>
<td>7.3 microns²</td>
</tr>
<tr>
<td>MROM cell pitch (Array B):</td>
<td>2.6 x 2.8 microns</td>
</tr>
</tbody>
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*Physical gate length*
VERTICAL DIMENSIONS

Die thickness: 0.3 mm (13 mils)

Layers:

Passivation 2: 0.65 micron
Passivation 1: 0.35 micron
Metal 3 - cap: 0.05 micron
  - aluminum: 1.0 micron
Interlevel dielectric 2 - glass 2: 0.25 - 0.4 micron
  - glass 1: 0.5 - 1.4 micron
Metal 2 - cap: 0.05 micron
  - aluminum: 0.8 micron
Interlevel dielectric 1 - glass 2: 0.4 micron
  - glass 1: 0.4 - 1.5 micron
Metal 1 - cap: 0.05 micron
  - aluminum: 0.55 micron
  - barrier: 0.1 micron
Pre-metal glass: 0.8 micron
Poly: 0.25 micron
Oxide over poly: 0.2 micron
Local Oxide: 0.55 micron
N+ S/D: 0.2 micron
P+ S/D: 0.2 micron
N-well: 6.5 micron
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Mag. 26,000x
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Mag. 13,000x

Mag. 26,000x
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Mag. 26,000x

Mag. 40,000x
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Mag. 26,000x

Mag. 40,000x

Mag. 52,000x

PRE-METAL DIELECTRIC
POLY GATES
P+ S/D

POLY GATE
GATE OXIDE
P+ S/D

POLY GATE
NITRIDE SIDEWALL SPACER
Figure 31. SEM section views of typical birdsbeak profiles.
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Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate

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poly, Mag. 3000x

poly, Mag. 8000x

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poly,
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