Construction Analysis

National Semiconductor LM2672
Simple Switcher® Voltage Regulator

Report Number: SCA 9712-570
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INTRODUCTION

This report describes a construction analysis of the National Semiconductor LM2672 Simple Switcher voltage regulator. Five devices were supplied, encapsulated in 8-pin Dual-In-Line plastic packages (DIP). Date codes were not identifiable.

MAJOR FINDINGS

Questionable Items:¹

• Metal cracks were noted at contact edges.

• Significant silicon in contacts.

Special Features:

• Linear Power BiCMOS process which includes a double diffused (DMOS) process.

• Extended shallow source/drain N-channel transistor structure.

Design Features:

• Large area for double diffused (DMOS) process.

• Large capacitor structures.

¹ These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
TECHNOLOGY DESCRIPTION

Assembly:

- Devices were encapsulated in 8-pin plastic DIPs.

- Lead-locking provisions (anchors and holes) were present at all pins.

- Thermosonic ball bond method employing 1.3 mil O.D. gold wire.

- Silver-filled polyimide die attach.

- Sawn dicing (full depth).

Die Process and Design

- Fabrication process: Linear Power BiCMOS process with N-epi, P-well, P+ iso, and N+ buried layer, incorporating N and P channel MOS, DMOS, NPN and PNP transistors.

- Final passivation: Two layers of passivation were employed. A layer of nitride over a layer of silicon-dioxide.

- Metallization: Two levels of silicon-doped aluminum defined by dry-etch techniques. No caps or barriers were present. Standard contacts and vias (no plugs). In the DMOS area metal 2 was placed directly on metal 1.

- Intermetal Dielectric (IMD): Intermetal dielectric consisted of single layer of glass. No planarization technique was used.

- Pre-metal glass: A single layer of reflow glass was used. Reflow was done prior to contact cuts. Grown and densified oxides were also present.
TECHNOLOGY DESCRIPTION (continued)

- Polysilicon: Single layer of dry-etched polysilicon (no silicide) was used to form all MOS gates on the die. It was also used as the top plate for the thin oxide capacitors. An LDD process was used with spacers removed.

- DMOS devices: A double diffused Hexfet style process was employed. N+ diffusions formed the sources of the transistor elements. Deep P+ diffusions formed the body and inherent body diode. N- epi/buried layer formed the drain.

- CMOS devices: Standard N+ and P+ implanted diffusions formed the sources/drains for these transistors. Sidewall spacers were selectively used and removed. Long shallow N+ LDD extensions were present on one side of some of the NMOS transistors. P-wells and N-epi were used for N-channel devices.

- Bipolar devices: Standard N+ diffusions were used for emitters and collectors of NPN’s and base contacts of PNP devices. The standard base diffusions also used a shallow P+ implant (probably the S/D P+) at contact areas. P+ isolation diffusions were diffused from top and bottom of the epi (to reduce isolation width).

- No buried contacts were employed.
ANALYSIS RESULTS I

Assembly: Figures 1 - 4a

Note: Package analysis was not required. The following data was obtained by observation and is given here as general information.

Questionable Items:1 None.

General Items:

- Devices were packages in 8-pin plastic DIPs.

- Package markings were clear and easy to read. Date codes were not identifiable.

- Overall package quality: Normal. No defects were noted on the external portions of the package. Deflash was of normal quality and workmanship. Lead form was of normal quality and workmanship. No problems were found.

- Die placement: Die was centered and silver-filled polyimide die attach was of good quantity and quality. No problems were found.

- Lead-locking provisions (anchors and holes) were present at all pins.

- Wirebonding: Thermosonic ball bond method using 1.3 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were good (see page 8). Metal 2 on 1 formed the bond pads. Wire spacing and placement was good. Probe mark damage was noted at some test pads. The damage decreased the metal spacing; however, no shorts were noted.

- Die dicing: Die separation was by full depth sawing with good quality workmanship.

1 These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

Die Process and Design:  

Questionable Items:¹

• Metal cracks were noted at contact edges.

• Significant silicon in contacts.

Special Features:

• Linear Power BiCMOS process which includes a double diffused (DMOS) process.

• Extended shallow source/drain N-channel transistor structure.

Design Features:

• Large area for double diffused (DMOS) process.

• Large capacitor structures.

General Items:

• Fabrication process: Linear Power BiCMOS process with N-epi, P-well, P+ iso, and N+ buried layer, incorporating N and P channel MOS, DMOS, NPN and PNP transistors.

• Design and layout: Die layout was clean and efficient. The identification number on the die was 2675.

• Die surface defects: None. No contamination or processing defects were noted.

¹ These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II (continued)

• Final passivation: The passivation consisted of a layer of nitride over a layer of silicon-dioxide. Passivation integrity test indicated defect free passivation. Edge seal was also good. Some residual metal was noted at the die edge; however, no problems are foreseen (Figures 3 and 3a).

• Metallization: Two levels of metal defined by a dry-etch of normal quality. Metal consisted of silicon-doped aluminum. No cap or barrier metals were employed. Standard vias and contacts were used (no plugs).

• Metal defects: None. No notching of the metal layers was present. There was significant silicon mound growth in contact areas following the removal of the metal in the MOSFET area. Worst case silicon mound growth occupied up to 40 percent of contacts and is shown in Figure 24. Cracks were noted at contact edges see Figures 26, 27 and 29.

• Metal step coverage: No significant metal thinning occurred at vias or contacts due to the sloped contact cuts.

• Contacts: Contact cuts appeared to be defined by a wet-etch technique of good quality. No significant over-etching of the contacts was present. No contact pitting was present. Substrate contacts were used to bias the P-wells (Figure 19).

• Intermetal Dielectric (IMD): Intermetal dielectric consisted of single layer of glass. No planarization technique was used. No problems were present.

• Pre-metal glass: A single layer of reflow glass was used over grown oxides. No problems were found.
ANALYSIS RESULTS II (continued)

- Polysilicon: Single layer of dry-etched polysilicon (no silicide) was used to form all MOS gates on the die. It was also used as the top plate for the thin oxide capacitors and gates for the DMOS structure. The LDD process used sidewall spacers which were removed. Large poly capacitor structures were used throughout entire die. No poly resistors were present. No problems were present.

- Isolation: N-epi islands with N+ buried layer separated by P+ isolation. There was good separation between buried layer and isolation with minimal buried layer shift. P-wells were noted in N-epi for N-channel devices. P+ isolation (up and down) diffusions were used to isolate the N-epi islands. A step in the oxide was noted at the P+ iso diffusions.

- DMOS devices: A double diffused process was employed. N+ diffusions formed the sources of the transistor elements. Deep P+ diffusions formed the body and inherent body diode. N- epi/N+ buried layer formed the drain.

- CMOS devices: Standard N+ and P+ implanted diffusions formed the sources/drains for these transistors. Some NMOS transistors used a unique LDD extension on one side of the gate. The step in the oxide would indicates this although the implant was too light to delineate.

- Bipolar devices: All bipolar devices were located in N-epi/N+ buried layers. Standard N+ diffusions were used for emitters and collectors of NPN’s and base contacts of PNP devices. The standard base diffusions also used a shallow P+ implant (probably the S/D P+) at contact areas. P+ isolation diffusions were diffused from top and bottom of the epi (to reduce isolation width).
PROCEDURE

The devices were subjected to the following analysis procedures:

- External inspection
- X-ray
- Decapsulation
- Internal optical inspection
- SEM inspection of assembly features and passivation
- Wirepull test
- Passivation integrity test
- Passivation removal and inspect metal 2
- Delayer to metal 1 and inspect
- Delayer to poly and inspect poly structures and die surface
- Die sectioning (90° for SEM)*
- Measure horizontal dimensions
- Measure vertical dimensions
- Material analysis

*Delineation of cross-sections is by silicon etch unless otherwise indicated.
**OVERALL QUALITY EVALUATION:** Overall Rating: Normal

**DETAIL OF EVALUATION**

<table>
<thead>
<tr>
<th>Category</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package integrity</td>
<td>N</td>
</tr>
<tr>
<td>Package markings</td>
<td>G</td>
</tr>
<tr>
<td>Die placement</td>
<td>G</td>
</tr>
<tr>
<td>Die attach quality</td>
<td>G</td>
</tr>
<tr>
<td>Wire spacing</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond placement</td>
<td>G</td>
</tr>
<tr>
<td>Wirebond quality</td>
<td>G</td>
</tr>
<tr>
<td>Dicing quality</td>
<td>N</td>
</tr>
<tr>
<td>Wirebond method</td>
<td>Thermosonic ball bonds using 1.3 mil gold wire.</td>
</tr>
<tr>
<td>Dicing method:</td>
<td>Sawn (full depth)</td>
</tr>
<tr>
<td>Die attach:</td>
<td>Silver-filled polyimide</td>
</tr>
<tr>
<td>Die surface integrity:</td>
<td></td>
</tr>
<tr>
<td>Tool marks (absence):</td>
<td>NP (probe damage)</td>
</tr>
<tr>
<td>Particles (absence):</td>
<td>N</td>
</tr>
<tr>
<td>Contamination (absence):</td>
<td>N</td>
</tr>
<tr>
<td>Process defects (absence):</td>
<td>N</td>
</tr>
<tr>
<td>General workmanship</td>
<td>N</td>
</tr>
<tr>
<td>Passivation integrity</td>
<td>G</td>
</tr>
<tr>
<td>Metal definition</td>
<td>N</td>
</tr>
<tr>
<td>Metal integrity</td>
<td>NP (cracks at contact edges)</td>
</tr>
<tr>
<td>Contact coverage</td>
<td>G</td>
</tr>
<tr>
<td>Contact registration</td>
<td>N</td>
</tr>
<tr>
<td>Contact defects</td>
<td>NP (some significant silicon mound growth)</td>
</tr>
</tbody>
</table>

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*
PACKAGE MARKINGS

**Top**

(National logo) 66AB
2672 M3.3

**Bottom**

none

**WIREBOND STRENGTH**

Wire material: 1.3 mil diameter gold

Die pad material: Aluminum

**sample 4**

# of wires tested: 11
Bond lifts: 0
Force to break - high: 18g
- low: 17g
- avg.: 17.9g
- std. dev.: 0.28

**DIE MATERIAL ANALYSIS**

Passivation: Nitride over silicon-dioxide.

Die metallization: Aluminum.

Intermetal dielectric: Silicon-dioxide.

Pre-metal glass: Single layer of reflow glass. Grown and densified oxides were also present.
**HORIZONTAL DIMENSIONS**

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
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<tbody>
<tr>
<td>Die size</td>
<td>1.8 x 3.5 mm (73.5 x 140.5 mils)</td>
</tr>
<tr>
<td>Die area</td>
<td>6.3 mm² (10,326 mils²)</td>
</tr>
<tr>
<td>Min pad size</td>
<td>0.13 mm x 0.13 mm (5.1 x 5.1 mils)</td>
</tr>
<tr>
<td>Min pad window</td>
<td>0.11 mm x 0.11 mm (4.4 x 4.4 mils)</td>
</tr>
<tr>
<td>Min metal 2 width</td>
<td>7.3 microns</td>
</tr>
<tr>
<td>Min metal 2 space</td>
<td>7.7 microns</td>
</tr>
<tr>
<td>Min metal 2 pitch</td>
<td>15 microns</td>
</tr>
<tr>
<td>Min via</td>
<td>5.3 microns</td>
</tr>
<tr>
<td>Min metal 1 width</td>
<td>3.4 microns</td>
</tr>
<tr>
<td>Min metal 1 space</td>
<td>4.3 microns</td>
</tr>
<tr>
<td>Min metal 1 pitch</td>
<td>7.7 microns</td>
</tr>
<tr>
<td>Min contact</td>
<td>3 microns</td>
</tr>
<tr>
<td>Min poly width</td>
<td>3.7 microns</td>
</tr>
<tr>
<td>Min poly space</td>
<td>4.7 microns</td>
</tr>
<tr>
<td>Min gate length*</td>
<td></td>
</tr>
<tr>
<td>- (N-channel)</td>
<td>3.7 microns</td>
</tr>
<tr>
<td>- (P-channel)</td>
<td>5.0 microns</td>
</tr>
<tr>
<td>Min N+ emitter</td>
<td>16 microns (round)</td>
</tr>
<tr>
<td>Min P+ emitter</td>
<td>12 microns (round)</td>
</tr>
<tr>
<td>Min P+ isolation</td>
<td>10 microns</td>
</tr>
<tr>
<td>Min edge of base to P+ iso</td>
<td>12 microns</td>
</tr>
<tr>
<td>Min emitter to edge of base</td>
<td>8 microns</td>
</tr>
</tbody>
</table>

*Physical gate length*
VERTICAL DIMENSIONS

Die thickness: 0.35 mm (14 mils)

Layers
Passivation 2: 1.0 micron
Passivation 1: 0.45 micron
Aluminum 2: 2 microns
Intermetal dielectric (IMD): 0.95 micron
Aluminum 1: 0.75 micron
Pre-metal glass: 0.65 micron
Poly: 0.4 micron
Local oxide: 1 micron
N+ S/D diffusion: 0.6 micron
P+ S/D diffusion: 0.45 micron
P DMOS body: 5.5 microns
P+ base (NPN): 2.8 microns
N+ (DMOS): 10 microns
N+ emitter and collector (NPN): 0.6 micron
N- epi: 4.5 microns
P-well: 5.5 microns
N+ buried layer: 24 microns (from surface)
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Mag. 7000x

Mag. 20,000x
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resistors

NPN transistor

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