Construction Analysis

Melexis
ELEX 16201C Device

Report Number: SCA 9712-571
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INTRODUCTION

This report describes a construction analysis of the Melexis Elex 16201C device. Five devices encapsulated in 20-pin Small Outline Integrated Circuit (SOIC) packages were supplied for the analysis.

MAJOR FINDINGS

Questionable Items: ¹

• This device had severe metal patterning problems and proper functioning of the device is unlikely.

• Metal 2 was severely overetched apparently during patterning which reduced original line widths by 80 percent (Figures 14-17).

• Metal 1 shorts were noted in the decode circuitry near the SRAM array (Figures 21-23).

• Metal 1 aluminum also thinned up to 85 percent ² in worst cases. Typical Metal 1 aluminum thinning was 75 percent ².

Note: These metal problems represent some of the most severe processing defects we’ve analyzed.

Special Features: None.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

Assembly:

• The devices were packaged in 20-pin Small Outline Integrated Circuit (SOIC) packages for surface mount applications.

• Lead-locking provisions (holes and/or anchors) at all pins.

• Thermosonic ball bond method employing 1.3 mil O.D. gold wire.

• All pins were connected.

• Die separation by sawn dicing.

• Silver epoxy die attach.

Die Process

• Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-epi, on a P-substrate.

• Die coat: No die coat was present.

• Overlay passivation: A single layer of nitride over a layer of silicon-dioxide.

• Bonding pads: Both Metal 2 and Metal 1 were used to form the bonding pads. Metal 2 via arrays were employed along the perimeter of the bond pads.

• Metallization: Two levels of metal were present. Both Metal 2 and 1 consisted of a layer of aluminum. No cap or barrier metals were employed on either metal. Both metallization layers were defined by dry-etch techniques. Standard vias and contacts were used (no plugs).
TECHNOLOGY DESCRIPTION (continued)

• Intermetal dielectric: Two layers of silicon-dioxide. The dielectric layer appeared to have been subjected to a etchback. Via cuts through this layer appeared to have been wet-etched.

• Pre-metal glass: A reflow glass over a densified oxide. This layer appeared to have been reflowed following contact cuts.

• Polysilicon: A single layer of poly was used on the die. Poly (no silicide) was used to form all gates on the die, the word lines and one plate of the capacitors in the EEPROM cell array. Direct poly-to-diffusion (buried) contacts were not used. Definition of the poly was by a dry etch.

• Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were present with the transistors to provide the LDD spacing and were left in place.

• Local oxide (LOCOS) isolation. A slight step was present in the oxide at the edge of the well boundaries which indicates a twin-well process was used.

• Wells: Twin-wells in a P-epi, on a P substrate.

• SRAM memory cells: A 6T CMOS SRAM cell design. Poly was used as the word lines, pull-up devices and storage gates. Metal 1 formed the bit lines and distributed GND and VCC to each individual cell. Cell size was 14.6 x 23 microns.

• EEPROM cell array: The memory cell consisted of a 3T, single capacitor, EEPROM design. Metal was used to form the bit lines. Poly was used to form the word/select lines, one plate of the capacitor and the tunnel-oxide device. Cell size was 13.3 x 35.7 microns.

• ROM cell array: A NAND ROM cell design was employed. Single transistor cell size was 6.2 x 28.8 microns. Implants are used to program the memory cells.
ANALYSIS RESULTS I

Assembly:  

Figures 1 - 8

Questionable Items: ¹ None.

General Items:

- Devices were packaged in 20-pin Small Outline Integrated Circuit (SOIC) packages for surface mount applications.

- Overall package quality: Normal. No defects were found on the external or internal portions of the packages. Leads were well formed and tinning was complete. No gaps were noted at lead exits.

- Lead-locking provisions (anchors and/or holes) were present.

- Wirebonding: Thermosonic ball bond method using 1.3 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were good (see page 11). Wire spacing and placement was normal.

- Die attach: Silver-epoxy die attach of normal quality. Some small voids were noted in the epoxy located at the edge of the die, but no problems are foreseen. The die placement on the header was slightly offset; however, and no problems were noted (Figure 5a).

- Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

Die Process and Design:  

Questionable Items:\(^1\)

- This device had severe metal patterning problems and proper functioning of the device is unlikely.

- Metal 2 was severly overetched apparently during patterning which reduced original line widths by 80 percent (Figures 14-17).

- Metal 1 shorts were noted in the decode circuitry near the SRAM array (Figures 21-23).

- Metal 1 aluminum also thinned up to 85 percent\(^2\) in worst cases. Typical Metal 1 aluminum thinning was 75 percent\(^2\).

Note: These metal problems represent some of the most severe processing defects we’ve analyzed.

Special Features:  None.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-epi, on a P substrate.

\(^1\)These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

\(^2\)Seriousness depends on design margins.
ANALYSIS RESULTS II (continued)

- Design and layout: Die layout was clean and efficient. Alignment was good at all levels.

- Die surface defects: None. No contamination or toolmarks were noted.

- Overlay passivation: A single layer of nitride over a layer of silicon-dioxide. Passivation integrity tests indicated defect-free passivation. Edge seal was good. Some active metal 2 lines were carried into the scribe lane and left exposed. (see Figure 11a). This is unusual since it leaves the active line subjected to contamination and moisture.

- Metallization: Two levels of metallization. Both Metal 2 and 1 consisted of a layer of aluminum. No cap or barrier metals were employed on either metal. Metal 1 formed the bit lines within the SRAM, EEPROM, and ROM cell arrays. Standard vias and contacts were used (no plugs).

- Metal patterning: Both metal layers were defined by a dry etch. Overetching of the Metal 2 was apparent. The lack of Metal 2 patterning control resulted in “jadded” lines which reduced line widths by 80 percent. These anomalies indicate extremely poor processing control. Although Metal 1 patterning was normal, Metal 1 shorts were also noted in the decode circuitry near the SRAM array (Figures 21-23), again illustrating poor processing control. It is highly unlikely that this device would operate properly. Three of the five devices were decapped and the anomalies were noted on all three devices.

- Metal defects: Severe patterning anomalies. (See above).
ANALYSIS RESULTS II (continued)

- Metal step coverage: Due to Metal 2 being overetched an accurate measurement of aluminum thinning could not be performed. Worst case Metal 1 aluminum thinned up to 85 percent at contact edges. Typical Metal 1 aluminum thinning was 75 percent. MIL-STD allows up to 70 percent metal thinning for contacts of this size. Metal lines were widened around contacts and contacts were completely surrounded by metal.

- Contacts: Metal 2 vias and Metal 1 contact cuts appeared to have been wet-etched. Contacts appeared to be reflowed. Some minor over-etching of the contacts was present. The contact cuts penetrated up to 40 percent of the polysilicon thickness and diffusion depths. However, no full penetration through the junctions was found.

- Intermetal dielectric: Two layers of silicon dioxide. The dielectric layer appeared to have been subjected to a etchback. Via cuts through this layer appeared to have been wet-etched.

- Pre-metal glass: A reflow glass over a densified oxide. This layer appeared to have been reflowed following contact cuts. No problems were found.

- Polysilicon: A single layer of poly was used on the die. Poly (no silicide) was used to form all gates on the die, the word lines and one plate of the capacitors in the EEPROM cell array. Definition of the poly was by a dry etch of normal quality. Poly lines extended into the scribe lane (which is unusual) and the poly appeared to be covered by the interlevel dielectric (see Figure 11a).

- Isolation: Local oxide (LOCOS) isolation was used. No problems were noted. The slight step present in the oxide at the well boundary indicates a twin-well process was employed. The P-well could not be delineated in cross-section.
ANALYSIS RESULTS II (continued)

- Diffusions: Standard implanted N+ and P+ diffusions were used for the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No silicide was present over diffusions.

- Wells: Twin-wells in a P-epi, on a P substrate. A step was present in the LOCOS at the well boundaries.

- Buried contacts: Direct poly-to-diffusion (buried) contacts were not used.

- SRAM memory cells: A 6T CMOS SRAM cell design. Poly was used as the word lines, pull-up devices and storage gates. Metal 1 formed the bit lines and distributed GND and VCC to each individual cell. Cell size was 14.6 x 23 microns.

- EEPROM cell array: The memory cell consisted of a 3T, single capacitor, EEPROM design. Metal was used to form the bit lines. Poly was used to form the word/select lines, one plate of the capacitor and the tunnel-oxide device. Cell size was 13.3 x 35.7 microns.

- ROM cell array: A NAND ROM cell design was employed. Single transistor cell size was 6.2 x 28.8 microns. Special implants are used to program the memory cells.
The devices were subjected to the following analysis procedures:

External inspection
X-ray
Package section
Decapsulation
Internal optical inspection
SEM inspection of assembly features and passivation
Passivation integrity test
Wirepull tests
Passivation removal
SEM inspection of metal 2
Delayer to metal 1
SEM inspection of metal 1
Delayer to poly and inspect poly structures and die surface
Die sectioning (90° for SEM)*
Measure horizontal dimensions
Measure vertical dimensions
Die material analysis

*Delineation of cross-sections is by silicon etch unless otherwise indicated.
OVERALL QUALITY EVALUATION: Overall Rating: Poor

DETAIL OF EVALUATION

Package integrity G
Package markings G
Die placement N
Die attach quality N
Wire spacing G
Wirebond placement G
Wirebond quality G
Dicing quality G
Wirebond method Thermosonic ball bonds using 1.3 mil gold wire.
Die attach method Silver-epoxy
Dicing method Sawn

Die surface integrity:
  Tool marks (absence) G
  Particles (absence) G
  Contamination (absence) G
  Process defects (absence) P

General workmanship P
Passivation integrity G
Metal definition P
Metal integrity P
Contact coverage G
Contact registration G
Contact defects N

1Severe metal patterning problems (both metals).

G = Good, P = Poor, N = Normal, NP = Normal/Poor
PACKAGE MARKINGS

<table>
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<tr>
<td>ELEX 16201C</td>
<td>Philippines</td>
</tr>
<tr>
<td>7537A 4996</td>
<td></td>
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WIREBOND STRENGTH

Wire material: 1.3 mil diameter gold
Die pad material: aluminum
Material at package post: silver

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<th>Sample #</th>
<th>1</th>
<th>2</th>
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<tr>
<td># of wires tested:</td>
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<td>20</td>
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<tr>
<td>Bond lifts:</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Force to break - high:</td>
<td>21g</td>
<td>25g</td>
</tr>
<tr>
<td>- low:</td>
<td>10g</td>
<td>12g</td>
</tr>
<tr>
<td>- avg.:</td>
<td>16g</td>
<td>17.5g</td>
</tr>
<tr>
<td>- std. dev.:</td>
<td>2.7</td>
<td>3.3</td>
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DIE MATERIAL ANALYSIS (WDX AND EDX)

Passivation: A single layer of nitride over a layer of silicon-dioxide.
Metal 2: Aluminum
Intermetal dielectric: Two layers of silicon-dioxide.
Metal 1: Aluminum.
Pre-metal glass: A reflow glass over a densified oxide.
### HORIZONTAL DIMENSIONS

<table>
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<tr>
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<tr>
<td>Die size:</td>
<td>4.4 x 7.2 mm (176 x 287 mils)</td>
</tr>
<tr>
<td>Die area:</td>
<td>31.6 mm$^2$ (50,512 mils$^2$)</td>
</tr>
<tr>
<td>Min pad size:</td>
<td>0.15 x 0.15 mm (6 x 6 mils)</td>
</tr>
<tr>
<td>Min pad window:</td>
<td>0.11 x 0.11 mm (4.7 x 4.7 mils)</td>
</tr>
<tr>
<td>Min pad space:</td>
<td>0.5 mm (19.5 mils)</td>
</tr>
<tr>
<td>Min pad to metal:</td>
<td>10 microns</td>
</tr>
<tr>
<td>Min metal 2 width:</td>
<td>1.35 microns</td>
</tr>
<tr>
<td>Min metal 2 space:</td>
<td>2.7 microns</td>
</tr>
<tr>
<td>Min via:</td>
<td>1.0 microns (round)</td>
</tr>
<tr>
<td>Min metal 1 width:</td>
<td>1.2 micron</td>
</tr>
<tr>
<td>Min metal 1 space:</td>
<td>1.4 micron</td>
</tr>
<tr>
<td>Min metal 1 pitch:</td>
<td>2.6 microns</td>
</tr>
<tr>
<td>Min contact:</td>
<td>1.4 micron (round)</td>
</tr>
<tr>
<td>Min poly width:</td>
<td>1.0 micron</td>
</tr>
<tr>
<td>Min poly space:</td>
<td>1.3 micron</td>
</tr>
<tr>
<td>Min poly pitch:</td>
<td>2.3 microns</td>
</tr>
<tr>
<td>Min gate length* - (N-channel):</td>
<td>1.0 micron</td>
</tr>
<tr>
<td>- (P-channel):</td>
<td>1.1 micron</td>
</tr>
<tr>
<td>EEPROM cell size:</td>
<td>474 microns$^2$</td>
</tr>
<tr>
<td>EEPROM cell pitch:</td>
<td>13.3 x 35.7 microns</td>
</tr>
<tr>
<td>ROM cell size:</td>
<td>178 microns$^2$</td>
</tr>
<tr>
<td>ROM cell pitch:</td>
<td>6.2 x 28.8 microns</td>
</tr>
<tr>
<td>SRAM cell size:</td>
<td>335 microns$^2$</td>
</tr>
<tr>
<td>SRAM cell pitch:</td>
<td>14.6 x 23 microns</td>
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*Physical gate length.*
## VERTICAL DIMENSIONS

**Die thickness:** 0.6 mm (25 mils)

### Layers

- **Passivation 2:** 0.8 micron
- **Passivation 1:** 0.4 micron
- **Metallization 2:** 1.0 micron
- **Intermetal dielectric:** 1.2 micron
- **Metallization 1:** 0.65 micron
- **Pre-metal glass:** 0.5 micron
- **Poly:** 0.3 micron
- **Oxide over N+:** 0.1 micron
- **Oxide over P+:** 0.09 micron
- **Local oxide:** 0.6 micron
- **N+ diffusion:** 0.55 micron
- **P+ diffusion:** 0.4 micron
- **N-well:** 5.3 microns
- **P-epi:** 13.5 microns
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as polished

delineated
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Figure 18. SEM section views of metal 1 line profiles.

Mag. 20,000x

Mag. 30,000x
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Figure 21. Topological SEM views illustrating metal 1 short. 0°.

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Figure 23. Additional topological SEM views illustrating metal 1 shorts. $0^\circ$. 
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Mag. 16,000x
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Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly, Red = Diffusion, and Gray = Substrate

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Mag. 200x

passivated, Mag. 500x