Construction Analysis

Macronix 27C8100PC-10
8Mbit NAND EPROM

Report Number: SCA 9712-572
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INTRODUCTION

This report describes a construction analysis of the Macronix 27C8100PC-10, 8Mbit NAND EPROM (OTP). Two samples were received for the analysis. The devices were packaged in 42-pin Dual In-Line plastic Packages (DIPs) date coded 9717.

MAJOR FINDINGS

Questionable Items:

1. Metal 1 aluminum thinned up to 100 percent at some locations of some contacts. Barrier metal remained intact to provide continuity.

Special Features:

- Unique cell design.

---

1These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application

2Seriousness depends on design margins.
TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 42-pin plastic Dual In-Line Packages (DIPs).

- The copper (Cu) leadframe was internally plated with silver (Ag).

- External pins were tinned with tin-lead (SnPb) solder.

- Lead-locking provisions were present at all pins.

- Thermosonic wirebonding using 1.2 mil O.D. gold wire.

- Sawn dicing (full depth).

- Silver epoxy die attach.

Die Process:

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P-substrate.

- Die coat: No die coat was present.

- Final passivation: Three layers of passivation with a planarizing SOG between. As determined by etch characteristics, passivation 1 and 3 appeared to be nitride. However, this is unusual for a UV EPROM to have nitride overlay.

- Metallization: A single level of metal defined by standard dry-etch techniques. The metal consisted of aluminum with a titanium-nitride cap and titanium-nitride/titanium barrier. Standard contacts were employed throughout (no plugs).

- Pre-metal dielectric: A single layer of reflow glass over densified oxide.
TECHNOLOGY DESCRIPTION (continued)

- Polysilicon: Three layers of dry-etched polysilicon. Poly 3 (tungsten silicide on poly) was used to form all peripheral gates on the die and program lines in the array. Poly 3 was also used to form the control lines in the array. Poly 2 was used in conjunction with poly 1 to form all floating gates in the array. Direct poly-to-diffusion contacts were not used.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process using shallow S/D implants was used with the oxide sidewall spacers left in place.

- Isolation: LOCOS (local oxide isolation).

- Wells: N-wells in a P-substrate. No step was present at well boundaries.

- Redundancy: Poly 3 redundancy fuses were present on the die. Some laser blown fuses were noted. Cutouts in the passivation were present over all fuses.

- Memory cells: The UV EPROM array employed a unique stacked gate structure implemented in a NAND configuration. Metal 1 formed the bit lines and carried GND. Poly 1 was used for all memory gates although it was contacted directly by poly 2 at floating gates. Poly 1 also defined the channel region for control gates, but was removed prior to poly 3 formation. The same gate oxide is thus present in both locations. Poly 3 formed all program and control lines in the array.
ANALYSIS RESULTS I

Assembly:  

Figures 1 - 4

Questionable Items:¹ None.

General Items:

• Devices were packaged in 42-pin plastic DIPs.

• Overall package quality: Good. No defects were found on the external or internal portions of the packages. External pins were well formed and no voids or cracks were noted.

• Wirebonding: Thermosonic bond method using 1.2 mil O.D. gold wire. Wire spacing and placement was good. No problems were noted.

• Die attach: Silver epoxy die attach of good quality.

• Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die edges.

• Die coat: No die coat was used on the die.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.
ANALYSIS RESULTS II

Die Process and Design:  

Questionable Items:¹

- Metal 1 aluminum thinned up to 100 percent² at some locations of some contacts. Barrier metal remained intact to provide continuity.

Special Features:

- Unique cell design.

General Items:

- Fabrication process: Devices were fabricated using selective oxidation CMOS process employing N-wells in a P-substrate.

- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.

- Surface defects: No toolmarks, masking defects, or contamination areas were found.

- Die coat: No die coat was used.

- Final passivation: Three layers of passivation with an SOG layer to planarize the surface. As stated above, passivation 1 and 3 appeared to be nitride. Edge seal was good as the passivation extended beyond the metallization.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.
ANALYSIS RESULTS II (continued)

• Metallization: A single level of metal was used. It consisted of aluminum with a titanium-nitride cap and a titanium-nitride on titanium barrier. Standard contacts were used (no plugs).

• Metal patterning: The metal layer was defined by a dry etch of normal quality.

• Metal defects: None. No voiding, notching or cracking of the metal layer was found. No silicon nodules were found following removal of the metal layer.

• Metal step coverage: Aluminum thinned up to 100 percent at some contacts. Barrier metal remained intact to provide continuity. This thinning was a result of minimum contact spacing. Normal metal thinning was typically 70 percent.

• Contacts: All contact cuts were defined by a dry etch of normal quality. Alignment of the metal was good. No overetching was present.

• Pre-metal dielectric: A layer of reflow glass (BPSG) over densified oxide was used under the metal layer. Reflow was performed after contact cuts and resulted in well rounded steps. No problems were found.

• Polysilicon: Three layers of polysilicon were used. Poly 3 (tungsten silicide on poly) was used to form all peripheral gates on the die and program lines in the array (over poly 2). Poly 3 was also used to form the control lines in the array. Poly 2 was used in conjunction with poly 1 to form all floating gates in the array. Definition of all layers was by a dry-etch of normal quality. Direct poly-to-diffusion contacts were not used.

• Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process using shallow S/D implants was used with oxide sidewall spacers left in place. No problems were found.

• Isolation: LOCOS (local oxide isolation). No step was present at well boundaries.
ANALYSIS RESULTS II (continued)

• Wells: N-wells formed in a P-substrate. No problems were found.

• Redundancy: Poly 3 redundancy fuses were present on the die. Some laser blown fuses were noted. Cutouts were present in the passivation over all fuses. No problems were found.

• Memory cells: The EPROM array employed a unique stacked gate structure implemented in a NAND configuration. Metal 1 formed the bit lines and carried GND. Poly 1 was used for all memory gates although it was contacted directly by poly 2 at floating gates. Poly 1 also defined the channel region for control gates, but was removed prior to poly 3 formation. The same gate oxide is thus present in both locations. Poly 3 formed all program and control lines in the array.
The devices were subjected to the following analysis procedures:

- External inspection
- X-ray
- Decapsulate
- Internal optical inspection
- SEM of assembly features and passivation
- Passivation integrity test
- Passivation removal
- SEM inspection of metal
- Aluminum removal and inspect contacts
- Delayer to silicon and inspect poly/die surface
- Die sectioning (90° for SEM)*
- Measure horizontal dimensions
- Measure vertical dimensions

*Delineation of cross-sections is by silicon etch unless otherwise indicated.
OVERALL QUALITY EVALUATION: Overall Rating: Normal to Poor.

DETAIL OF EVALUATION

Package integrity G
Package markings G
Die placement G
Wirebond placement G
Wirebond quality N
Dicing quality N
Die attach quality N
Die attach method Silver epoxy
Dicing method: Sawn (full depth)
Wirebond method Thermosonic ball bonds using 1.2 mil O.D. gold wire

Die surface integrity:
  Toolmarks (absence) G
  Particles (absence) G
  Contamination (absence) G
  Process defects (absence) N

General workmanship N
Passivation integrity G
Metal definition N
Metal integrity NP
Metal registration G
Contact coverage G
Contact registration G

G = Good, P = Poor, N = Normal, NP = Normal/Poor
PACKAGE MARKINGS

TOP

MX (logo) 27C8100PC-10
M12829
TAIWAN
B9717 VPP = 12.5V

BOTTOM

B9717
M12829

DIE MATERIALS

Overlay passivation: Layer of glass over two layers of nitride?
with an SOG between.

Metallization: Aluminum with a titanium-nitride cap and a
titanium-nitride on titanium barrier.

Pre-metal dielectric: Reflow glass (BPSG).

Polycide: Tungsten-silicide on polysilicon.
**HORIZONTAL DIMENSIONS**

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die size</td>
<td>7.4 x 7.5 mm (291 x 294 mils)</td>
</tr>
<tr>
<td>Die area</td>
<td>55.5 mm² (85,554 mils²)</td>
</tr>
<tr>
<td>Min pad size</td>
<td>0.1 x 0.1 mm (3.9 x 3.9 mils)</td>
</tr>
<tr>
<td>Min pad window</td>
<td>0.09 x 0.09 mm (3.5 x 3.5 mils)</td>
</tr>
<tr>
<td>Min pad space</td>
<td>0.02 mm</td>
</tr>
<tr>
<td>Min metal width</td>
<td>0.9 micron</td>
</tr>
<tr>
<td>Min metal space</td>
<td>1.0 micron</td>
</tr>
<tr>
<td>Min metal pitch (uncontacted)</td>
<td>1.9 micron</td>
</tr>
<tr>
<td>Min metal pitch (contacted):</td>
<td>2.5 microns</td>
</tr>
<tr>
<td>Min contact</td>
<td>0.9 micron (round)</td>
</tr>
<tr>
<td>Min poly 3 width</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>Min poly 3 space</td>
<td>0.6 micron</td>
</tr>
<tr>
<td>Min diffusion spacing</td>
<td>0.75 micron</td>
</tr>
<tr>
<td>Min gate length*</td>
<td></td>
</tr>
<tr>
<td>- (N-channel):</td>
<td>0.8 micron</td>
</tr>
<tr>
<td>- (P-channel):</td>
<td>0.9 micron</td>
</tr>
<tr>
<td>Min poly 2/poly 1 width</td>
<td></td>
</tr>
<tr>
<td>- (floating gate):</td>
<td>0.6 micron</td>
</tr>
</tbody>
</table>

**VERTICAL DIMENSIONS**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die thickness</td>
<td>0.5 mm (19 mils)</td>
</tr>
<tr>
<td>Layers</td>
<td></td>
</tr>
<tr>
<td>Passivation 4</td>
<td>0.8 micron</td>
</tr>
<tr>
<td>Passivation 3</td>
<td>0.65 micron</td>
</tr>
<tr>
<td>Passivation 2 (SOG)</td>
<td>0 - 1.5 micron</td>
</tr>
<tr>
<td>Passivation 1</td>
<td>0.35 micron</td>
</tr>
<tr>
<td>Metal 1 - cap</td>
<td>0.05 micron (approx.)</td>
</tr>
<tr>
<td>- aluminum</td>
<td>0.9 micron</td>
</tr>
<tr>
<td>- TiN/Ti barrier</td>
<td>0.15 micron</td>
</tr>
<tr>
<td>Pre-metal glass</td>
<td>0.35 micron (average)</td>
</tr>
<tr>
<td>Poly 3 - silicide</td>
<td>0.13 micron</td>
</tr>
<tr>
<td>- poly</td>
<td>0.17 micron</td>
</tr>
<tr>
<td>Poly 2</td>
<td>0.06 micron (approx.)</td>
</tr>
<tr>
<td>Poly 1</td>
<td>0.06 micron (approx.)</td>
</tr>
<tr>
<td>Local oxide</td>
<td>0.5 micron</td>
</tr>
<tr>
<td>N+ S/D diffusion†</td>
<td>0.2 micron</td>
</tr>
<tr>
<td>P+ S/D diffusion</td>
<td>0.3 micron</td>
</tr>
<tr>
<td>N-well</td>
<td>2.5 microns (approx.)</td>
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*Physical gate length.
†Shallow S/D implant could not be delineated well enough to measure.
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Mag. 1500x

Mag. 6500x
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