1995 SUCCESSFUL TECHNOLOGIES REVIEW

EXPLANATION OF FORMAT

This book is organized into sections by product types.

In all cases an initial overview of each section is followed by summary tables comparing design rule dimensions, layer thicknesses, and materials used. In a few cases, data reported in a previous year is included to allow comparison or provide background.

This is then followed by a highly concentrated technology discussion of each product included, and example figures illustrating the most innovative features of the technology. (Full reports covering each individual product are available separately).

The discussions have been organized to be as concise and similar to each other as possible in order to facilitate ease of comparison. Careful reading will demonstrate that very detailed information is in fact provided.

In almost all cases no information about the technology was provided by the manufacturer and all information reflects our interpretation of analysis results. No electrical testing of the circuits was done by ICE so functionality and speeds are as reported by our clients or in product literature.

All analysis was done at ICE's own laboratories during 1994 (although a few parts were date coded 1993).
OVERVIEW OF
1994 TECHNOLOGY

As usual, a number of interesting and in some cases at least, unexpected developments occurred during 1994.

The most noticeable of these was in the DRAM area where we not only saw our first 64 Mb DRAMs, but also learned how slow they are in getting into production and how persistent the 16 Mb parts became. In fact, we found out that some manufacturers are now into their fourth 16 Mb design, a record as far as we know.

In SRAMs the focus this last year seems to have shifted to byte-wide organizations like 64K x 18/16. Here also we have not seen a rush of activity into the 4 Mb designs although NEC’s 64K x 18 does incorporate their 4 Mb cell design.

Flash has not lost much impetus and showed interesting design features, namely that redesign of the cell is not necessary (or possible?). All one really needs to do to cram more bits into a package is to shrink dimensions and/or stack more than one die in a package (e.g., Intel 32 Mb). Based on this kind of pressure to reduce design rules, we would expect these parts to be at the leading edge in small features, but this has so far not been the case.

The broad category of programable devices covering FPGAs, EPLAs, and EPLDs continue to represent mature technology with either a clever circuit design or a unique special process feature. These include anything from anti-fuse to one-time programable UVEPROMs to EEPROMs, etc. No drastically new items were seen this year, but the normal process and design rule trends do result in dice with larger capacities or new circuit features.

Microprocessors continue to be very active in pushing the technology, even more so than DRAMs. As proof of this the minimum gate lengths observed (0.3 micron) this year were on the latest NEC MIPS design, the most metal levels on IBM and Intel entries, and the only evidence so far of shallow trench isolation, on the IBM parts. Also CMP planarization and use of plugs for vertical interconnect is more prevalent in this product category then elsewhere.

Overall we observed the following trends.

- Smaller dimensions of course, reaching 0.3 micron gate lengths (although 0.45 or 0.5 micron is much more common). Also 0.5 micron metal widths and in a few cases, spacing.

- Contacts in the 0.6 micron to 0.8 micron. DRAM cells less than 2 micron² (1.6 micron minimum) and SRAM cells at 18 microns² on dedicated SRAM parts, but very close (21 microns²) on CPUs.
• More levels of interconnect. Three or four (including metal substitute layers like polycides) are now becoming common and we have in fact seen six levels of metal.

• Also more use of wells and implants and a slow trend towards more chemical-mechanical planarization (CMP).

• Missing this year were larger dice. The largest seen being some 20 percent smaller than reported on last year.
# TABLE OF MOST AGGRESSIVE FEATURE SIZES

The following table shows the most aggressive features ICE observed in 1994.

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<th>FEATURE SIZES</th>
<th>PRODUCT</th>
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<td>Min via (metal to metal)</td>
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