SRAMs

Most interest this year seems to have been in the x16 or x18 organizations at the 1 Mb level.

We thus report on four new parts in this category and have included the data in the tables on the Sharp device (reported on last year) to allow comparisons.

On these devices, only NEC made use of thin-film-transistors (TFT) pullups, everyone else so far is sticking with the standard 4T cell using resistive pullups. It may be of interest here to note that although NEC’s TFT cell on the dedicated SRAM product is only 18 microns$^2$, their 4T cell used in the cache SRAM array on their R4400MC microprocessor only measures 21 microns$^2$.

Die and cell sizes varied considerably and possibly of most interest here is the fact that although NEC’s TFT cell is the smallest (and certainly the most complex), Samsung’s die is smaller.

All parts were made by CMOS process technologies and only Micron made use of plugs for vertical interconnect, and CMP.
# Horizontal Dimensions (Design Rules)

## SRAMs

<table>
<thead>
<tr>
<th>SRAMs</th>
<th>Hitachi HM621864HJP-20 1Mb (x18) 9428</th>
<th>NEC D431018LE-15 1Mb (x18) 9327</th>
<th>Micron MT5C64K16A1-12 1Mb (x16) 9432</th>
<th>Samsung KM6161002J-15 1Mb (x16) 9418</th>
<th>Sharp LH521028U-20 1Mb (x16) 9329 (see 1994 report)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Die size</strong></td>
<td>6.45 x 13.8 mm (88 mm²)</td>
<td>5.8 x 12.7 mm (74 mm²)</td>
<td>5.8 x 12.7 mm (74 mm²)</td>
<td>5.2 x 11.3 mm (59 mm²)</td>
<td>10 x 12 mm (120 mm²)</td>
</tr>
<tr>
<td><strong>Min M2 width</strong></td>
<td>1.2µm</td>
<td>1.0µm</td>
<td>2.7µm</td>
<td>0.9µm</td>
<td>1.0µm</td>
</tr>
<tr>
<td><strong>Min M1 width</strong></td>
<td>1.2µm</td>
<td>0.9µm</td>
<td>1.2µm</td>
<td>0.9µm</td>
<td>0.7µm</td>
</tr>
<tr>
<td><strong>Min M2 space</strong></td>
<td>1.1µm</td>
<td>1.0µm</td>
<td>1.0µm</td>
<td>1.0µm</td>
<td>1.7µm</td>
</tr>
<tr>
<td><strong>Min M1 space</strong></td>
<td>1.0µm</td>
<td>0.8µm</td>
<td>1.1µm</td>
<td>1.0µm</td>
<td>0.8µm</td>
</tr>
<tr>
<td><strong>Min via (Met. to Met.)</strong></td>
<td>1.0µm</td>
<td>0.85µm</td>
<td>1.8µm</td>
<td>1.2µm</td>
<td>1.0µm</td>
</tr>
<tr>
<td><strong>Min cntct (Met. to Si)</strong></td>
<td>1.0µm</td>
<td>0.75µm</td>
<td>0.7µm</td>
<td>0.9µm</td>
<td>1.0µm</td>
</tr>
<tr>
<td><strong>Min Poly 4</strong></td>
<td>NA</td>
<td>0.4µm</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td><strong>Min Poly 3</strong></td>
<td>NA</td>
<td>1.0µm</td>
<td>NA</td>
<td>0.45µm*</td>
<td>NA</td>
</tr>
<tr>
<td><strong>Min Poly 2</strong></td>
<td>0.55µm</td>
<td>1.5µm*</td>
<td>0.9µm</td>
<td>0.5µm</td>
<td>1.0µm</td>
</tr>
<tr>
<td><strong>Min Poly 1</strong></td>
<td>0.7µm*</td>
<td>0.4µm*</td>
<td>0.55µm</td>
<td>0.45µm*</td>
<td>0.5µm*</td>
</tr>
<tr>
<td><strong>Min gate - (N)†</strong></td>
<td>0.7µm</td>
<td>0.4µm</td>
<td>0.55µm</td>
<td>0.45µm</td>
<td>0.5µm</td>
</tr>
<tr>
<td><strong>Min gate - (P)†</strong></td>
<td>0.7µm</td>
<td>0.6µm</td>
<td>0.5µm</td>
<td>0.5µm</td>
<td>0.7µm</td>
</tr>
<tr>
<td><strong>Cell pitch</strong></td>
<td>4.4 x 6.8µm</td>
<td>3.2 x 5.6µm</td>
<td>4.3 x 7.5µm</td>
<td>3.8 x 5.9µm</td>
<td>5.5 x 8µm</td>
</tr>
<tr>
<td><strong>Cell area</strong></td>
<td>30µm²</td>
<td>18µm²</td>
<td>32µm²</td>
<td>22µm²</td>
<td>44µm²</td>
</tr>
</tbody>
</table>

*Polycide  †Physical gate length  

**TABLE 2 - 1**
<table>
<thead>
<tr>
<th>SRAMs</th>
<th>Hitachi HM621864HJP-20 1Mb (x18) 9428</th>
<th>NEC D431018LE-15 1Mb (x18) 9327</th>
<th>Micron MT5C64K16A1-12 1Mb (x16) 9432</th>
<th>Samsung KM6161002J-15 1Mb (x16) 9418</th>
<th>Sharp LH521028U-20 1Mb (x16) 9329 (see 1994 report)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final passivation</td>
<td>1.4µm</td>
<td>0.75µm</td>
<td>1.5µm</td>
<td>1.0µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>Metal 2</td>
<td>0.85µm</td>
<td>1.0µm</td>
<td>1.25µm</td>
<td>1.3µm</td>
<td>1.15µm</td>
</tr>
<tr>
<td>Metal 1</td>
<td>0.75µm</td>
<td>1.0µm</td>
<td>0.7µm</td>
<td>0.6µm</td>
<td>0.9µm</td>
</tr>
<tr>
<td>Intermetal dielectric</td>
<td>0.3µm</td>
<td>0.6µm</td>
<td>0.7µm</td>
<td>0.5µm</td>
<td>0.7µm</td>
</tr>
<tr>
<td>Poly 4</td>
<td>NA</td>
<td>0.05µm</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Poly 3</td>
<td>NA</td>
<td>0.05µm</td>
<td>NA</td>
<td>0.25µm*</td>
<td>NA</td>
</tr>
<tr>
<td>Poly 2</td>
<td>0.07µm</td>
<td>0.13µm*</td>
<td>0.08µm</td>
<td>0.08µm</td>
<td>0.13µm</td>
</tr>
<tr>
<td>Poly 1</td>
<td>0.25µm*</td>
<td>0.25µm*</td>
<td>0.35µm</td>
<td>0.3µm*</td>
<td>0.3µm*</td>
</tr>
<tr>
<td>Recessed oxide</td>
<td>0.35µm</td>
<td>0.4µm</td>
<td>0.55µm</td>
<td>0.4µm</td>
<td>0.5µm</td>
</tr>
<tr>
<td>N-well</td>
<td>?µm</td>
<td>5µm</td>
<td>6.5µm</td>
<td>6.5µm</td>
<td>?µm</td>
</tr>
<tr>
<td>P-well</td>
<td>4µm</td>
<td>4µm</td>
<td>4.5µm</td>
<td>4µm</td>
<td>2µm</td>
</tr>
<tr>
<td>Epi</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>

*Polycide

**TABLE 2 - 2**
### Die Materials

<table>
<thead>
<tr>
<th>SRAMs</th>
<th>Hitachi</th>
<th>NEC</th>
<th>Micron</th>
<th>Samsung</th>
<th>Sharp</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HM621864HJP-20</td>
<td>D431018LE-15</td>
<td>MT5C64K16A1-12</td>
<td>KM6161002J-15</td>
<td>LH521028U-20</td>
</tr>
<tr>
<td></td>
<td>1Mb (x18) 9428</td>
<td>1Mb (x18) 9327</td>
<td>1Mb (x16) 9432</td>
<td>1Mb (x16) 9418</td>
<td>1Mb (x16) 9329</td>
</tr>
</tbody>
</table>

| | | | | | (see 1994 report) |

<table>
<thead>
<tr>
<th>Final passivation</th>
<th>Nitride on glass</th>
<th>Nitride</th>
<th>Nitride on glass</th>
<th>Nitride on glass</th>
<th>Nitride on glass</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal 2</td>
<td>Molybdenum</td>
<td>Titanium-nitride</td>
<td>Molybdenum</td>
<td>Titanium-nitride</td>
<td>Aluminum</td>
</tr>
<tr>
<td></td>
<td>Aluminum</td>
<td>Aluminum</td>
<td>Aluminum</td>
<td>Titanium-nitride</td>
<td>Titanium-nitride</td>
</tr>
<tr>
<td></td>
<td>Molybdenum</td>
<td>Titanium-nitride</td>
<td>Aluminum</td>
<td>Titanium-nitride</td>
<td>Titanium-tungsten</td>
</tr>
<tr>
<td>Metal 1</td>
<td>Same as M2</td>
<td>Same at M2</td>
<td>Aluminum</td>
<td>Titanium-nitride</td>
<td>Same as M2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Titanium</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Plugs</td>
<td>NA</td>
<td>NA</td>
<td>Tungsten</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Intermetal dielectric</td>
<td>Glass</td>
<td>Glass</td>
<td>Glass</td>
<td>Glass</td>
<td>Glass</td>
</tr>
<tr>
<td>Reflow glass</td>
<td>BPSG</td>
<td>BPSG</td>
<td>BPSG</td>
<td>BPSG</td>
<td>BPSG</td>
</tr>
<tr>
<td>Polycide metal</td>
<td>Tungsten</td>
<td>Tungsten</td>
<td>None</td>
<td>Tungsten</td>
<td>Tungsten</td>
</tr>
</tbody>
</table>

**TABLE 2 - 3**
TECHNOLOGY DESCRIPTION

HITACHI HM621864HJP-20
1 Mbit (64K x 18) CMOS SRAM

Introduction

These parts were packaged in 44-pin, Small Outline J-lead (SOJ) packages using an LOCCB internal design. Parts were date coded week 28 of 1994, and all were fully functional production parts. Memory organization was 64K words x 18 bits. They operate from a standard 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

- Molybdenum cap and barrier layers.

Quality

Quality of process implementation was only fair primarily due to large silicon nodules in the metallization and problems in covering vertical steps with metal at vias (M2 to M1).

In the area of layer patterning, etch definition and control (depth) were both good.

Alignment/registration was good.

Packaging/assembly quality using the Lead-On-Chip Center Bond (LOCCB) package was also good.

Technology

Devices were made by a twin (multiple)-well CMOS process employing an N substrate. No epi was detected. Two levels of metal, and two levels of polysilicon one of which (poly 1) was a tungsten polycide, were used. A normal recessed-oxide isolation was employed and no significant attempt was made to shorten the birdsbeak. Redundancy fuses were present.
Both metal 1 and metal 2 consisted of aluminum with molybdenum caps and barriers. As mentioned, the silicon doping of the aluminum left large silicon nodules reducing effective metal cross section.

Standard vias and contacts were used, no plugs and no reflowed aluminum.

Planarization of the intermetal dielectric was by deposited glass layers including a spin-on-glass (SOG). No planarizing etch was used. The dielectric under metal 1 was planarized by a reflow process. There was no evidence whatsoever of a chemical-mechanical planarization (CMP) process.

All gates were made with polycide (poly 1) and all used oxide sidewall spacers that were left in place. Polycide was also used for the fuses (redundancy elements). No silicide metallization treatment (salicide process) was present on the diffusions.

Direct (buried) contacts between polycide and diffusion were only used in the memory array.

Minimum feature measured anywhere on these dice was the 0.55 micron poly 2 width.

Minimum physical gate lengths measured were 0.7 micron for both N-channel and P-channel.

Memory Cell Structure

A standard four transistor, two resistor NMOS SRAM cell was employed. Metal 2 provided bit lines and used metal 1 links to the N+ sources of the select gates. Metal 1 provided direct ground connections to the sources of each group of 4 storage flip-flop gates, and piggyback Vcc connections to the poly 2 Vcc lines.

Poly 1 (polycide) used for gates made use of direct (buried) contacts to both the N+ drain of the select gates and to the poly 2 pullup resistors. These resistors were normal, that is, selectively doped to provide both Vcc distribution and resistive links.

Cell size was a rather large 30 microns².
Packaging/Assembly

The packages used were 44 pin plastic SOJ types but internally used the LOCCB design. Power pins were present on both sides (at center). All pins were connected. Internally the iron-nickel leadframe was spot-plated with silver and externally pins were plated with lead-tin solder. Die attach was by a doublebacked adhesive Kapton-type tape. Standard thermosonic wirebonds using gold wire were used.

A thin polyimide type die coat, patterned to clear bond pads, was present to protect against alpha particle induced leakage and packaging stresses.
The Hitachi HM621864HJP-20 SRAM circuit die. Mag. 16x.
Hitachi HM621864HJP-20. SEM views of device structures.
Hitachi HM621864HJP-20. SEM views of the SRAM array.

Mag. 6000x, 60°

Mag. 5000x, 0°

section, Mag. 12,000x
TECHNOLOGY DESCRIPTION

NEC μPD431018LE-15
1 Mbit (64K x 18) CMOS SRAM

Introduction

Ref. report SCA 9412-381

These parts were packaged in standard 44-pin, plastic Small Outline J-lead (SOJ) packages. Parts were date coded week 27 of 1993. They were fully functional production samples. Memory organization was 64K words x 18 bits and devices operate from a standard 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

- Thin-Film-Transistor (TFT) load devices in the memory cells.

Quality

Quality of process implementation was normal although metal 1 thinning at bit line contacts was significant.

In the area of layer patterning, etch definition of all layers was good. Etch control was normal with some minor overetch present.

Alignment/registration was good.

Packaging/assembly quality was good as well. The packages used were standard, not the LOCCB type.

Technology

Devices were made by a twin (multiple)-well CMOS process employing an N substrate and no epi. Two levels of metal, two levels of polycide (tungsten on polysilicon), plus two levels of
polysilicon were used. The memory cells used TFT pull-up devices. A normal recessed-oxide isolation was used. No evidence of attempts to significantly shorten the birdsbeak area was found.

Both metal levels consisted of aluminum with titanium-nitride caps and titanium-nitride on titanium barriers.

No plugs were used at any interconnect. Standard via contacts connected metal 2 to metal 1. Metal 1 to silicon contacts were also standard. Polycide 2 which was used as a metal substitute in the array only made direct (buried) contacts to N+ diffusion.

Planarization of the intermetal dielectric was by deposited glass layers including a Spin-On-Glass (SOG), coupled with etchback techniques. The dielectric under metal 1 was planarized by a reflow process. No evidence of chemical-mechanical planarization (CMP) was found.

All gates were made with poly 1 (polycide) including the gates in the cell array. As mentioned, four poly levels (including two polycides) were used and of special note here is that contacts existed between almost every level. For example, N+ was contacted directly by poly 1 and poly 2 (polycide). Poly 3 made direct contact to poly 1 and was in turn contacted directly by poly 4. Metal 1 connected to N+, P+, poly 1, poly 2 and poly 4.

Oxide sidewall spacers were used on all the gates and were left in place. No silicide metallization treatment (salicide process) was employed on diffusions.

No evidence of special dielectric or gate oxide materials was detected.

The devices use multiple wells including N-wells of different depth and P-wells inside deep N-wells. The P-well in N-well structure appeared to be used primarily in the array. Source/drain diffusions appeared to be of the double-diffused LDD type.

Minimum features measured anywhere on these dice were the 0.4 micron poly 4 and poly 1 widths.

Minimum physical gate lengths measured were 0.4 micron for N-channel and 0.6 micron for P-channel.
Memory Cell Structure

The most unique feature of this product was the use of the TFT pull-up devices in the memory cells. So far, we have only seen these used on two manufacturer's products; NEC and Hitachi.

These devices consisted of PMOS transistors made in the poly 4 lines located directly above their poly 3 gate electrodes. They are intended to improve performance at low level supply voltages (e.g., 2V), and were implemented above the standard SRAM cell elements so that no additional die area was consumed. The structure appeared to be the same as that used by NEC for their 4 Mb SRAMs (see 1994 report).

This is a very complex structured cell array area especially since there are so many interconnects between the various levels.

Poly 1 (polycide) as mentioned was used for the gates (and word lines), and poly 2 (polycide) was simply a metal substitute to provide ground connections. Bit connections were made by metal 1. Poly 4 distributed Vcc.

Cell size was 18 microns² which is the same as the cell used in the 4 Mb device.

Packaging/Assembly

The packages used were the standard 400 mil wide, 44-pin, plastic SOJ types. This is unlike the 4 Mb part we analyzed. It used an LOCCB package. Dual power pins were located at the center on each side of the package. The header/paddle was directly connected to pin 34 and is used to provide GND connections to both ends of the die by wirebonds.

The copper leadframe was spot-plated with silver internally, while externally leads were plated with lead-tin solder.

Die attach was by silver-filled epoxy and standard thermosonically bonded gold wire ball and stitch bonds were used.

A thin, patterned (to clear bond pads) polyimide die coat was present to protect against alpha particle induced leakage and packaging stresses.
Portion of the NECμPD431018 SRAM. Mag. 25x.
Remaining portion of the NECμPD431018 SRAM. Mag. 25x.
NECμPD431018. SEM views of SRAM cells.

Mag. 7400x, 60°

Mag. 9200x, 0°

Mag. 20,000x
TECHNOLOGY DESCRIPTION

MICRON MT5C64K16A1DJ-12
1 Mbit (64K x 16) CMOS SRAM

Introduction

Ref. report SCA 9412-394

These parts were packaged in 44-pin, plastic, Small Outline J-lead (SOJ) packages. Parts were date coded week 32 of 1994, and all were fully functional production parts. Memory organization was 64K words x 16 bits. They operate from a standard 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

- Chemical-mechanical planarization (CMP).

- Dual sidewall spacers on some gates.

- Isolated sidewall spacers left in place (standard Micron feature).

Quality

Quality of process implementation was good. No items of concern were found.

In the area of layer patterning, etch definition of all layers was very good, and control (depth) was good, showing only minor overetch at contact cuts.

Alignment/registration was good.

Packaging/assembly quality was also good.
Technology

Devices were made by a twin (multiple)-well CMOS process employing a P substrate. No epi was detected. Two levels of metal, and two levels of polysilicon (no polycide) were used. A normal recessed-oxide isolation was used with no significant attempt to shorten the birdsbeak.

Both metal 1 and metal 2 consisted of aluminum. Metal 2 had a titanium-nitride cap and no detectable barrier/adhesion layer. Metal 1 used a titanium barrier/adhesion layer and had no detectable cap.

Standard M2 to M1 via connections were used but M1 to silicon contacts made use of tungsten plugs (on pads of poly 2 at bit line contacts).

Two types of planarization were employed on these devices. The intermetal dielectric was planarized by multiple glass depositions and a planarizing etch. No use of a spin-on glass (SOG) was indicated. Planarization of the intermediate oxide (under metal 1) used the chemical-mechanical planarization (CMP) method. It was probably done before plug formation, but plug height was controlled very well. If it seems odd that two different methods were used, please remember that on most parts using CMP, the dielectric under the topmost metal layer is not planarized by CMP.

All gates were made with poly 1 and all used oxide sidewall spacers that were left in place on N-channel devices, but removed on P-channel gates. In fact, the N-channel gates used double sidewall spacers. Also, following the standard Micron process procedure, free standing isolated sidewall spacers remain in areas where P+ diffusion runs (like guardbands) exist. No silicide metallization treatment (salicide process) was used on the diffusions.

Direct (buried) contacts between poly and diffusion were only used in the memory cells.

Minimum feature measured anywhere on the dice was the 0.55 micron polycide width.

Minimum physical gate lengths measured were 0.55 micron for both N-channel and P-channel.
Memory Cell Structure

A standard four transistor, two resistor NMOS SRAM cell was used. Metal 2 was used for piggyback word lines and employed metal 1 links to the poly word lines/select gates. Metal 1 provided the bit lines. Vcc was distributed by poly 2 and N+ diffusion provided the ground connection.

Poly 1 used for gates made direct (buried) contacts to both the N+ drain of the select gates and to the poly 2 pullup resistors. These resistors were normal, that is, selectively doped to provide both Vcc distribution and resistive elements.

Cell size was a rather large 32 microns².

Packaging/Assembly

The packages used were 44 pin plastic SOJs. Power pins were present on both sides (at center). Pins 22 and 23 were not connected. Internally the copper leadframe was spot-plated with silver and externally pins were plated with lead-tin solder. Die attach was by silver-epoxy and standard thermosonic wirebonds using gold wire were used.

A thin polyimide type die coat, patterned to clear bond pads, was present to protect against alpha particle induced leakage and packaging stresses.
Portion of the Micron Semiconductor MT5C64K16A1 SRAM. Mag. 26x.
Remaining portion of the Micron Semiconductor MT5C64K16A1 SRAM. Mag. 26x.
Micron Semiconductor MT5C64K16A1. SEM views of device structures.
TECHNOLOGY DESCRIPTION

SAMSUNG KM6161002J-15
1 Mbit (64K x 16) CMOS SRAM

Introduction

Ref. report SCA 9412-392

These parts were packaged in 44-pin, plastic, Small Outline J-lead (SOJ) packages. Parts were date coded week 18 of 1994, and all were fully functional production parts. Memory organization was 64K words x 16 bits. They operate from a standard 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

- Smallest 1 Mb SRAM die analyzed to date.

- Fairly standard process.

Quality

Quality of process implementation was fair. Some fairly large silicon nodules were present in the metal and metal thinning was greater than desirable, but neither condition was serious.

In the area of layer patterning, etch definition of all layers was good. Control (depth) showed minor overetch at metal contact cuts, but even this minimum overetch is of some concern as it equals the barrier thickness and thus creates some danger of causing cracks at contact periphery in this layer.

Alignment/registration was good.

Packaging/assembly quality was normal.
Technology

Devices were made by a twin (multiple)-well CMOS process employing a P substrate. No epi was detected. Two levels of metal, and three levels of polysilicon two of which (poly 1 and 3) were tungsten polycides, were used. A normal recessed-oxide isolation was used with no apparent attempt to shorten the birdsbeak.

Both metal 1 and metal 2 consisted of aluminum with titanium-nitride caps. In addition, metal 1 used a titanium-nitride barrier on a thin titanium adhesion layer. Polycide 3 was used as a metal substitute in the cell array.

No plugs were used at vias or contacts and no aluminum reflow was present either. Samsung has used aluminum reflow at contacts on some products in the past. In this case, only standard contact and via connections were employed.

Planarization of the intermetal dielectric was by deposited glass layers and planarizing etch. A Spin-On-Glass (SOG) was not used and no evidence of CMP (chemical-mechanical planarization) was present. The dielectric under metal 1 was planarized by a reflow process as was the dielectric under polycide 3.

All gates were made with polycide 1 and all used oxide sidewall spacers that were left in place. No silicide metallization treatment (salicide process) was used on the diffusions.

Direct (buried) contacts were employed between polycide 3 and poly 2 and diffusions, and between poly 2 and polycide 1 and diffusions. All of these were used in the memory cell array.

Minimum feature measured anywhere on these dice was the 0.45 micron polycide 1 width.

Minimum physical gate lengths measured were 0.45 micron for N-channel and 0.5 micron for P-channel.

Memory Cell Structure

A four transistor, two resistor NMOS SRAM cell was used. Metal 1 was used for bit lines and employed polycide 3 links to the N+ sources of the select gates. Polycide 3 provided direct ground connections to the source of each storage flip-flop gate pair and was used to make buried/interpoly
contacts for cross-coupling. Selectively doped poly 2 distributed Vcc and provided the pull-up resistors.

Polycide 1 was used for all gates and employed direct (buried) contacts to both the N+ drain of the select gates and to the poly 2 pullup resistors.

Cell size was 22 microns$^2$.

**Packaging/Assembly**

The packages used were 44 pin plastic SOJ types. Power pins were present on both sides. Internally the iron-nickel leadframe was spot-plated with silver and externally pins were plated with lead-tin solder. Die attach was by silver-epoxy and standard thermosonic wirebonds using gold wire were used.

No evidence of a die coat was found.
Portion of the Samsung KM6161002 SRAM. Mag. 25x.
Remaining portion of the Samsung KM6161002 SRAM. Mag. 25x.
Samsung KM6161002. SEM views of device structures.

section,
Mag. 14,000x

Mag. 5200x, 0°

Mag. 8400x