This report is organized into sections by **product types**.

In all cases an initial overview of each section is followed by summary tables comparing design rule dimensions, layer thicknesses, and materials used. In a few cases, data reported in a previous year is included to allow comparison or provide background.

This is then followed by a highly concentrated technology discussion of each product included, and example figures illustrating the features of the technology. *(Full reports covering each individual product are available separately).*

The discussions have been organized to be as concise and similar to each other as possible in order to facilitate ease of comparison. Careful reading will demonstrate that very detailed information is in fact provided.

In almost all cases no information about the technology was provided by the manufacturer and all information reflects our interpretation of analysis results. No electrical testing of the circuits was done by ICE so functionality and speeds are as reported by our clients or in product literature.

All analysis was done at ICE’s own laboratories during 1995 or early 1996 (although a few parts were date coded 1994).
OVERVIEW OF TECHNOLOGY STATUS

JANUARY 1996

It needs to be pointed out at the start that our comments below are based on technology we’ve actually seen appearing in real products, not the public announcements or discoveries that receive the bulk of the publicity in the press.

The best illustration of this may again be in the area of DRAMs where it seems we’ve been deluged with announcements and advertisements for 64 Mbit devices for over three years — and in fact performed our first analysis on two types two years ago — but have seen nothing since until now. It was therefore very interesting to finally see the new Samsung 160 mm² die version of this product, date coded week 52 of 1995, and compare it to the Hitachi part dated coded week 51 of 1993, almost exactly two years previous. Design rules were not improved although cell and die size were. We thus draw the conclusion that although manufacturers of these product types have undoubtedly not been totally inactive, the priorities were obviously affected very significantly by the terrific markets for 16 Mbit parts and below.

In fact, this lethargy in bringing larger capacity more advanced technology versions of memory devices into full production seems to have included the entire memory business.

For example, the first 4 Mb SRAM we analyzed was done in 1992, on a part date coded week 51 of 1991, over four years ago(!), and it had a die size smaller than the Toshiba part included here (date coded week 9 of 1995)!

Somewhat similar comments can be made about EPROM.

Obviously, there seems to have been much more emphasis on functional adaptations (wide organizations) than in technology advancements.

This is entirely opposite to what has happened in the microprocessor arena where Intel alone has made more process technology advancements than the entire memory industry in the last year or two! In fact, from the first Pentium class device analyzed in 1993 (date code 9328) to
the 120 MHz/133 MHz devices analyzed in 1995 (presumably fabbed in mid-1995) these products have evolved from a really primitive example of process technology to a technological prowess that is the equivalent of the best we’ve seen. It clearly demonstrates that the wake-up call issued by IBM has been heard at Intel and may have resulted in waking up the giant, so to speak.

Not that the other manufacturers in this business segment have been sitting idly by. IBM has made significant strides as well and Motorola is not far behind.

In contrast, non-U.S. manufacturers offering products in the microprocessor area have shown no evidence whatsoever in seriously addressing these changes in process technology, and we include the Hitachi SH2 as an example of this. NEC has been the most aggressive in the past, but we’ve seen no recent examples of their capability.
## TABLE OF MOST AGGRESSIVE FEATURE SIZES

The following table shows the most aggressive features ICE observed in 1995.

<table>
<thead>
<tr>
<th>FEATURE SIZES</th>
<th>PRODUCT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Largest die</td>
<td>190mm²</td>
</tr>
<tr>
<td>Min metal 6 width</td>
<td>7.0µm</td>
</tr>
<tr>
<td>Min metal 6 space</td>
<td>2.5µm</td>
</tr>
<tr>
<td>Min metal 5 width</td>
<td>0.9µm</td>
</tr>
<tr>
<td>Min metal 5 space</td>
<td>0.8µm</td>
</tr>
<tr>
<td>Min metal 4 width</td>
<td>0.9µm</td>
</tr>
<tr>
<td>Min metal 4 space</td>
<td>0.9µm</td>
</tr>
<tr>
<td>Min metal 3 width</td>
<td>0.7µm</td>
</tr>
<tr>
<td>Min metal 3 space</td>
<td>0.5µm</td>
</tr>
<tr>
<td>Min metal 2 width</td>
<td>0.45µm</td>
</tr>
<tr>
<td>Min metal 2 space</td>
<td>0.5µm</td>
</tr>
<tr>
<td>Min metal 1 width</td>
<td>0.3µm</td>
</tr>
<tr>
<td>Min metal 1 space</td>
<td>0.4µm</td>
</tr>
<tr>
<td>Min poly width (not as gate)</td>
<td>0.2µm</td>
</tr>
<tr>
<td>Min via (metal to metal)</td>
<td>0.6µm</td>
</tr>
<tr>
<td>Min contact (metal to silicon)</td>
<td>0.5µm</td>
</tr>
<tr>
<td>Min gate length N-channel/P-channel</td>
<td>0.25µm/0.25µm</td>
</tr>
<tr>
<td>Min DRAM cell size</td>
<td>1.2µm²</td>
</tr>
<tr>
<td>Min SRAM cell size</td>
<td>14.25µm²</td>
</tr>
<tr>
<td>Most levels of metal</td>
<td>6</td>
</tr>
<tr>
<td>Most levels of poly</td>
<td>5</td>
</tr>
<tr>
<td>Rated (ICE) most complex process</td>
<td></td>
</tr>
<tr>
<td>Rated (ICE) most advanced technology</td>
<td></td>
</tr>
</tbody>
</table>
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