PROGRAMABLE DEVICES

This is the broadest category of products we cover in one section from a technology as well as functionality standpoint.

Both Altera and Xilinx especially are aggressively improving their offerings so that Altera for example already uses three levels of metal and half micron gates. Based on recent reports and on what we’ve seen, these devices appear to be the most rapid in implementing the advanced process technologies embodied in microprocessors, as well as some of the special technologies such as antifuse.
## Horizontal Dimensions (Design Rules)

<table>
<thead>
<tr>
<th><strong>Programmable Devices</strong></th>
<th>XILINX</th>
<th>ALTERA</th>
<th>ALTERA</th>
<th>ACTEL</th>
<th>HITACHI</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>XC5210</td>
<td>EPF81500</td>
<td>EPM7256</td>
<td>A1460A</td>
<td>HG62G027</td>
</tr>
<tr>
<td></td>
<td>FPGA 9538</td>
<td>PLA 9537</td>
<td>EPLD 9519</td>
<td>FPGA 9441</td>
<td>ASIC 1995</td>
</tr>
</tbody>
</table>

| **Die size** | 8 x 8.9 mm (71 mm²) | 10 x 11.5 mm (115 mm²) | 9.1 x 10.1 mm (92 mm²) | 10.5 x 11 mm (115 mm²) | 6.6 x 6.6 mm (43.6 mm²) |
| Min M3 width/space | 0.9µm/0.9µm | 0.8µm/0.8µm | NA | NA | NA |
| Min M2 width/space | 0.8µm/1µm | 0.8µm/0.8µm | 1.0µm/1.0µm | 1.5µm/1.6µm | 1.9µm/1.2µm |
| Min M1 width/space | 0.7µm/0.9µm | 0.8µm/0.8µm | 0.6µm/1.0µm | 1.2µm/1.3µm | 1.8µm/1.2µm |
| Min via (Met. to Met.) | 1.0µm | 0.7µm | 1.4µm | 1.4µm | 1.0µm |
| Min cntct (Met. to Si) | 0.8µm | 0.6µm | 1.0µm | 1.1µm | 1.2µm |
| Min Poly 2 | NA | NA | NA | 0.75µm | NA |
| Min Poly 1 | 0.6µm* | 0.5µm* | 0.45µm* | 1.8µm | 0.7µm* |
| Min gate - (N)* | 0.6µm | 0.5µm | 0.45µm | 0.75µm | 0.7µm |
| Min gate - (P)* | 0.6µm | 0.5µm | 0.65µm | 0.85µm | 0.75µm |
| Cell pitch | NA | NA | 6 x 14.25µm | 3.4 x 4µm | 15 x 70µm |
| Cell area | NA | NA | 85µm² | 13.5µm² | 1050µm² |

*Polycide †Physical gate length ‡Plugs

**TABLE 4 - 1**
## VERTICAL DIMENSIONS

<table>
<thead>
<tr>
<th>PROGRAMMABLE DEVICES</th>
<th>XILINX</th>
<th>ALTERA</th>
<th>ALTERA</th>
<th>ACTEL</th>
<th>HITACHI</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>XCC5210</td>
<td>EPF81500</td>
<td>EPM7256</td>
<td>A1460A</td>
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<td>PLA</td>
<td>EPLD</td>
<td>FPGA</td>
<td>ASIC</td>
</tr>
<tr>
<td></td>
<td>9538</td>
<td>9537</td>
<td>9519</td>
<td>9441</td>
<td>1995</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>0.9µm</th>
<th>0.7µm</th>
<th>0.6µm</th>
<th>1.0µm</th>
<th>1.0µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final passivation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal 3</td>
<td>0.85µm</td>
<td>1.0µm</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Metal 2</td>
<td>0.55µm</td>
<td>0.6µm</td>
<td>1.15µm</td>
<td>1.1µm</td>
<td>1.1µm</td>
</tr>
<tr>
<td>Metal 1</td>
<td>0.65µm</td>
<td>0.6µm</td>
<td>0.8µm</td>
<td>0.75µm</td>
<td>0.75µm</td>
</tr>
<tr>
<td>Intermetal dielectric</td>
<td>0.7µm</td>
<td>0.5µm</td>
<td>0.8µm</td>
<td>0.5µm</td>
<td>0.8µm</td>
</tr>
<tr>
<td>Poly 2</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>0.3µm</td>
<td>NA</td>
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<tr>
<td>Poly 1</td>
<td>0.25µm*</td>
<td>0.25µm*</td>
<td>0.35µm*</td>
<td>0.3µm</td>
<td>0.3µm*</td>
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<tr>
<td>Recessed oxide</td>
<td>0.4µm</td>
<td>0.4µm</td>
<td>0.45µm</td>
<td>0.65µm</td>
<td>0.55µm</td>
</tr>
<tr>
<td>N-well</td>
<td>?Ο</td>
<td>1.5µm</td>
<td>3.5µm</td>
<td>4µm</td>
<td>?Ο</td>
</tr>
<tr>
<td>P-well</td>
<td>5µm</td>
<td>3µm</td>
<td>3µm</td>
<td>3.5µm</td>
<td>5µm</td>
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<tr>
<td>Epi</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>11µm (P)</td>
</tr>
</tbody>
</table>

*Polycide*  *Could not delineate*  

**TABLE 4 - 2**
### Die Materials

<table>
<thead>
<tr>
<th>PROGRAMMABLE DEVICES</th>
<th>XILINX</th>
<th>ALTERA</th>
<th>ALTERA</th>
<th>ACTEL</th>
<th>HITACHI</th>
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<td></td>
<td>FPGA</td>
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<tr>
<td></td>
<td>9538</td>
<td>9537</td>
<td>9519</td>
<td>9441</td>
<td>1995</td>
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</table>

<table>
<thead>
<tr>
<th></th>
<th>Nitride</th>
<th>Nitride on glass</th>
<th>Nitride</th>
<th>Nitride on glass</th>
<th>Nitride</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final passivation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal 3</td>
<td>Titanium-nitride</td>
<td>Titanium-nitride</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td>Aluminum</td>
<td>Aluminum</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Titanium-nitride</td>
<td>Titanium</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal 2</td>
<td>Same as M3</td>
<td>Same as M3</td>
<td>Aluminum</td>
<td>Titanium-tungsten</td>
<td>Titanium-tungsten</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal 1</td>
<td>Same as M3</td>
<td>Titanium-nitride</td>
<td>Same as M2</td>
<td>Titanium-nitride</td>
<td>Same as M2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Aluminum</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Titanium-tungsten</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Titanium-nitride</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intermetal dielectric</td>
<td>Glass w/SOG</td>
<td>Glass w/SOG</td>
<td>Glass w/SOG</td>
<td>Glass w/SOG</td>
<td>Glass w/SOG</td>
</tr>
<tr>
<td>Reflow glass</td>
<td>BPSG</td>
<td>BPSG</td>
<td>BPSG</td>
<td>BPSG</td>
<td>BPSG</td>
</tr>
<tr>
<td>Polycide metal</td>
<td>Tungsten</td>
<td>Tungsten</td>
<td>Tungsten</td>
<td>NA</td>
<td>Tungsten</td>
</tr>
</tbody>
</table>

**TABLE 4 - 3**
TECHNOLOGY DESCRIPTION

XILINX XC5210
LOGIC CELL ARRAY (FPGA)

Introduction

These parts were packaged in 160-pin, Plastic Quad Flat Packs (PQFPs), date coded week 38 of 1995. All parts were fully functional production samples. This architecture provides typically 10,000 plus useable gates. SRAM flip-flops provide programability. The devices operate from a standard 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

- No via or contact plugs despite use of three levels of metal and fairly aggressive design rules.

Quality

Quality of process implementation was normal. Metal thinning was significant in a few particular locations only.

In the area of layer patterning, both etch definition and control (depth) were normal.

Alignment/registration was also normal.
Technology

These devices were made by a twin-well CMOS process in an N substrate. No epi was used. Three levels of metal and one level of polycide were used. A normal recessed-oxide isolation was employed. No attempt to shorten the birdsbeak area was made.

A single thick layer of nitride was used for final passivation.

All three metal levels consisted of aluminum and were defined by standard dry etch techniques. All used titanium-nitride caps and barriers. No evidence of a separate adhesion layer was found.

No plugs were present at any vias or contacts. We consider this unusual in a three metal process, especially one employing design rules in the 0.6 - 0.7 micron range such as this. It necessitates special via/contact etching procedures to slope walls adequately for metal step coverage.

Planarization of the intermetal dielectric was by two deposited glass layers, SOG, and planarizing etch. The dielectric under metal 1 was planarized by a reflow process.

Polycide provided all gates on the die. All gates used oxide sidewall spacers that were left in place. Standard implanted source/drain diffusions were used. No fuses were found.

Gate oxide appeared to be normal grown oxide and no unusual dielectric layers were noted. Reflow glass was the normal BPSG type.

No buried contacts were used and no salicide source/drain treatment was present.

Overall minimum feature measured anywhere on these dice was the 0.6 micron polycide width, although metal 1 was also quite narrow, measuring 0.7 micron minimum width.
Minimum physical gate lengths measured were 0.6 micron for both N-channel and P-channel.

**Array Cell Structures**

These parts used SRAM flip-flops to program internal functions thus physical process structures are identical to the peripheral circuit areas.

**Packaging/Assembly**

As mentioned, devices were packaged in standard 160-pin, PQFPs with gull-wing leads. All pins were connected, but there were numerous bond pads that were not. Die attach was by a silver epoxy and standard thermosonic wirebonds using gold wire were used.

No special heatsink or other elements were used.

No evidence of a die coat was found.
Die photographs of the Xilinx FPGA. Mag. 20x.
SEM section views of general structure.
N-channel, Mag. 26,000x

P-channel, Mag. 26,000x

bond pad, Mag. 5700x

SEM section views of gates and bond pad edge.
TECHNOLOGY DESCRIPTION

ALTERA EPF81500ARC240-4
PROGRAMABLE LOGIC ARRAY (PLA)

Introduction

These parts were packaged in 240-pin, Plastic Quad Flat Packs (PQFPs), incorporating a large heatsink. They were date coded week 37 of 1995. All parts were fully functional production samples. This architecture provides 15,500 useable (31,000 available) gates and incorporates JTAG boundary scan test circuitry. The devices operate from a standard 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

- Three metal single poly technology (plugs at contacts — not at vias).

Quality

Quality of process implementation was normal to poor, the problems consisting of overetch at vias causing severe metal thinning at steps.

In the area of layer patterning, etch definition was good, but control (depth) was poor.

Alignment/registration was good.
Technology

These devices were made by a twin-well CMOS process on an N substrate. Three levels of metal and one level of polycide were used. A normal recessed-oxide isolation was employed. No attempt to shorten the birdsbeak area was made. Basic array cells called “Logic Elements” consist of relatively complex circuits, but since flip-flops provide the programability the technology is the same.

All three metal levels consisted of aluminum and were defined by standard dry etch techniques. All three levels used titanium-nitride caps. M3 and M2 employed thick titanium barriers/adhesion layers while M1 used a titanium-nitride barrier on a thin titanium adhesion layer.

No plugs were present at vias, but were employed at all contacts to silicon. The standard vias between M3 and M2 and between M2 and M1 were slope-etched to aid step coverage and in fact the thick titanium did cover these steps well but the aluminum did not. Height of the tungsten plugs used at contacts between M1 and silicon was well controlled. Plugs had the same titanium-nitride barrier on titanium adhesion layer present under metal 1.

Planarization of the intermetal dielectrics was by two deposited glass layers separated by an SOG. A planarizing etch was done to aid planarization. The dielectric under metal 1 was planarized by a standard reflow process.

Polycide provided all gates on the die. All gates used oxide sidewall spacers that were left in place. Standard implanted N+ and P+ source/drain diffusions were used. Polycide also provided the fuse elements present.

No buried contacts were used and no salicide source/drain treatment was employed.

Standard grown gate oxide was employed and there was no evidence of any nitride or other unusual dielectrics.
Overall minimum feature measured anywhere on these dice was the 0.5 micron polycide width.

Minimum physical gate lengths measured were 0.5 micron for both N-channel and P-channel.

**Array Cell Structures**

These parts use SRAM flip-flops to program Logic Element functions thus physical structures in the array are identical to the peripheral circuits.

**Packaging/Assembly**

As mentioned, devices were packaged in 240-pin, PQFPs, incorporating a large copper heatsink. A number of pins were not connected. Die attach was by a silver epoxy and standard thermosonic wirebonds using gold wire were used. The dice were mounted directly on the heatsink.

No evidence of a die coat was found.
Photograph of the Altera PLA. Mag. 16x.
SEM section views illustrating general device structure. Mag. 13,000x.
TECHNOLOGY DESCRIPTION

ALTERA EPM7256EQC160-20
EPLD

Introduction

Ref. report SCA 9512-443

These parts were packaged in 160-pin, Plastic Quad Flat Packs (PQFPs), date coded week 19 of 1995. All parts were fully functional production samples. This design provides 5,000 useable gates and represent the second generation “MAX” architecture. The devices operate from a standard 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

- Multiple thin oxides and an implant under poly.

Quality

Quality of process implementation was normal except for microcracks in the titanium-tungsten barrier metal around the bottom perimeter of the contacts.

In the area of layer patterning, etch definition was good, but control (depth) was poor at contacts, causing the microcracks.

Alignment/registration was good.
Technology

These devices were made by a twin-well CMOS process on a P substrate. Two levels of metal and one level of polysilicon (polycide) were used. A normal recessed-oxide isolation was employed. No attempt to shorten the birdsbeak area was made. The cell array used thin tunnel oxide windows for programming.

Passivation was a single level of silicon-nitride but extra care had been taken to provide stress relief. It included M2 to M1 via arrays at the die corners, and metal bus lines that were slotted and angled at die corners.

Both metal levels consisted of aluminum and were defined by standard dry etch techniques. Both also used no cap layer but did have a thick layer of titanium-tungsten barrier as an adhesion/barrier layer.

No plugs were used at vias or contacts.

Planarization of the intermetal dielectric was by at least three deposited glass layers (TEOS?) separated by two layers of spin-on-glass (SOG). The dielectric under metal 1 was planarized by a reflow process.

Tungsten-polycide provided all gates on the die including the array cells. All gates used oxide sidewall spacers that were left in place. Standard S/D implanted diffusions were employed throughout but a totally separate diffusion is used in the memory array under part of the polycide (see below).

All three thin gate/capacitor/tunnel dielectrics appeared to be normal grown oxides.

No salicide source/drain treatment was used and buried contacts were also not present.

Overall minimum feature measured anywhere on these dice was the 0.45 micron polycide width.
Minimum physical gate lengths measured were 0.45 micron for N-channel and 0.65 micron for P-channel.

**Array Cell Structures**

These parts use windows of ultra thin oxide for programming (EEPROM technique). Metal 2 was used to distribute word lines (via metal 1 links), while metal 1 provided bit, program, and enable lines. Polycide formed all gates.

Individual programable cell size was 6 x 14.25 microns (85 microns$^2$).

**Packaging/Assembly**

As mentioned, devices were packaged in standard 160-pin, PQFPs with gull-wing leads. All pins were connected. Die attach was by a silver epoxy and standard thermosonic wirebonds using gold wire were used.

No special heatsink or other elements were employed.

No evidence of a die coat was found.
Whole die photograph of the Altera EPLD. Mag. 20x.
SEM view of EEPROM cells along with the cell schematic.
SEM section view of an EEPROM cell (X-direction). Mag. 12,000x.
TECHNOLOGY DESCRIPTION

ACTEL A1460
FPGA (Antifuse)

Introduction

Ref. report SCA 9504-402

These parts were packaged in 208-pin, Plastic Quad Flat Packs (PQFPs), date coded week 41 of 1994. All parts were fully functional production samples. This architecture provides 8,000 equivalent gate array gates or 20,000 PLD equivalent gates. The devices operate from a standard 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

- Antifuse structure.

Quality

Quality of process implementation was normal to poor due to metal 1 integrity at contacts.

In the area of layer patterning, both etch definition and control (depth) were normal.

Alignment/registration was also normal.
Technology

These devices were made by a twin-well CMOS process in a P-epi on a P substrate. Two levels of metal and two levels of polysilicon were used. A normal recessed-oxide isolation was employed. No attempt to shorten the birdsbeak area was made. The cell array used poly 1 over diffusion with ultra thin oxide windows for programming.

A thick layer of nitride over a layer of glass provided the final passivation.

Both metal levels consisted of aluminum and were defined by standard dry etch techniques. Metal 2 used no cap but did have a layer of titanium underneath as an adhesion/barrier layer. Metal 1 used a titanium-nitride cap and barrier and a very thin titanium adhesion layer.

No plugs were present at vias or contacts and no polycide or salicide source/drain treatment was used.

No buried contacts were used. Metal 2 contacted metal 1, and metal 1 contacted diffusions and poly.

Planarization of the intermetal dielectric was by two deposited glass layers, a minor planarizing etch, and a substantial layer of spin-on-glass (SOG) on top. The dielectric under metal 1 was planarized by a reflow process.

Poly 2 (not a polycide) provided all gates on the die while poly 1 was used exclusively for program elements. (Note: it was impossible to determine with absolute certainty which was poly 1 and which was poly 2). All gates used oxide sidewall spacers that were left in place. Standard implanted N+ and P+ source/drain diffusions were used. Another totally separate diffusion was used in the memory array (see below).
Both gate oxide and antifuse dielectric appeared to be normal grown oxides, but a thin layer of what appeared to be silicon nitride was present directly below the BPSG reflow glass (above poly 2). Since we found no cutouts that would indicate its use as a mask definition layer, we assume it is intended as a sealing layer, but we don’t know why.

Overall minimum feature measured anywhere on these dice was the 0.75 micron poly 2 width.

Minimum physical gate lengths measured were 0.75 micron for N-channel and 0.85 micron for P-channel.

**Array Cell Structures**

These parts used round windows of ultra thin, ruptureable oxide for programming. These windows were located between poly 1 and special N+ diffusion “program” lines in 8-bit groups between piggyback metal contacts. The array was in the form of an X-Y matrix. Cells are programmed by “zapping” the thin dielectric to establish a connection between the poly 1 line and the N+ diffusion line. Series resistance is kept low by strapping the N+ with piggyback metal 2 lines.

Individual cell size was 3.4 x 4 microns (13.5 microns²). Diameter of the antifuse window was measured to be approximately 1.0 micron.

**Packaging/Assembly**

As mentioned, devices were packaged in standard 208-pin, PQFPs. Not all pins were connected. Die attach was by a silver epoxy and standard thermosonic wirebonds using gold wire were used.

No special heatsink or other elements were used.

No evidence of a die coat was found.
The Actel FPGA intact circuit die. Mag. 15x.
SEM section views of general construction. Mag. 10,000x.
SEM views of the antifuse array.

Mag. 2500x, 60°

Mag. 3400x

Mag. 26,00x
TECHNOLOGY DESCRIPTION

HITACHI HG62G027
GATE ARRAY

Introduction

Ref. report SCA 9508-423

This part was packaged in a 168-pin, Plastic Quad Flat Pack (PQFP). The date code could not be determined, but was most probably early 1995. The part was a fully functional production device. This is a channelless design. The device operates from a standard 5V power source.

See tables for specific dimensions and materials identification and see figures for examples of physical structures.

Unusual/Unique Features

- Staggered wirebond pads on the die to allow large number of connections.

Quality

Quality of process implementation was normal to poor, as usual due to problems in covering vertical steps with the die metallization.

In the area of layer patterning, both etch definition and control (depth) were normal.

Alignment/registration was also normal.
Technology

These devices were made by a twin-well CMOS process on an N substrate. No epi was present. Two levels of metal and one level of polycide were used. A normal recessed-oxide isolation was employed, and birdsbeaks were relatively short.

Final passivation consisted of a thick layer of silicon-nitride that was not planarized.

Both levels of metal consisted of aluminum and were defined by standard dry etch techniques. Both levels of metal used titanium-tungsten cap and barrier layers. Vias and contacts were standard (no plugs).

No buried contacts were used and no salicide treatment of the diffusions was present. Planarization of the intermetal dielectric was by two deposited glass layers (TEOS?) separated by a spin-on-glass (SOG). No planarizing etch appeared to have been used. The dielectric under metal 1 was planarized by a normal reflow process.

Polycide provided all gates on the die and there was no observable difference between I/O buffer process structures and those in the array. All gates used oxide sidewall spacers that were left in place. Source/drain diffusions were of the standard implanted type. A normal recessed oxide was used for isolation. A step in this oxide indicated use of twin-wells.

Gate oxide appeared to be a normal grown oxide and no unusual dielectric layers were found. Reflow glass was also a normal BPSG.

Overall minimum feature measured anywhere on this dice was the 0.7 micron polycide width.

Minimum physical gate lengths measured were 0.7 micron for N-channel and 0.75 micron for P-channel.
Array Cell Structures

These parts used a standard channelless design with four gate electrodes in series over each diffusion area. Gates were accessible from either end. Resulting cell size was 70 x 15 microns (4 each N- and P-channel gates).

Packaging/Assembly

As mentioned, devices were packaged in 168-pin, Plastic Quad Flat Packs with gull-wing leads. Four large cutouts were present in the paddle. Ends of the leads at bonding areas were staggered to help accommodate the high density staggered bond pads on the die. Standard thermosonic wirebonding using gold wire was used.

No evidence of die coat was found.
The Hitachi Gate Array intact circuit die. Mag. 28x.
SEM section views of general construction.
Topological SEM views of polycide gates.

Mag. 1200x

N-channel, Mag. 40,000x

P-channel, Mag. 40,000x