3

Yield and Yield Management

3 Yield and Yield Management

Clearly line yield and defect density are two of the most closely guarded secrets in the semiconductor industry. Line yield refers to the number of good wafers produced without being scrapped, and in general, measures the effectiveness of material handling, process control, and labor. Die yield refers to the number of good dice that pass wafer probe testing from wafers that reach that part of the process. It is intended to prevent bad dice from being assembled into packages that are often extremely expensive and measures the effectiveness of process control, design margins, and particulate control. Figure 3-1 shows some typical numbers for a few product types normalized to twenty masking layers, similar feature and die sizes, and the Murphy defect density model.

Product	Metric	Best Score	Average Score	Worst Score
Memory	Line Yield	98.8	93.0	87.1
	Die Yield	93.6	77.4	52.8
CMOS Logic	Line Yield	97.2	89.8	77.8
	Die Yield	78.6	71.1	48.6
MSI	Line Yield	91.2	77.9	65.9
	Die Yield	56.7	49.5	43.1

*** 2Q mask layers, ~1m feature size, 0.5sq. cm**

Source: UC Berkeley Study 22793

Figure 3-1. Typical Line Yield and Die Yields (Normalized*)

Yield improvement is the most critical goal of all semiconductor operations as it reflects the amount of product that can be sold relative to the amount that is started. Yield is also the single most important factor in overall wafer processing costs. That is, incremental increases in yield (1 or 2 percent) significantly reduce manufacturing cost per wafer, or cost per square centimeter of silicon. In the fab, yield is closely tied to equipment performance (process capability), operator training, overall organizational effectiveness, and fab design and construction.

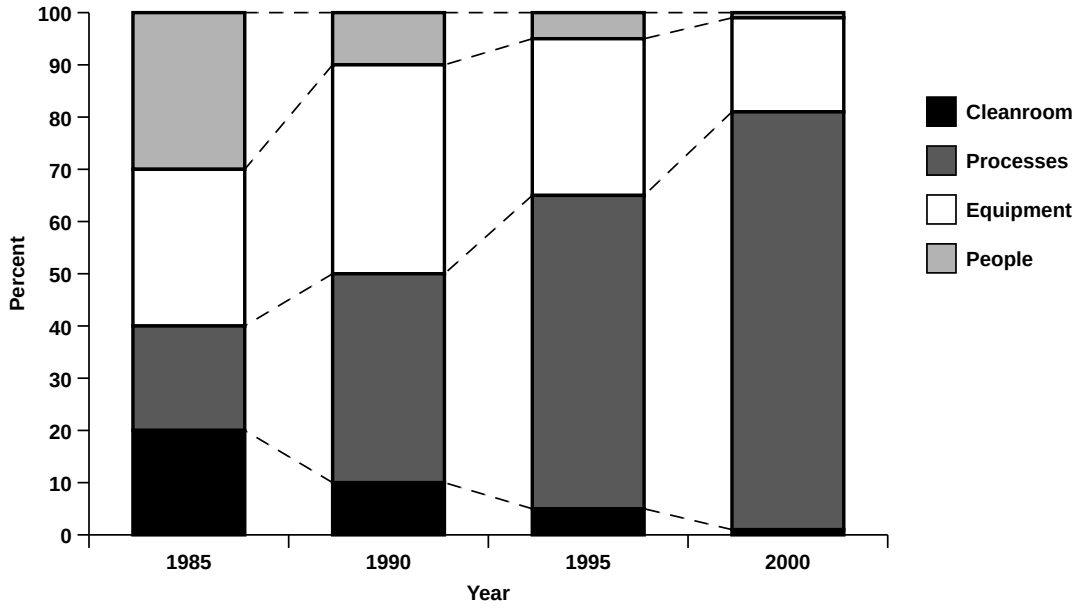
Continued device miniaturization in the semiconductor industry and the trend to larger and larger die sizes means that particulate contamination has an ever increasing impact on yields. Today, over 80 percent of yield loss of VLSI chips manufactured in volume can be attributed to random defects. The other main contributors to yield loss include design margin and process variation, followed by photolithography errors, and material (wafer) defects (Figure 3-2). The dramatic decline in the contribution of people to particulate problems in the fab can be attributed to better education and training, adherence to clean room disciplines, and less direct contact by the people due to more use of automation.

PROBE YIELD PROBLEM	YIELD LOSS (%)	PERCENT OF TOTAL PROBE YIELD LOSS
CONTAMINATION	40	80
DESIGN MARGIN	5	10
PROCESS VARIATION	3	6
PHOTOLITHOGRAPHY ERRORS	1	2
MATERIAL DEFECTS	1	2
TOTAL LOSS	50	100
PROBE YIELD (100% - DIE LOSS) = 50%		

Source: ICE 12056G

Figure 3-2. Typical 1996 Silicon Wafer IC Probe Yield Losses

Random defects can be traced back to the tools, the people, the processes, the process chemicals and gases, or the cleanroom itself. Over the years, cleanroom technology and the purification of process materials has been improved so dramatically that the majority of contamination in leading-edge fabs today is due to the processes and tools (Figure 3-3). However, for many existing fabs, cleanroom contamination remains a significant, yield-limiting factor.



Source: CleanRooms 19973A

Figure 3-3. Sources of Wafer-Level Contamination

Contamination control involves the control of particulates, transition metals, heavy metals, organics, and any other undesirable contaminants that result from IC processing. Figure 3-4 shows some of the critical parameters that drive IC complexity over time, including minimum device feature size, resist exposure wavelength, and maximum critical particle diameter also known as "killer defect" size. As shown, critical particle size is one-fifth the feature size at these small geometries. Figure 3-5 illustrates one of the problems that IC manufacturers face today. The category of Class one clean room is inadequate in monitoring particles for some of the future feature sizes due to the inaccuracies of measuring particles that small. This fact, along with the previously discussed sources of particles today, may lead to the more pervasive use of mini-environments and robots as an alternative to the classical clean room designs. This has some major implications on the cost of tomorrow's fabs. This will be addressed in a future section.

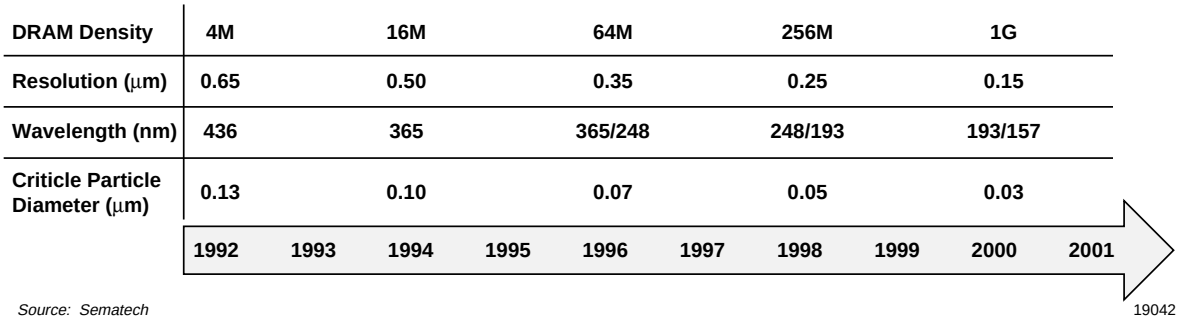


Figure 3-4. DRAM Evolution, Exposing Wavelength, and Critical Particle Diameter

Class Name		Class Limits							
		0.1μm		0.2μm		0.3μm		0.5μm	
		Volume units		Volume units		Volume units		Volume units	
SI	English*	(m^3)	(ft^3)	(m^3)	(ft^3)	(m^3)	(ft^3)	(m^3)	(ft^3)
M 1		350	9.91	75.7	2.14	30.9	0.875	10.0	0.283
M 1.5	1	1,240	35.0	265	7.50	106	3.00	35.3	1.00
M 2		3,500	99.1	757	21.4	309	8.75	100	2.83
M 2.5	10	12,400	350	2,650	75.0	1,060	30.0	353	10.0
M 3		35,000	991	7,570	214	3,090	87.5	1,000	28.3
M 3.5	100	—	—	26,500	750	10,600	300	3,530	100
M 4		—	—	75,700	2,140	30,900	875	10,000	283
M 4.5	1,000	—	—	—	—	—	—	35,300	1,000

*** For naming and describing the classes, SI names and units are preferred; however, English (U.S. customary) units may be used.**

Source: Institute of Environmental Sciences 21409

Figure 3-5. Airborne Particulate Cleanliness Classes (FED-STD-209E)

In terms of the other major forms of contamination, Figures 3-6 and 3-7[1] illustrate the types of contaminants that are common, along with some of the more popular cleaning techniques used to remove them, respectively.

Another concern for yield loss in the fab on many device structures is ESD (electrostatic discharge). Care must be exercised in the design and construction of the facility and equipment set to minimize the possibility of producing unwanted charges that can lead to device damage.

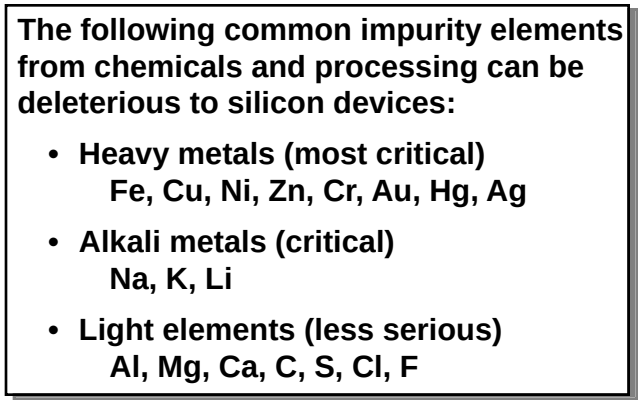


Figure 3-6. Impurity Elements Harmful to Silicon Wafers Processing

Solution	Chemical Symbols	Common Name	Purpose or Removal of:
Ammonium hydroxide/ hydrogen peroxide/ water	$NH_4OH/H_2O_2/H_2O$	RCA-1, SC-1 (Standard Clean-1), APM (ammonia/peroxide mix), Huang A	Light organics, particles, and metals; protective oxide regrowth
Hydrochloric acid/ hydrogen peroxide/ water	$HCl/H_2O_2/H_2O$	RCA-2, SC-2 (Standard Clean-2), HPM (hydrochloric/peroxide mix), Huang B	Heavy metals, alkalis, and metal hydroxides
Sulfuric acid/ hydrogen peroxide	H_2SO_4/H_2O_2	Piranha, SPM (sulfuric/ peroxide mix), "Caros acid"	Heavy organics
Hydrofluoric acid/water	HF/H_2O	HF, DHF (dilute HF)	Silicon oxide
Hydrofluoric acid/ ammonium fluoride/ water	$HF/NH_4F/H_2O$	BOE (buffered oxide etch), BHF (buffered hydrofluoric acid)	Silicon oxide
Nitric acid	HNO_3	—	Organics and heavy metals

Source: Handbook of Wafer Cleaning Technology 21666A

Figure 3-7. Partial List of Silicon Wafer Cleaning Solutions

Yield Modeling

Each semiconductor manufacturer has its own methods for modeling and predicting the yield of new products, estimating the yield of existing products, and verifying suspected causes of yield loss. A variety of yield models, including Murphy's, Poisson's, and Seeds' model, as well as the newer negative binomial model, can be used to estimate yield from defect density and die size. In comparison (Figure 3-8), each model has a different way of accounting for the distribution of defects on a wafer. The negative binomial model accounts for particle clustering on wafers. Unfortunately, this model is also one of the most difficult to use.

Oftentimes, several yield formulas are implemented within a particular company (e.g., Murphy's model for memory, Seed's model for gate arrays, etc.). Ultimately, each model's merit can only be judged by how it performs when compared to actual yields (i.e., there is no universal model).

For those other than the IC producers, either the standard Murphy model or Seeds model will generally suffice. A plot of the Murphy model (Figure 3-9) shows how a difference in defect density between 0.2 and 0.5 defects/cm^2, means the difference between a 68 percent probe yield and a 40 percent probe yield, respectively, for a 200mm^2 device. Yield is also strongly influenced by die size. Figure 3-10 simply illustrates the effect of die size on yield.

To compensate for shortening product lifecycles and drops in device ASP's as products mature, semiconductor manufacturers continually attempt to improve probe yields through the reduction in defect densities and shrinks of die sizes each generation by 20 percent or more. Recently, in response to the plummeting pricing of DRAMs, some manufacturers have transferred 64M cell designs to their 16M processes to enable smaller die sizes, higher yields, and reduced manufacturing costs. Importantly, however, this savings is partially off-set by the added complexity associated with manufacturing the 64M cell,

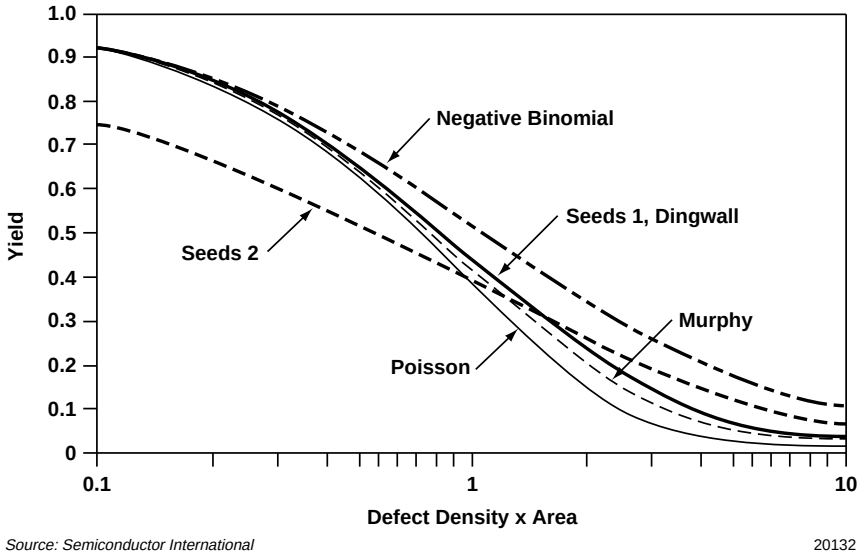


Figure 3-8. Comparing the Various Yield Models

which should increase the cost of manufacturing these smaller dice. This is graphically illustrated in Figure 3-11 which shows three generations of 4Mb DRAM designs. The number of chips per wafer increases dramatically through each generation.

Figure 3-12 shows ICE's estimates of 1996 defect densities as a function of device technology and feature size. For the most advanced fab facilities, defect densities range between 0.3 and 1.2 defects per square centimeter, whereas many of the older bipolar lines operate at defect densities as high as 3 defects per square centimeter. Figure 3-13 shows how the industry has decreased defect density as die sizes have increased. Essentially, in the manufacture of today's large leading-edge chips (0.35μm), less than 1.0 defect per square centimeter must be achieved in order to economically produce the devices.

Manufacturers are also improving methods for moving new processes from R&D to the production floor so that starting yields are higher, and ultimately, better yield can be accomplished. A recent study of 16 fabs in the U.S., U.K., Germany, Japan, and Taiwan by students at the University of California (Berkeley)[2], indicated that fabs starting at higher defect densities rarely achieve better yields than fabs starting at lower defect levels (Figures 3-14 and 3-15). Participants of the study included AMD, Cypress Semiconductor, Delco Electronics, DEC, Intel, IBM, ITT Intermetall, LSI Logic, NEC, Nihon Semiconductor, Oki, Silicon Systems, TSMC, Texas Instruments, and Toshiba.

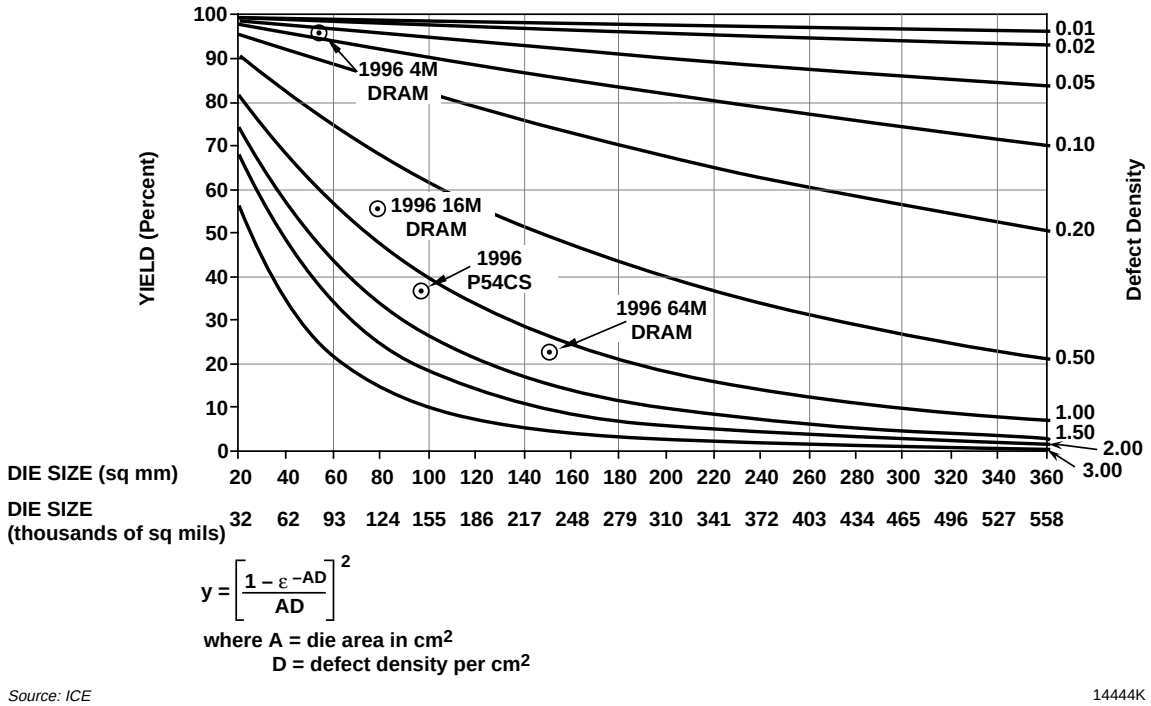


Figure 3-9. Murphy's Probe Yield Model (As a Function of Defects per sq. cm)

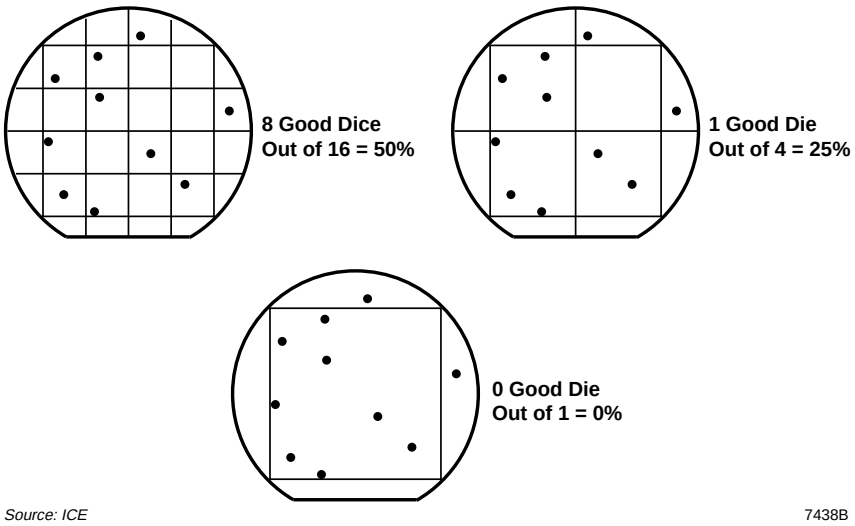


Figure 3-10. Effect of Die Size on Yield

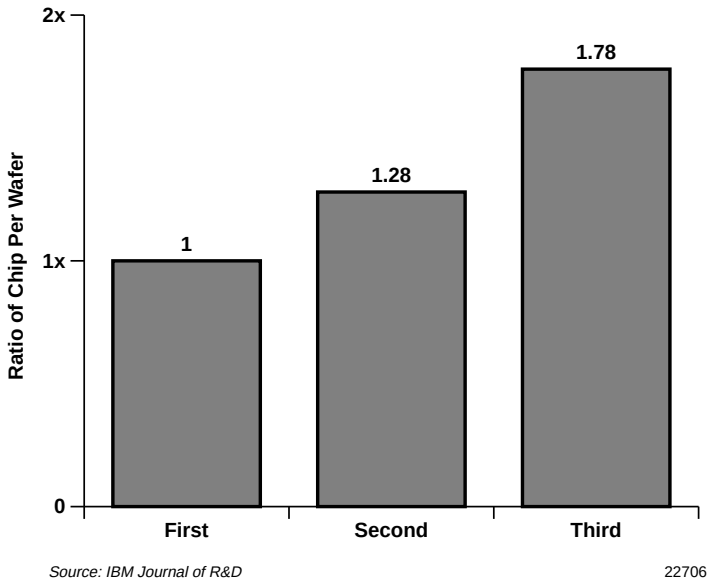
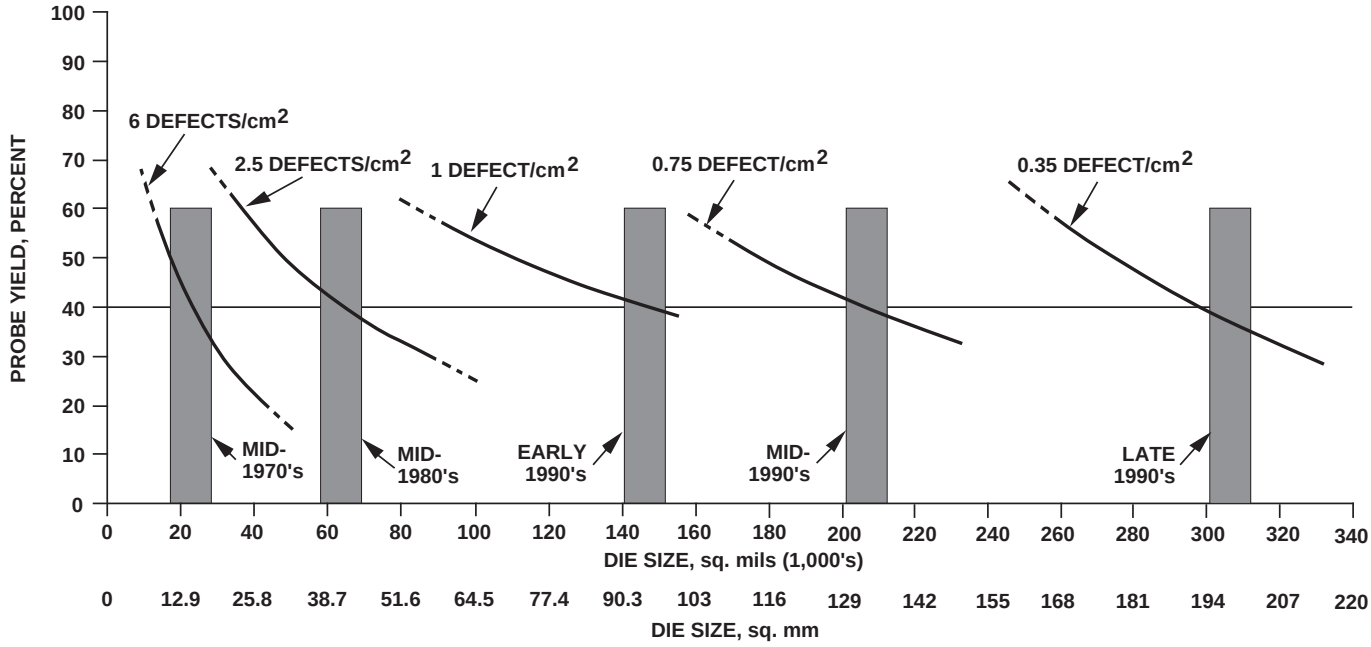


Figure 3-11. Chips-Per-Wafer Yield Improvement Across Three Generations of 4Mb DRAM

FEATURE SIZE (μ)	PROCESS TECHNOLOGY (DEFECTS/SQ CM)					
	CMOS 14-16 MASKS	ADVANCED CMOS 18-20 MASKS	ADVANCED BiCMOS 22 MASKS	BIPOLAR 8-10 MASKS	BIPOLAR 14-16 MASKS	ADVANCED BIPOLAR 22 MASKS
5.0	—	—	—	3	—	—
2.0	0.6	—	—	—	2.1	—
1.5	0.5	—	0.6	—	1.2	0.6
1.0	0.4	0.3	0.7	—	—	0.8
0.8	0.3	0.4	0.8	—	—	1.0
0.5	—	0.8	1.0	—	—	—
0.35	—	1.0	1.2	—	—	—

Source: ICE 14446H

Figure 3-12. Typical 1996 IC Process Defect Levels



Source: ICE 11227D

Figure 3-13. Die Size and Defect Density Trends

Figure 3-14. Defect Densities of 0.7-0.9µm Memory Flows

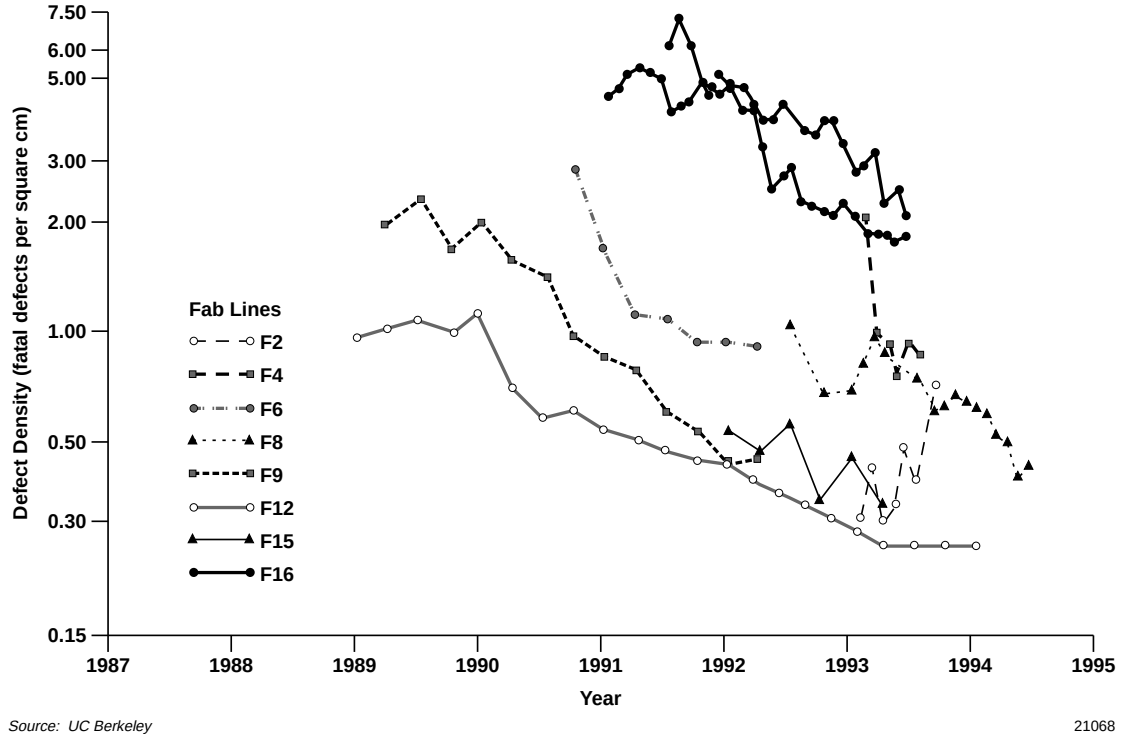


Figure 3-15. Defect Densities of 0.7-0.9µm Logic Flows

Tracking of Random Defects

Wafer fabs routinely track and report on defect density as a measure of manufacturing excellence. In many cases, however, the defect densities reported are simply calculations based on historical wafer probe yield information. While this may be an adequate starting point, the real challenge is to make improvements in these numbers as efficiently as possible. In order to accomplish this, the fab engineer needs to identify the specific process steps, pieces of equipment, input materials, etc. that are the major contributors to the defect density.

Many organizations are beginning to adopt a methodology called defect budgeting as a means to narrow down the search for sources of random defects in the process. The methodology involves the construction of a detailed process flow diagram for isolated segments of the process and the use of various problem solving tools to tie the total defects measured at the end of the process sequence to the likely sources in the process flow. An example of one of these diagrams is shown in Figure 3-16. The constituents that carry random defects into the process will vary widely according to the type of process being mapped. For example, for one process step there may be several different input materials to consider and no additional components, while others may be equipment intensive with very little in the way of defect contribution from input materials or components. All of these factors must be considered when constructing the map. These defect process maps are most effective when used for a small section of the total process flow. The areas to be investigated are established using Pareto diagrams of random defect occurrence.

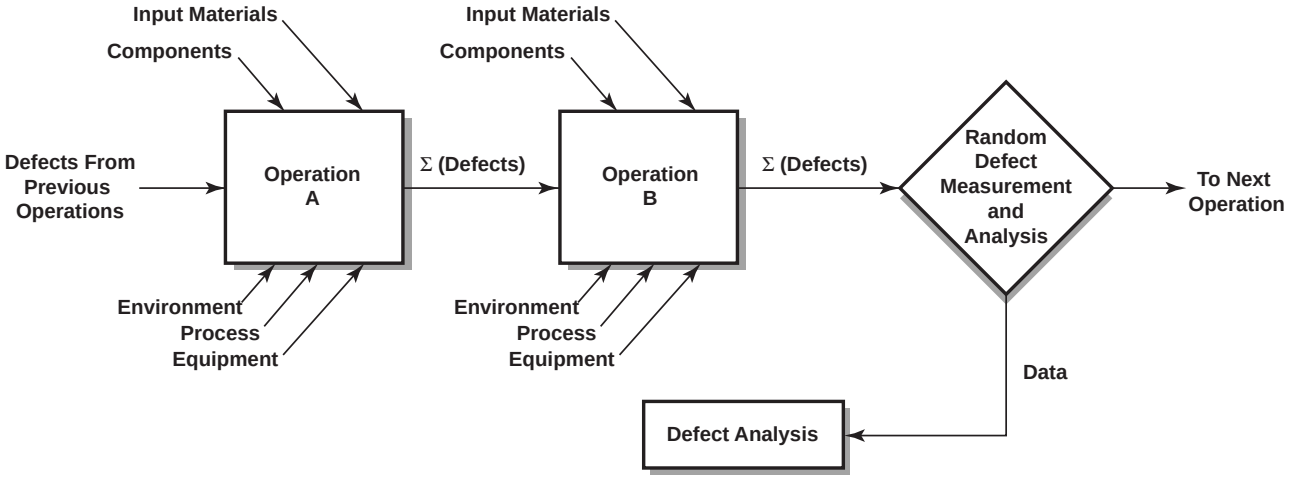


Figure 3-16. Defect Budget Process Map

Problem solving tools that are generally used during the process in addition to Pareto diagrams are Cause and Effect diagrams, and several methods of statistically designed experiments. Also necessary are published information by equipment suppliers, related technical publications, and sophisticated metrology tools designed to detect random defects. The trend is for these all to be combined into a systematic yield management system. These will be discussed in more depth later in this section.

Once this diagram is completed, priorities may be established to take action on major contributors to the defect rate in a more efficient manner. The continuous effort to reduce defect densities is critical to the fab for numerous reasons.

First, there is the issue of maintaining a competitive wafer cost. This will be illustrated in the section on benchmarking by looking at comparisons of defect density versus wafer and die cost.

Secondly, there is the need to prepare for the next generations of parts with higher device densities and probably larger wafers.

Third, there is the effect of defect densities on cycle time and product output. For any input wafer level capacity for the fab, the anticipated output and corresponding cycle time depend greatly on defect density. To estimate the effect on cycle time, making the assumption that a modern fab is basically rework free, the baseline cycle time must be multiplied by the reciprocal of the first time yield. The first time yield can then be expressed as a function of defect density by substituting one of the yield model formulas (Murphy, Seeds, etc.). Assuming an input limit of 20,000 wafers per month, the effective output capacity is drastically reduced as the defect density increases. A quick calculation shows that cycle time rapidly increases as defect densities increase since more time must be expended to satisfy any constant output requirement. This obviously can have a major impact on the total equipment set needs for the fab.

Metrology Tools: Tying Contamination to Yield

In the fab, patterned and unpatterned wafer inspection systems allow accurate identification of defects on wafers. However, these systems currently include no method for classifying the defects into "killer" and harmless defects. In addition, past interfaces between these inspection systems with probe yield and off-line metrology tools (i.e., SEMs, FIBs) was limited by the inability to manage the large volume of data created by these systems by fabs operating 24 hours a day, 7 days a week. However, sophisticated software tools are now making it feasible to build facility-wide information systems to collect, store, and analyze valuable yield management data from many sources in the fab and/or assembly operations.

The data required for yield management includes parametric test and functional probe from the test floor, process data from the fab equipment, in-line monitoring data from patterned wafer inspection systems, and work-in-process (WIP) data from the factory floor management system. Patterned wafer inspection systems, using both laser-based inspection systems (by Tencor and Inspex) as well as white-light inspection systems with digital image processing (manufactured by KLA) are available for in-line monitoring of defects. These systems, which have been used in fabs for several years, have

only recently become capable of real-time processing of the enormous amount of defect data generated in the monitoring process.

Yield management must enable process engineers to be able to understand and evaluate the trade-offs between the cost of an inspection and the potential cost of lost product if a defect remains undetected for any significant amount of time. By analyzing, in near real-time, product test results and monitoring information, yield might be suitably predicted so that a decision of whether to scrap product based on the data can be made. Sematech is in the process of developing such as system (Figure 3-17), which integrates information from a variety of defect metrology tools (from Tencor, KLA, Ultrapointe, etc.) with characterization tools (i.e., SEMs, FIB systems, etc.), electrical test results (Hewlett-Packard or other), and the CAD database.[3] Working from a Sparc-based host PC, such a comprehensive yield management system would be able to automatically correlate process defects to electrical test results, while also considering SPC data. Defect partitioning would allow isolation of defects to the process cell or process tool in which they were first detected. The relationship to probe yield would allow identification of "killer defects," and could provide clues as to the causes of these defects. This capability should greatly enhance the defect budgeting process.

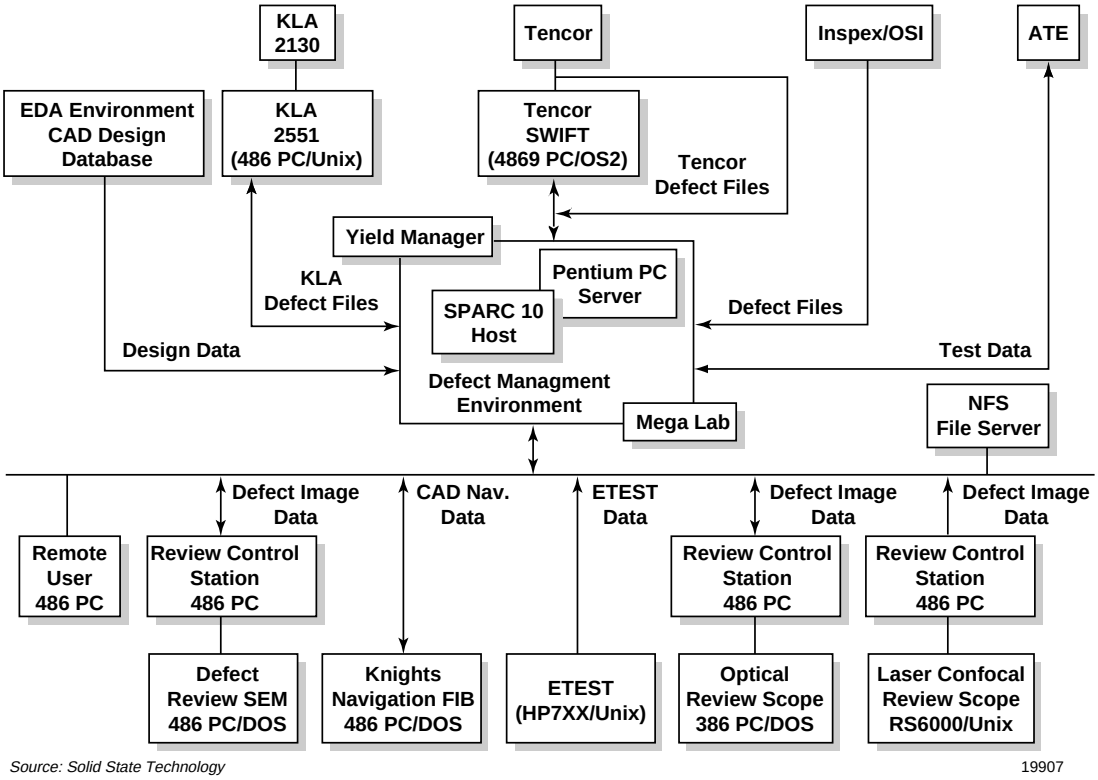


Figure 3-17. Comprehensive Yield Management System Under Development at Sematech

As we reviewed in Chapter 1, yield depends on defect density. It is also generally accepted that at least 50 percent of yield loss in fabs is due to random defects, in other words, contamination at the wafer surface. However, despite this relationship, methods for directly correlating yield and device performance to actual contamination levels is practically non-existent.[2] In addition, yield is always going to be a function of the device and its associated process. As new fabs tackle the challenges associated with characterizing processes for sub-0.5mm processing, many traditional laboratory tools typically used for failure analysis and device characterization may become attractive for in-line defect monitoring (Figure 3-18).

Process Capability and the Role of SPC

Comprehensive yield management in a fab would ideally include the automated collection of data from multiple sources (both process equipment and monitoring tools), feedback to a common source for real-time analysis, automatic classification as to impact on yield and cause of defect, and rapid elimination of yield-limiting problems. Yield improvement would be driven by the ability to continually improve process capability, while decreasing defect density at each major process tool. In reality, however, most existing fabs have neither the sophisticated software solutions nor the workstations needed to process the data and implement such real-time yield management. In addition, the methods for directly correlating yield and device performance to actual contamination levels are scarce, although companies including Texas Instruments, Tencor, KLA, Hewlett-Packard, and others, are developing these capabilities.

Another major factor controlling line and probe yields is the ability of the fab to control process variations on critical parameters. In many progressive fabs, situational Statistical Process Control (SPC) is now becoming more popular as engineers concentrate more on critical processes and avoid the temptation to overuse tools such as process control charts.

Although there are a variety of tools available to the process engineer to assist in making statistically valid decisions with a small amount of data, the most useful Statistical Process Control tools in the fab are:

- Process Capability Analysis
- Process Control Charts
- Measurement System Analysis

Care must be exercised, however, that the usefulness of these tools is directly related to the ability of the engineer to apply them correctly to specific applications. As an example, consider the case of Variable Control Charts and their applicability to fab operations. Figure 3-19 shows a classical variable control chart form applied to sheet resistance values from a diffusion operation. The X bar, R chart shown in the figure was originally developed in the 1920's by Shewhart and was intended to track a continuous flow manufacturing process that produces large quantities of identical product. In our application in the fab, the process is more batch oriented and the target values might vary from batch to batch. Therefore, the sampling plans, frequency of sampling, control limit calculations need to be modified to account for the possibility that several families of variation could exist and that the chart should be sensitive to all of those possibilities. That is why new control chart types, such as the Roberts Chart, have been developed. More and more of these charts are

being commented on in the literature and the creative process engineer should be on the alert looking for adjustments in the tools that reflect changes in process technology.

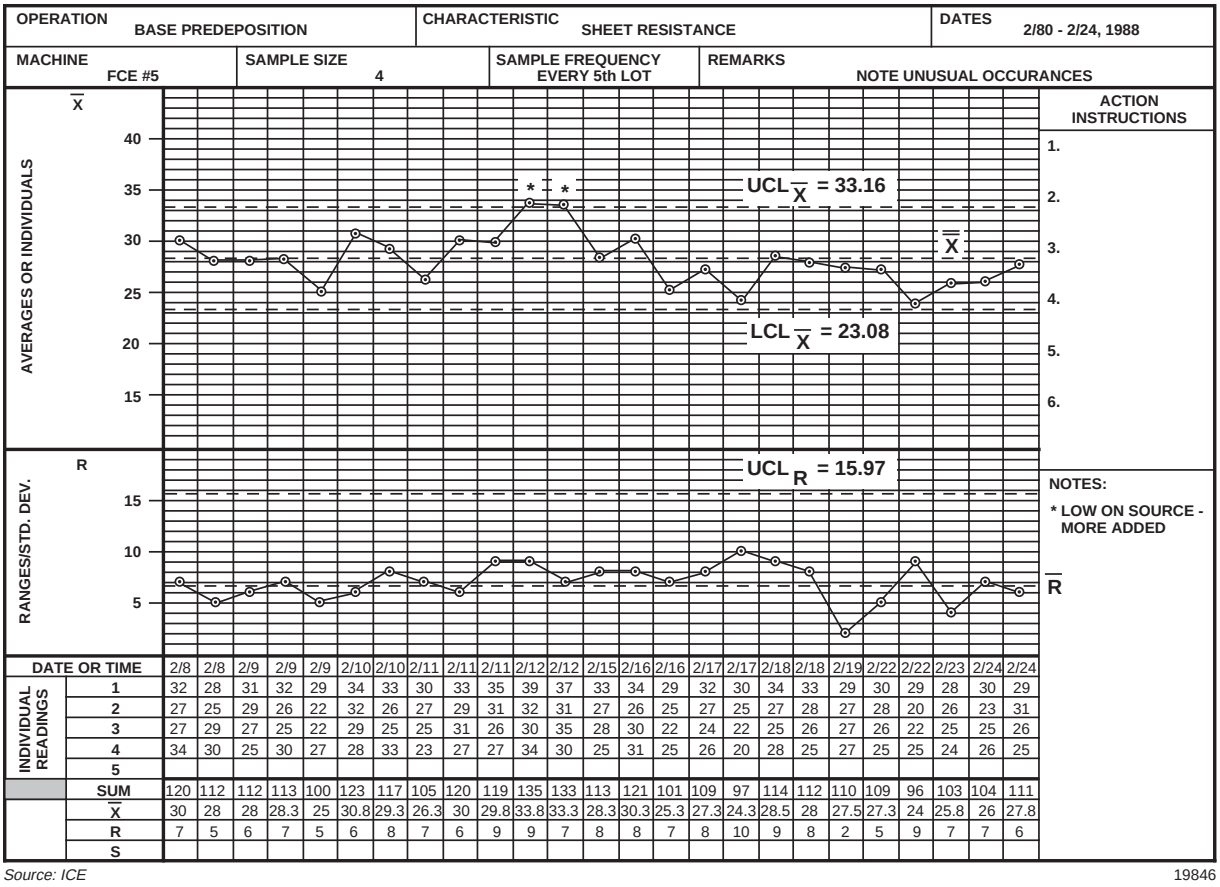
Process Analysis	Wafer Fab Technology		
	1.0μm	0.7-0.8μm	0.4-0.6μm
Microstructure and Microtopography	LaB_6 50Å SEM 120keV 3Å TEM	20Å FESEM 200keV 1.8Å TEM AFM & STM	Immersion Lens 8Å FESEM High Voltage or FETEM AFM & STM
Composition and Phase Identification	0.5-1.0μm SEM-EDX 2000Å AES 10 μm 0_2 & Cs SIMS mm XRF X-ray & Electron Diffraction	0.3-1.0μm SEM Low-Z EDX 80Å TEM, Low-Z EDX 2000Å AES 100 μm XRF X-ray Diffraction Small Area Electron Diffraction	0.3-1.0μm SEM, Low-Z EDZ 80Å TEM, Low-Z EDX <500Å FEAES 100μm Low-Z XRF X-ray Diffraction Small Area Electron Diffraction
Residues and Organics	AES O_2 & Cs SIMS FTIR	AES, ESCA TOF SIMS 10μm FTIR & RAMAN	AES, ESCA TOF SIMS 10-1.0μm FTIR & RAMAN
Microcontamination	SIMS	TXRF VPD-GFAA VPD-ICP-AES O_2 & Cs SIMS	TXRF VPD-GFAA VPD-ICP-MS New SIMS (TOF, Post Ionization, Accelerator, <500Å Ga)
Particle Analysis	SEM-EDX FTIR AES Optical Fluorescence	SEM, Low-Z EDX AES FTIR RAMAN Optical Fluorescence	SEM, Low-Z EDX FEAES FIB With Ga SIMS FTIR RAMAN Optical Fluorescence
Mechanical Behavior	Empirical Observation Stress Measurements Of Thin Films By Measurement Of Wafer Bow	Microindentor for Stress-Strain and Microhardness Measurements of Thin Films Direct Measurement of Stress in <1.0 μm Lines by X-ray Diffraction	Microindentor for Stress-Strain and Microhardness Measurements of Thin Films Direct Measurement Of Stress in <1.0μm Lines by X-ray Diffraction
Critical Dimensions	LaB_6 Source SEM	<2keV FESEM	<2keV Immersion Lens FESEM
Film Thickness and Roughness	Optical Interferometry Ellipsometry Film Resistivity Profilometry	Optical Inferometry Ellipsometry XRF Direct Measurement AFM & STM Profilometry	Optical Interferometry Ellipsometry XRF Direct Measurement AFM & STM Profilometry
Defects Metrology	Optical Defect Inspection Tools	Optical Tools Computer Linked To LaB_6 SEM, Low-Z EDX (Automatic Particle Coordinate Transfer and Steering to Analysis Area, Image Spectral Acquisition with Digital Storage)	Optical Tools, et al., Computer Linked to FESEM, Low-Z EDX et al (Automatic Particle Coordinate Transfer and Steering to Analysis Area, Fully Automated Analysis and Reporting)

Legend:

AES - Auger Electron Spectroscopy
AFM - Atomic Force Microscopy
EDX - Energy Dispersive X-ray
ESCA - Electrospectroscopy For Chemical Analysis
FEAES - Field Emission AES
FESEM - Field Emission SEM
FETEM - Field Emission TEM
FIB - Focused Ion Beam
FTIR - Fourier Transform Infrared
low z - Light Or Low Element
RAMAN - Raman Optical Spectroscopy
SEM - Scanning Electron Microscopy
SIMS - Secondary Ion Mass Spectroscopy
STM - Scanning Tunneling Microscopy
TEM - Transmission Electron Microscopy
TOF SIMS - Time Of Flight SIMS
TXRF - Total Reflection XRF
VPD-GFAA - Vapor Phase Decomposition, Graphite Furnace Atomic Absorption
VPD-ICP/AES - VPD-ICP - Auger Electron Spectroscopy
VPD-ICP/MS - VPD Inductively Coupled Plasma, Mass Spectroscopy
XRF - X-ray Fluorescence

Source: Semiconductor International 19909

Figure 3-18. Likely Evolution of Problem-Solving Tools for Increasingly Complex Devices



DATE OR TIME		2/8	2/8	2/9	2/9	2/9	2/10	2/10	2/11	2/11	2/11	2/12	2/12	2/15	2/16	2/16	2/17	2/17	2/18	2/18	2/19	2/22	2/22	2/23	2/24	2/24
INDIVIDUAL READINGS	1	32	28	31	32	29	34	33	30	33	35	39	37	33	34	29	32	30	34	33	29	30	29	28	30	29
	2	27	25	29	26	22	32	26	27	29	31	32	31	27	26	25	27	25	27	28	27	28	20	26	23	31
	3	27	29	27	25	22	29	25	25	31	26	30	35	28	30	22	24	22	25	26	27	26	22	25	25	26
	4	34	30	25	30	27	28	33	23	27	27	34	30	25	31	25	26	20	28	25	27	25	25	24	26	25
	5																									
	SUM	120	112	112	113	100	123	117	105	120	119	135	133	113	121	101	109	97	114	112	110	109	96	103	104	111
	$\bar{X}$	30	28	28	28.3	25	30.8	29.3	26.3	30	29.8	33.8	33.3	28.3	30.3	25.3	27.3	24.3	28.5	28	27.5	27.3	24	25.8	26	27.8
	R	7	5	6	7	5	6	8	7	6	9	9	7	8	8	7	8	10	9	8	2	5	9	7	7	6
	S																									

Figure 3-19. Example of a Statistical Process Control (SPC) Chart

Measurement System Analysis is a critical part of ensuring control over process variations. The basic concept is to be able to analyze any measurement system to determine it's vulnerability to measurement variation. Since measurements are simply another manufacturing related process, one has to expect that variations when measuring a unit multiple times will occur. The goal is to quantify that amount of variation to avoid invalid conclusions about variation. In other words, when experiencing variations when measuring a characteristic of the unit, the natural assumption is that it is due to the process. If the variation is measurement related, there is a real risk that unnecessary adjustments in the process will be executed, thereby exacerbating the total variation.

Also, by performing Measurement System Analysis, it is possible to identify incapable measuring systems and anticipate when future problems might occur. As a rule of thumb, one looks for the variation due to the measurement system to be less than 10 percent of the tolerance goal.

Existing fabs generally utilize SPC out-of-spec data, probe data, and data from field failures to identify sources of yield loss when yields fall below acceptable levels. For shop floor control, Promis or Workstream software packages are used, with operators manually entering information needed to later track low yielding wafers to equipment sets, operators, process conditions, etc. In addition to these commercially available

solutions, many manufacturers have developed proprietary solutions for yield management and shop floor control (controlling work-in-process (WIP), inventory and equipment). They might also have proprietary methods for achieving a certain level of in-line defect monitoring.

When new equipment is brought into the fab, its operations are characterized for each device manufactured in that facility. Statistical techniques should be used to relate process variations to yield. From that initial analysis, key parameters are selected for process monitoring and for process capability analysis.

Histograms can be constructed to verify normality as part of the process capability study and is intended to ensure that processes with only random effects are quantified in the study. For example, a histogram of sheet resistance is shown in Figure 3-20. Since the definition for process capability is the distance between -3s and +3s around the mean, a simple calculation using a reasonable sample size will quantify the amount of variation in the process under investigation.

To evaluate the calculated process capability versus fab requirements, the process engineer will normally use Process Capability Indices such as Cp and Cpk. These indices are figures of merit that describe the process variation in terms of it relationship to a set of specifications. The objective is to have a process capability index as large as possible which indicates that the total process variation is considerably smaller than the specification it is intended to satisfy. Figure 3-21 illustrates the relationship between process variation and process capability indices for a given specification. Also included are the formulae for Cp and Cpk for comparison.

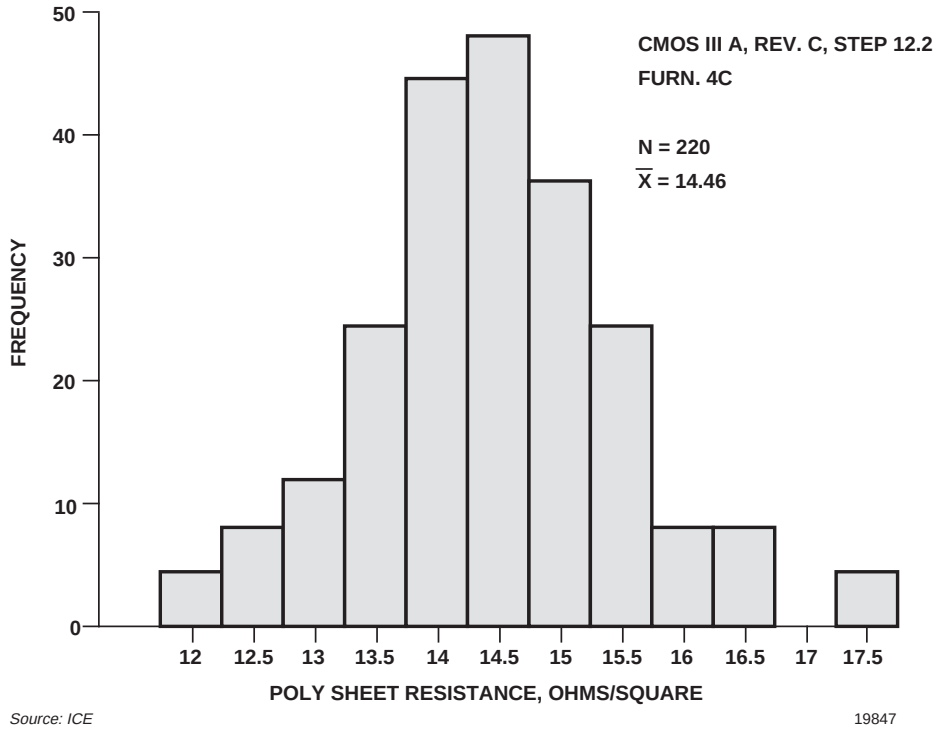


Figure 3-20. A Typical Histogram Shows the Distribution Around a Target Value

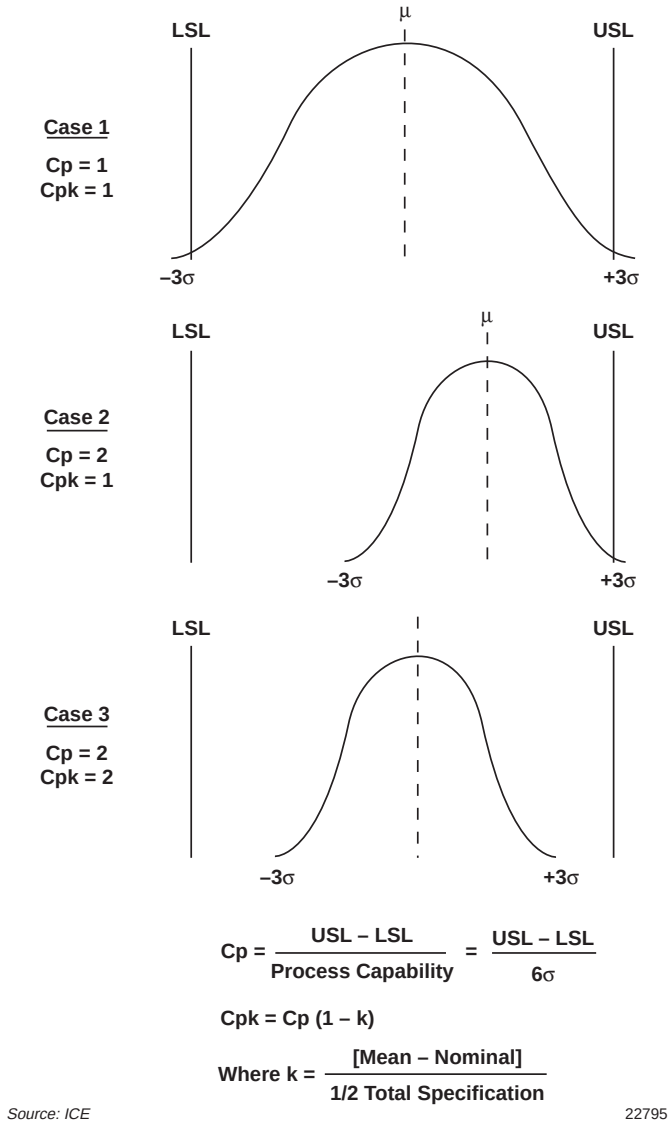


Figure 3-21. Relationship Between Cp and Cpk

The use of SPC data for continuous improvement in a semiconductor manufacturing environment has become hampered by the increasing volume of data produced at each process step. One must focus on the important measurements (determining which measurements are key to product quality). Typically, engineers analyze defect distributions, constructing Pareto charts that plot the reasons for failures versus the frequency of occurrence. Then the defect is traced back to any number of causes (i.e., if the problem is shorts, SEM and FIB analysis among elemental SIMS or other analyzes might be used to identify the culprit). Data allows tracing to the specific tools, recipe, set-up, operator, etc., along with PM schedules.

Ultimately, the product yield is affected not only by the processing and testing of the chip, but also the original design. While a thorough discussion of EDA capabilities is beyond the scope of this book, suffice it to say that many companies are interested in tying yields and process data back to the original design.

Yield Data Management Systems

As the need for more data relevant to making improvements in line and probe yields becomes more acute due to the tremendous leverage of yield on manufacturing costs (and therefore profits), another potential problem is created. The extremely large amount of data now available for this purpose needs to be managed in a systematic way to ensure the efficient implementation of improvement programs.

To this end, organizations have tried to adopt data management systems to assist in this task. Some fabs have taken the approach of developing their own internal proprietary systems to coordinate the data generated by analysis tools. To a large degree, this was necessary due to the lack of standards utilized by the metrology manufacturers, and to the lack of commercially available systems for managing this type of data. The degree of success realized through this approach has been directly correlatable to the internal resources available to the interested organizations.

As an example, Intel has had success in applying the "Theory of Constraints" concepts presented in the 1993/1994 time frame in papers by Menon and Sohn to fab line yields. The model allows for the establishment of individual operation scrap goals based on an overall line yield goal. Figure 3-22 illustrates a table of individual process step goals within a cluster, along with actual performance and focal areas for improvement.

Cluster Toolset	Scrap Goal	Weekly Scrap	Delta	Focus Areas
M. Etch	27	250	(223)	M. Etch
Planar	9	52	(43)	Planar
Sputter	31	64	(33)	Sputter
Diff:FE	186	210	(24)	Diff:FE
Gold	3	10	(7)	Gold
WAMO	10	9	1	
AMAT	24	23	1	
Diff:BE	3	—	3	
WJ	6	2	4	
LRC	70	54	16	
Litho	130	101	29	
Implant	56	26	30	
AWS	145	66	79	
Total	700	867	167	

Source: Intel 22796

Figure 3-22. Hypothetical Weekly Scrap Targets

In the recent past, several alliances have been formed to attempt to integrate the actual data being generated into a yield improvement methodology. One example of this type of effort is the formation of the Yield Management Team (YMT) which has members from several companies representing metrology hardware, wafer probe equipment, and software solutions. The team includes Advantest Corp., Electroglas Corp., Keithley Instruments, Knights Technology, SVR, and riant Technologies Inc.

The goal of YMT is to work on improving technical equipment and software interfaces and develop new technologies, and then try to select the best combination of equipment and software for individual fab requirements.

Figure 3-23 represents how a fab might integrate the in-line data generation, analysis, and end of line test data into a centralized, rational data base.[4]

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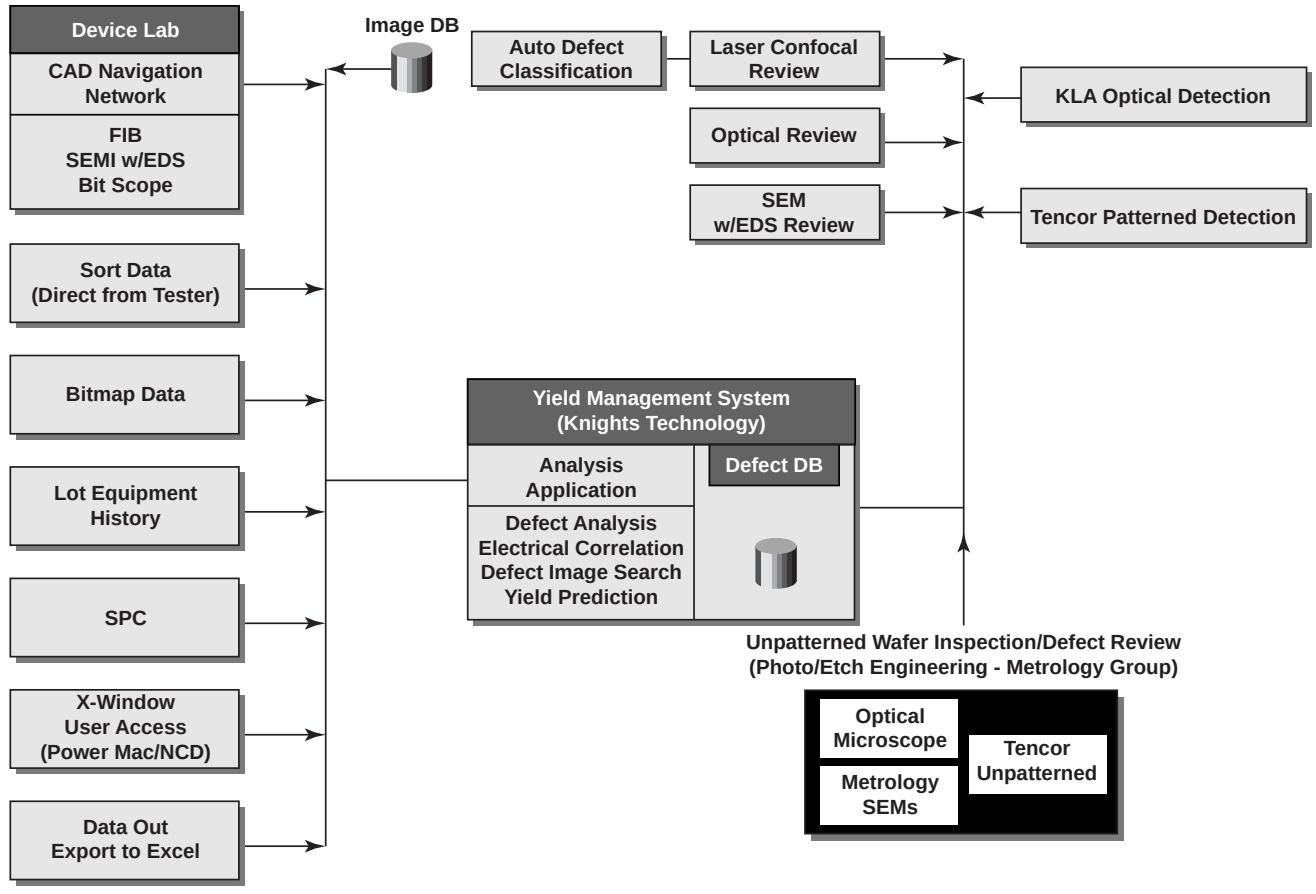

Figure 3-23. MOS-13 Defect Management System