4

Fab Benchmarking

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Fab benchmarking is a practice used by semiconductor manufacturers worldwide to assess the competitiveness of their manufacturing operations. Benchmarking between fabs within a company is a common practice, as manufacturers today can have 20 or more fab lines worldwide. Comparisons among different semiconductor companies is less commonly performed and is typically accomplished using outside consulting firms. In any event, benchmarking is a formal practice designed to assess a fab's or company's performance relative to the performance of world-class manufacturers. World-class semiconductor operations are distinguished in terms of line and probe yields, manufacturing cost per wafer, labor productivity, cycle times, tool productivity, and on-time delivery performance. World-class fabs also consistently improve performance in each of these areas through superior practices in manufacturing technology, factory operation, organization, and management. Importantly, a world-class fab does not have to be a manufacturer of state-of-the-art devices: It achieves excellent asset management given the assets that it has.

This Chapter first defines world-class manufacturing and presents associated performance objectives. It then explains how benchmarking measures consist of several different, yet interrelated categories including:

- Yields and yield learning
- Process control and Computer integrated manufacturing
- Cycle time management
- Tool productivity
- Labor productivity
- Human resources management
- Customer satisfaction

In each of the categories, metrics of performance are defined and explained. For instance, within the category of tool productivity are such metrics as cost of ownership and overall equipment effectiveness. Fab-wide, companies often use various management strategies to target many or all of the above goals. Chapter 5 which follows explores the use of such management strategies and the practical implementation of these techniques by different semiconductor manufacturers.

Within this chapter, select results are also presented from a worldwide survey of 28 fabs designed to identify operational practices that underlie leading-edge manufacturing performance. The Competitive Semiconductor Manufacturing Survey[1], performed by the University of California at Berkeley over a five-year period, was the first study of its kind in the semiconductor industry and it revealed the large variation in performance among semiconductor fabs.

Importantly, the study tied the achievement of high marks in a developed set of performance metrics with a list of key practices.

World-class Manufacturing Objectives

What makes an IC manufacturer or its suppliers world class? To maximize the productivity of fab operations, IC manufacturers continually strive to:

- Increase yields,
- Increase throughput,
- Decrease inventories,
- Decrease operating expenses,
- Decrease lead times, and
- Improve customer service.

These goals are accomplished by reducing manufacturing cycle times, improving throughput (by increasing equipment productivity), and reducing the time spent performing non-value added procedures (i.e., misprocessing, set-up of equipment, running test wafers). Therefore, world-class manufacturing objectives become:

- Improved process capability,
- Greater equipment availability/utilization,
- Reduced misprocessing,
- Higher yields,
- Reduced step-up time of equipment,
- Selective use of off-line metrology and inspection equipment,
- Faster learning and diagnosis (e.g., yield ramp or yield learning),
- Improved scheduling and maintenance procedures,
- Smoother transitions from R&D and pilot-line operations to production,
- Better understanding of processes and manufacturing, and
- Improved employee productivity and morale.

Because so many of these objectives rely on equipment performance, the requirements for each piece of equipment become critical.

Equipment Selection Criteria

A short list of the most important criteria in equipment selection follows.

- Process capability, and flexibility to meet future requirements,
- High reliability (mean time between failure of at least 200 hours),
- High availability,
- High throughput to maximize the number of wafer processed,
- Low, consistent, and predictable defect density,
- Serviceability, and
- Low cost of consumables.

High yields are achieved when the process capability of each piece of equipment is well characterized and repeatable. As device requirements change more quickly and as product introductions shorten, equipment must increasingly be able to meet today's performance objectives and readily extend to meet tomorrow's requirements.

Equipment selection criteria have changed over the last 20 or so years. While performance remains one of the key criteria, fab managers are increasingly stressing the importance of equipment cost-of-ownership, serviceability, and reliability.

Benchmarking Yields and Yield Learning

Results from Berkeley's CSM study indicated there are eight underlying themes for world-class manufacturing. With respect to yield and yield management, key practices of leading fabs in the study included:

- Rigorous management of SPC programs, retiring unneeded control charts and adding new ones as needed, adjusting control limits as appropriate and adjusting frequencies of measurements to focus on critical areas of improvement
- Automatic display of corrective action guidelines when an out-of-control situation occurs, often accompanied by automatic notification of the engineer and automatic disabling of the equipment
- Automated uploading of metrology data, SPC measurements, tracking data, etc.
- Integration of engineering databases and in-line defect inspection results with databases of die yields, parametric measurements, allowing statistical correlation between die failures and causes
- Extensive analysis of wafer map and bit-fail patterns to trace faults to the root cause of the defects. The cause may be related to processing equipment, environment, people, etc.
- Automated recipe downloading at the tools with "smart" lot-machine interfaces

Bringing New Equipment and Processes into the Fab

Semiconductor manufacturers typically spend a lot of time and money bringing new equipment into the fab. Any reduction in this critical "yield learning" time can significantly improve the company's competitive position. In some cases, rapid yield learning allows the company to bring new devices to market faster, for which it can command higher prices, leading to higher profits. By bringing equipment to a production-worthy state faster, the cost burden of the newly-purchased piece of equipment is also lessened.

Semiconductor firms use a variety of strategies to reduce the time-to-silicon or time-to-money. Today, equipment is often installed at the vendors' sites several months prior to being placed in the fab so that the new processes and equipment will be optimized prior to fab installation. Marathon testing is typically performed to ensure adequate mean time between failure (MTBF) and mean time between repair (MTBR) rates on the equipment. Such processes have become more necessary as the complexity of equipment has accelerated over the years (both in terms of hardware and software), and new equipment development and introduction cycles have accelerated with advancing technology.

There are essentially three distinct, yet overlapping stages a new piece of equipment undergoes (Figure 4-1). First, the equipment vendor typically develops a unit process or processes, which are usually tested first at the vendor's site, known as alpha-site testing. The next phase is beta-site testing. During beta-site testing, the unit process or processes are customized for each of the IC manufacturers processes, and the process may be further optimized to allow for integration. Beta-site testing can include processing of up to a thousand wafers. Many of the larger IC houses will perform "Ironman" or "marathon" testing of new equipment at one site, for the benefit of the entire organization. During such tests, equipment is run continuously and modifications to the equipment are made to continually reduce mean time between failure and mean time to repair rates. In the third stage, the IC manufacturer purchases additional equipment (ramp-up) to tool its facility. At this stage, minor improvements that might only be realized during production are performed. Here we

review strategies used by Intel and Motorola to accelerate cycles of learning and ensure the use of production-ready equipment in the production line.

Intel's Partners With Vendor to Enable Faster Ramp-up

Intel recently used a partnership-based management strategy to develop and transfer a new process tool into production.[2] The strategy was designed to ensure minimum impact to fab output, and faster return-on-investment based on the minimization of process and equipment changes once the tool is installed in a manufacturing line. The equipment improvement program included proliferation methodologies to rapidly improve equipment performance and improve site-to-site process replication among Intel fabs. The complete program reduced the cost of ownership of the unit process by 60 percent due to an increased throughput of 18 percent, a 2X defect reduction, and a 4X increase in the number of wafers processed between preventive maintenance procedures. This project was performed while both development and manufacturing fabs were in the middle of an aggressive ramp.[2]

The upgrade consisted of nine modifications to the chamber hardware and a process change. It took nine months to complete, and involved interaction between five groups within Intel and four groups at the supplier. The article stresses the importance of close vendor-customer relations throughout the development phases. The project attempted to eliminate past problems, including poor parts' quality, delays in delivery, insufficient documentation, insufficient operator training, and poor process replication. Such problems are at least partially due to the intense pressure on vendors to improve product performance and meet product introduction dates, often resulting in equipment introductions that do not meet advertised benefits. To meet demand, vendors are compelled to subcontract parts manufacturing to more than one subcontractor, which can result in significant lot-to-lot variation. In addition, without adequate training on specific hardware, parts may be installed incorrectly. The set of process improvements on a 200mm CVD system are summarized in Figure 4-2.

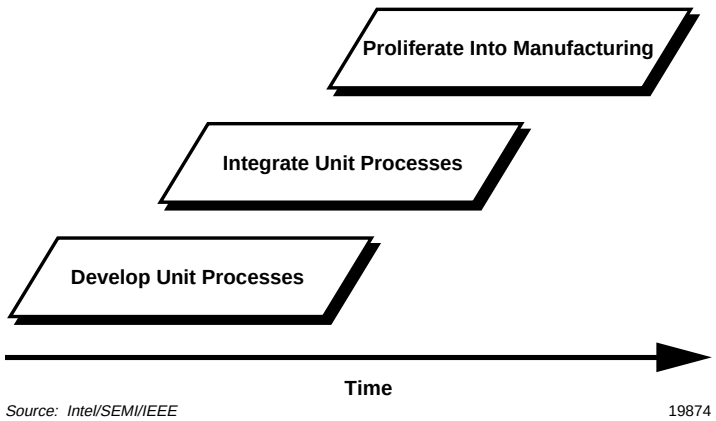


Figure 4-1. The Entire Process Development Cycle Takes Two or More Years to Complete

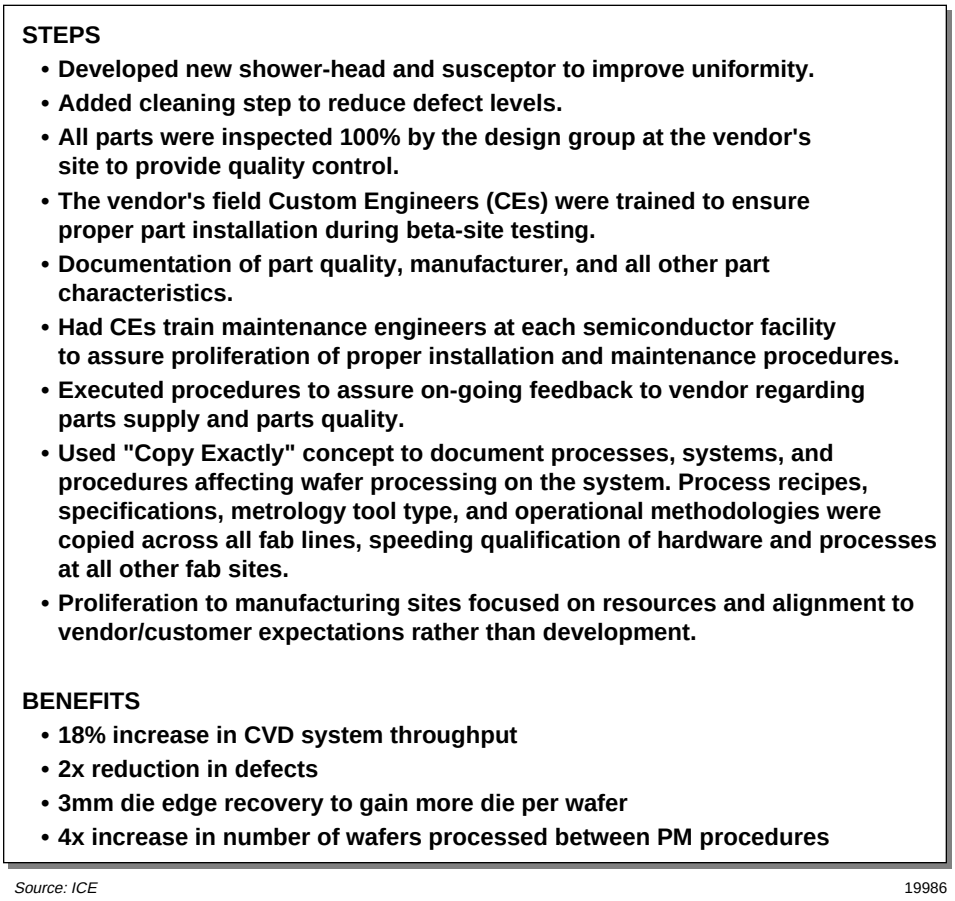


Figure 4-2. Steps Taken to Improve the Manufacturability of a 200mm CVD Tool and Benefits Gained

Initially, the CVD tool had been fairly non-manufacturable, with very low uptimes and high defect densities. To improve uniformity, first, a new showerhead and wafer susceptor were designed. While this change significantly improved uniformity, uniformity drift problems after 150 wafers persisted. Next, an additional clean recipe was developed.

To reduce variation in spare parts, the vendor was informed in advance about the scope of the project and was required to freeze parts manufacturing processes so that all spare parts manufactured would be identical to those that were being beta-site tested. Then, an inspection procedure at the equipment vendor was developed to ensure 100 percent inspection of each part for quality control. A documentation procedure was also instituted to ensure parts quality.

Next, the equipment engineers that installed the parts during alpha site testing trained the equipment engineers, and this team then trained the Intel technicians at each site in proper part installation.

In spite of this high level of control, out-of-specification parts were still shipped, emphasizing the need to improve vendor-customer relations. Site-to-site process replication, due to small differences in systems set-up (such as different pumps), continued to be an issue. One procedure that aided

site-by-site replication was the use of a "copy exactly" procedure, where process recipes, specifications, etc., for a particular module were copied across all fabs manufacturing a particular product. Proliferation was thereby simplified, as the qualification at the manufacturing sites was viewed more as an extension of a "post-PM qualification," rather than a new hardware qualification. This resulted in substantial savings in test runs and manpower.[2]

Motorola Targets Faster Cycles of Learning

Motorola recently outlined a proactive approach to equipment development, aimed at shortening the cycles of learning on new processing equipment.[3] The program uses "Ironman" testing and a comprehensive debug process at the vendor's site to allow the manufacturing robustness of both software and hardware components of process tools to be increased. The program continually tracks how quickly design problems are fixed, so that engineers can drive key parameters to lower values of mean-time-to-failure, mean-time-between interrupt (or repair), and cost of ownership. As a result, the quality and cost effectiveness of the delivered equipment is improved, and the cycle time for bringing the equipment to a production-worthy state is shortened significantly.

Motorola first created Strategic Equipment Teams, empowered to identify the technologies and equipment needed to process future devices. The teams could either choose commercially available equipment or, if not satisfied with these systems, engage in joint development programs with the vendors to assure development and "burn-in" of systems and the availability of production-worthy equipment within a usable timeframe. The teams:

- Established sector-wide equipment roadmaps,
- Integrated equipment evaluations and development methodologies sector-wide,
- Benchmarked equipment performance in existing factories,
- Recommended manufacturable equipment sets for future factories, and
- Sent a single message to suppliers, reflecting needs of the entire sector.

One of the techniques the company used to improve supplier performance included installing a Motorola-owned processing tool at the vendor's site for parallel use by its engineering group and Motorola engineers. Typically, latest products are not readily available for the vendor to perform hardware and software testing. In this process, the engineering team at the vendor's site identified faults in the system, and executed Engineering Change Notices (or the equivalent) to drive continuous improvement of the equipment hardware and software in a timely manner. A key issue was ensuring that the engineering project manager could implement such changes and proliferate them in the field, into the vendor's manufacturing, and into the new product design.

The focus of "Ironman" tests is to improve the performance of the integrated hardware, wafer transfer, and process control of the equipment. Motorola has found in previous Ironman studies, that approximately 90 percent of all manufacturing performance issues identified with available tools in the early

stages are either hardware or software related. This is key as vendor's equipment improvement efforts typically focus on process performance, not equipment manufacturability or robustness. During these Ironman test, the equipment:

- Runs a process recipe 24 hours a day unless required for process development or design evaluation related activities,
- Undergoes routine PM , start-up, and shutdown procedures, testing all hardware and software capability of the tool, and
- Undergoes system hardware and software upgrades and process enhancements.

The equipment debug phase generally undergoes three stages of learning. First, major improvements are made, resulting in up to 5-20 hour MTBI (mean-time-between-interrupt), with the second stage extending that level to 20-60 hours MTBI. The third and most challenging cycle is when MTBI approaches 120 or more hours. During the entire debug process, the teams continually track the time it takes to identify an issue, design a fix, evaluate the new design, and make the fix available. A metric tracking the cycles of learning is identified and improved upon in a systematic manner.[5] The equipment improvement at the supplier site is critical, as it represents full departure from previous procedures in which the equipment was essentially debugged by the customers in the fabs in a non-competitive fashion.[5]

The article points out how process tool testing has evolved with the increasing software component in semiconductor equipment (Figure 4-3). In the 1970s and 1980s, tests focused on mechanical and electrical performance. Today, while understanding of mechanical failures has evolved to a sophisticated level, expertise in software programming has not developed as quickly. In addition, certain problems can be both software- and hardware-related. In Motorola's study, this was evidenced by the number of software fixes for different iterations of a system's software, which did not continuously improve (Figure 4-4).

Reliability Level	Time Period		Statistical Test
	Hardware	Software	
Percent or Parts Per Thousand	1970s	1990s	Test all
Parts Per Million	1980s	2000s	Sampling
Parts Per Billion	1990s	2010s	Varied Statistical – Accelerated testing – Burn-in testing – ESS – Life testing – (etc.)

Source: Motorola/IEEE/SEMI 19875

Figure 4-3. Software development Has Become a Key Aspect of Process Tool Development

Revisions	Required Fixes
2.1	105
2.2	73
2.3	24
2.4	7
2.5	23
2.7	45
2.8	29
3.0	27
Average	42

Source: Motorola/IEEE/SEMI 19876

Figure 4-4. Number of Fixes for Different Revisions of Software Programs Do Not Necessarily Improve

The article suggests that Ironman studies be run only after the equipment has demonstrated MTBI levels of 120 hours or more. When this level is attained, any introductions of hardware or software to the tool will slow development and may actually degrade system performance. It also recommends that the supplier run marathon tests continuously, while tracking and improving on the time needed to implement design fixes.

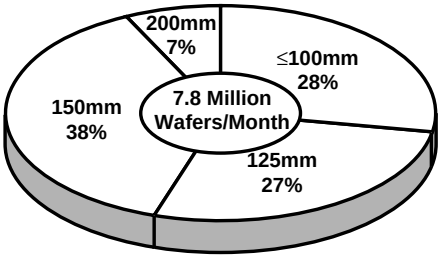
By installing the Motorola-owned equipment at both the vendor's site and the user's site, parallel, more cost-effective programs for process improvement were possible.

From year-to-year, the 800 plus existing fabs are being made more cost effective out of necessity. In 1994 and early 1995, many existing fab expansions and upgrades were being performed in conjunction with improvement programs to increase the effectiveness of existing equipment and facilities.

For many of these companies, the focus is on producing non-leading-edge devices (2.0-0.8μm), on 100, 125, or 150mm wafers. Because the profits on devices shrink with maturity, the company must continually reduce manufacturing costs, while producing the greatest number of good devices per wafer start (e.g., high productivity and high yields). As shown in Figure 4-5, the largest percentage of wafers used in 1994 were 150mm (38 percent), and approximately the same number of 100 and 125mm wafers were used (28 and 27 percent). Only 7 percent of the wafers used were 200mm. However, ICE expects this situation to change rapidly. Interestingly, a glance at regional wafer usage (Figure 4-6) reveals how the North American, European and ROW countries consume many more 100mm wafer than the Japanese. The distribution of fab capacities listed in ICE's 1995 Profiles report indicates how fab capacities ranges anywhere from 500 wafers per week to over 30,000 wafers per week. The goal for all these companies is to meet world-class manufacturing objectives.

The Importance of Cycle Time Management

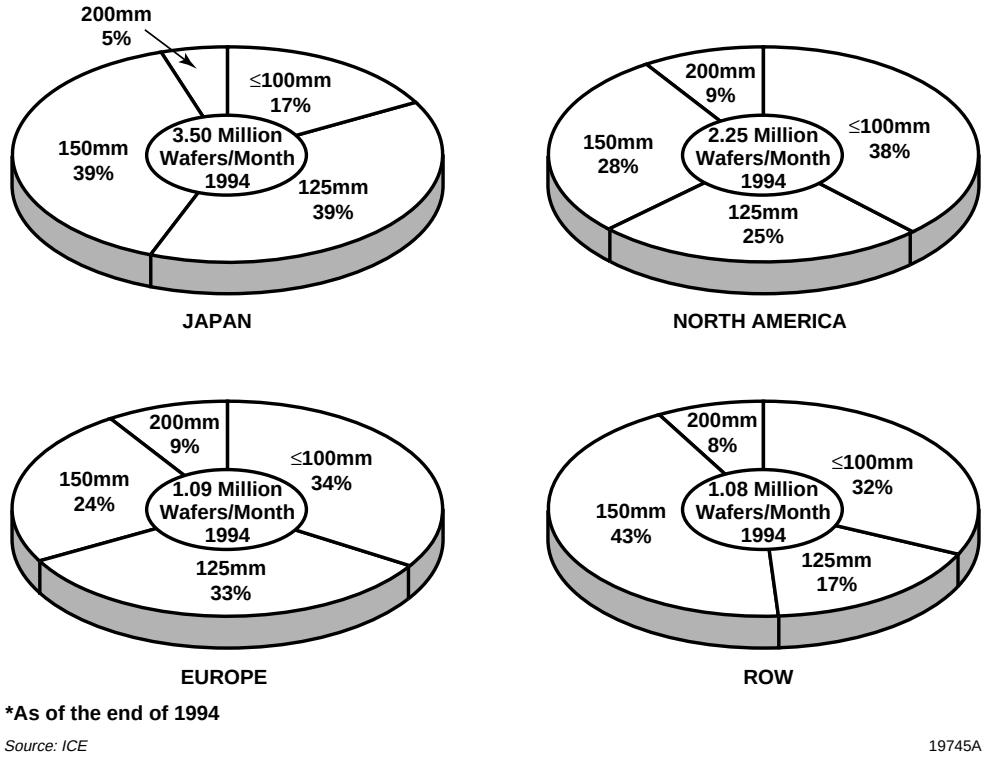
Cycle time is the time needed to fabricate devices. More specifically, it is the time required to process a product from start to finish -- either from wafer start to the time the final passivation layer is put on the wafer (wafer processing time), or from wafer start to the time the packaged device is ready for shipping. Average wafer processing time for fabs worldwide is between 30 and 90 days.



*As of the end of 1994

Source: ICE 19743A

Figure 4-5. 1994 Worldwide Distribution of Wafer Size Capacity



*As of the end of 1994

Source: ICE 19745A

*Figure 4-6. Regional Monthly Wafer Capacity by Wafer Size**

The principle advantage of fast cycle time manufacturing is rapid yield learning. "Yield learning" time, also called defect learning time, refers to the time required to bring a new product's yield to acceptable levels. Yield learning time is typically between 6 months and 2 years, depending on production capability, engineering capability, and device complexity. The obvious advantage to low yield learning time is in reducing time-to-market, often enabling the company to sell the chips at higher prices and more rapidly recoup investments. Not surprisingly, the first company bringing new devices to market is typically in a much better position to dominate the market for that particular product.

Rapid cycle time manufacturing is also becoming more critical as product lifecycles continue to shorten. As discussed in Chapter 1, products command the highest prices early in their lifetime. Therefore, the fab's ability to rapidly ramp to high volume production of devices with the highest ASPs becomes even more important. Obviously the reduced cost per wafer realized when production levels are reached are a strong incentive as well.

Fast cycle time manufacturing also means more wafers are processed in a given timeframe, so that processing problems can be detected more quickly and the yield of a given device can be improved more quickly. Industry experts have discovered time and again that a company's profitability largely depends on its ability to rapidly identify and fix processing problems.

The actual cycle time of products in a fab is limited at the low end by the raw process time for a wafer undergoing a certain process. Often referred to as the theoretical cycle time, this time is typically between 5 and 10 working days or 120 and 240 hours. In practice, a fab tries to attain an actual cycle time that is between 2X and 3X the theoretical cycle time. A cycle time of 2.5-3.0 days per mask layer is considered average, a 2-day cycle time per layer is very good and a world-class fab is capable of processing a layer in 1.2 days. Some examples of cycle time per layer for Memory fabs is shown in Figure 4-7.[1] Figure 4-8 and 4-9 show similar data for CMOS Logic and MSI cycle times per layer.

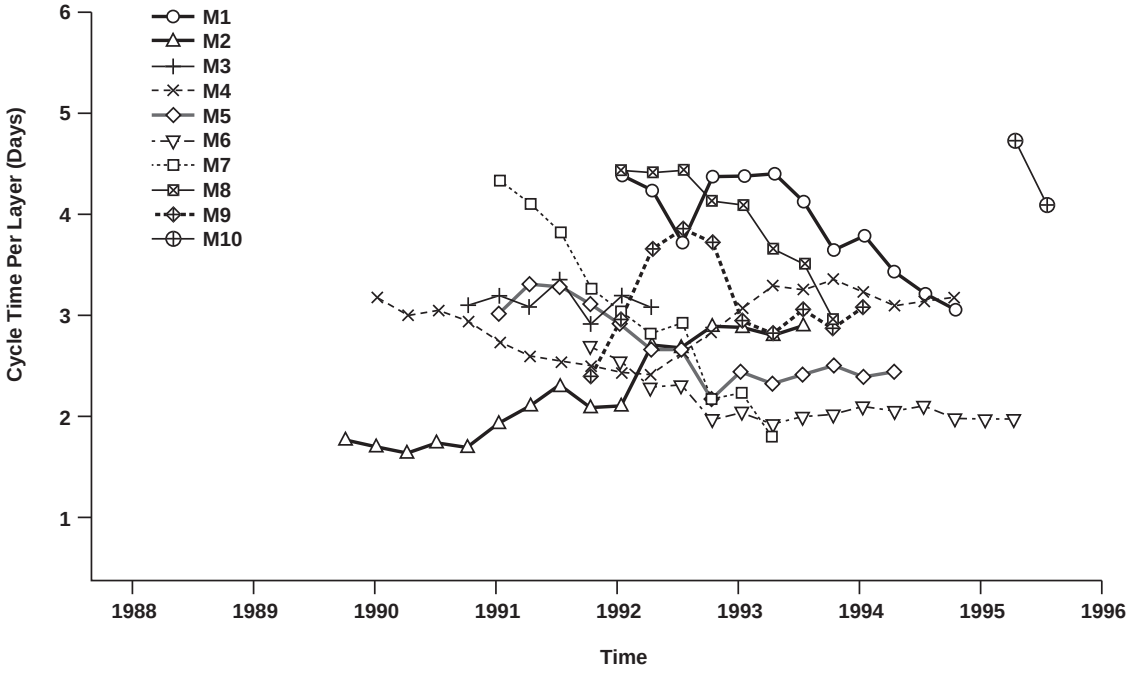
However, it is important to note that short cycle time manufacturing does have its downsides. To achieve faster cycle time, a larger equipment set is usually required so that product is not waiting for tool availability. In addition, although low cycle time enhances the likelihood of on-time delivery of devices and allows faster yield learning, it will not necessarily reduce manufacturing cost per wafer. Inventories are lower, but smaller batches of devices may need to be processed so that processing time at any one piece of equipment is not too long.

The Most Important Trends in Equipment Design

Many of the trends discussed throughout this book are critical to new fab equipment operation. To enable faster yield-learning:

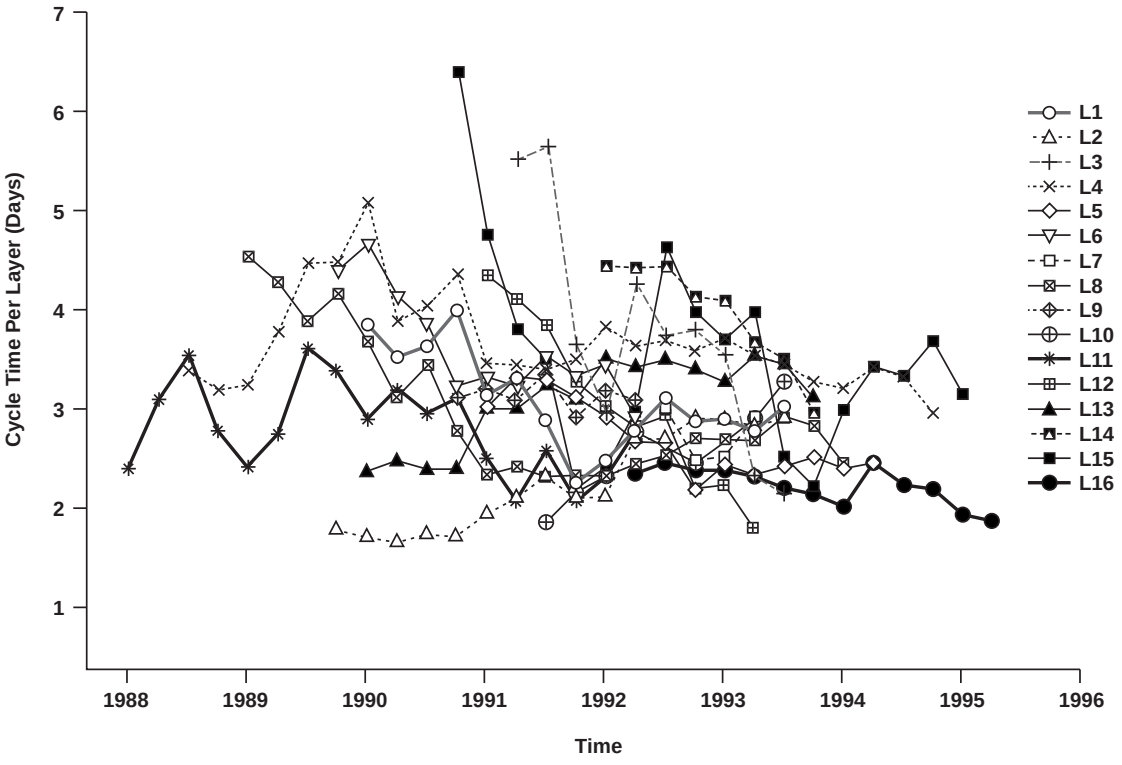
- Equipment efficiency must be increased more rapidly in the pre-production stages of development (Figure 4-10),
- The manufacturability of equipment — throughput, cost of consumables, and cost of maintenance must be targeted during equipment design phases,
- Unless the equipment vendor has extensive software programming capabilities, third- party suppliers should be used to facilitate faster time-to-market,
- Users and vendors should work together to take advantage of the latest hardware and software capabilities,
- Equipment must be capable of extending beyond one generation of product,
- Partnerships should be formed early in design phases to speed time-to-market of equipment and ensure customer satisfaction.

In addition to these trends, emerging features on production tools such as minienvironments, in-situ particle monitors, equipment control interfaces, etc., must be considered early in the design phases. Progressive equipment companies are also using modeling programs during equipment design stages to improve the quality of delivered product.



Source: University of California Berkeley 22918

Figure 4-7. Memory Fab Cycle Time Per Layer



Source: University of California Berkeley 22919

Figure 4-8. CMOS Logic Fab Cycle Time Per Layer

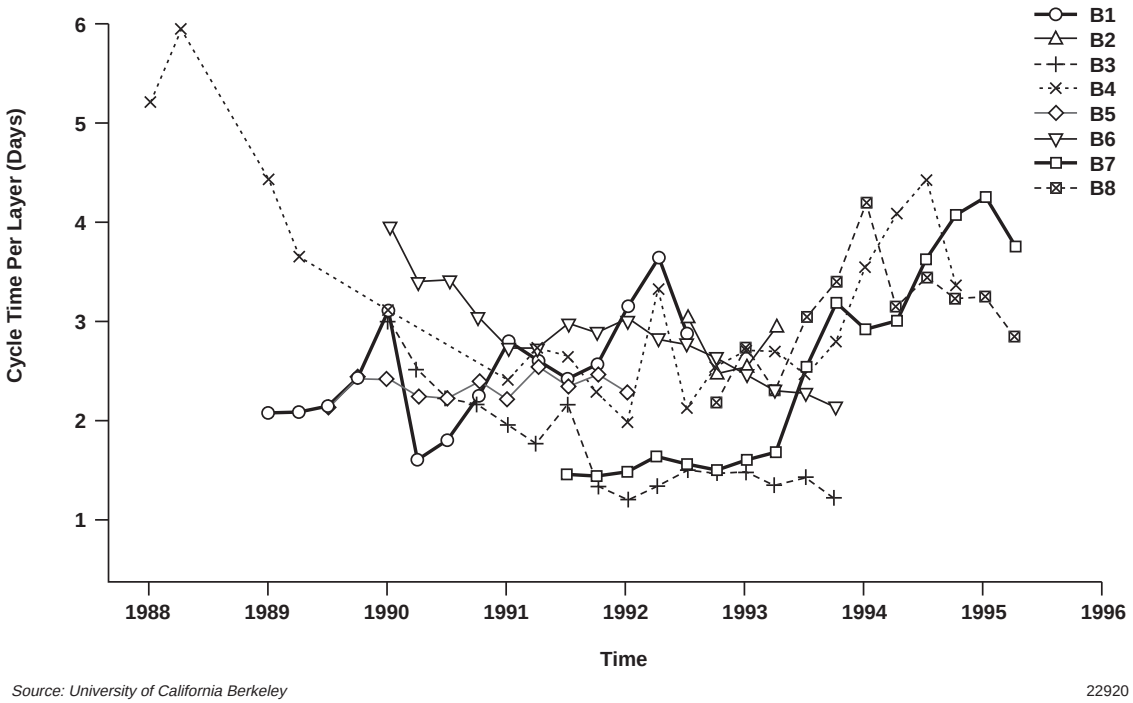


Figure 4-9. MIS Fab Cycle Time Per Layer

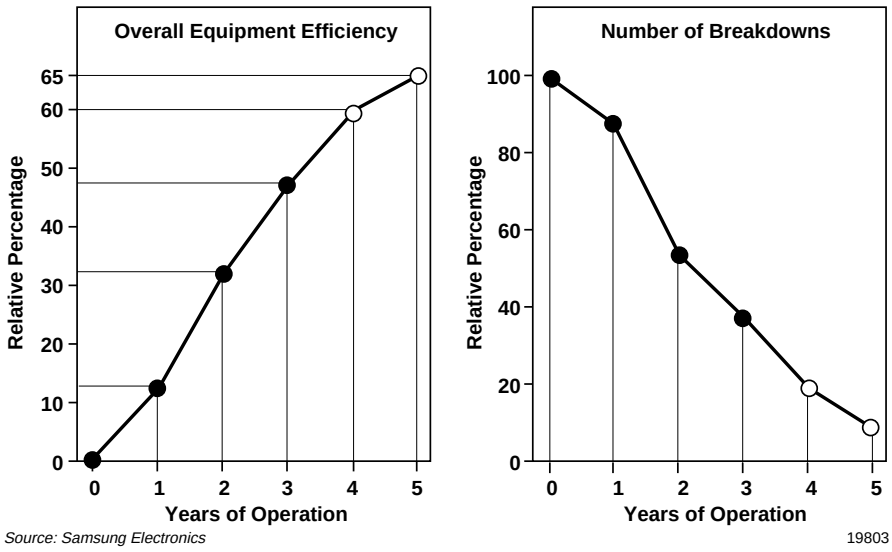


Figure 4-10. Equipment Efficiency as a Function of Product Maturity

Future tools also need real-time feedback and control of critical process parameters, optimization of batch size to reduce cycle time, and advanced product tracking to increase the productivity of the fabs. "Minibatch" tools may provide the best solution for single-wafer quality with batch throughputs. Such tools include the Novellus Concept One and Dual-Altus dielectric CVD and tungsten CVD systems, which process several wafers sequentially, Concept Systems' Gemini III epi tool or Mattson's Aspen stripper and CVD tools, which process small batches, or W-J's 1000 APCVD tool, which processes several wafers in an "assembly-line" mode.

Useful Tool Lifetime

To effectively reduce manufacturing costs, many manufacturers will attempt to use equipment for as long as possible. Tool lifetime varies depending on the type of processing equipment and the processing requirements of the devices being manufactured. In cases where device dimensions remain relatively stable for a long period of time, the fabs have very mature equipment, including 15-year-old projection aligners, 20-year-old ion implanters, and 20-year-old IC testers. However, in this industry, such examples are really exceptions to the rule. Lifetimes of some tools are often limited to only one or two generations of devices (3-6 years).

Fabs purchase new equipment if the existing equipment can no longer attain the desired process result, if it is converting from one wafer size to another, or if it is expanding capacity (in which case, used equipment might also be considered). In making transitions in device generation, the equipment can often be upgraded or undergo an equipment improvement program (EIP) to allow its use in processing the new product. Typically, 60-90 percent of the existing equipment set can be used to produce next-generation devices. Companies can effectively minimize the investment for next-generation technology by limiting the amount of new equipment purchased to less than 20 percent (reusing 80 percent), spending no more than a 1.5X premium for next-generation tools, and controlling the increase in the number of process steps to 1.1X (via device design and equipment capability). This strategy, used by IBM in the manufacture of DRAMs, slows the overall increase in wafer processing costs, and allows more timely return on investment (Figures 4-11 and 4-12).

	Per Generation	Per Year*
Productivity to Customers	2.8x	40%
Technology Change		
Bits/Chip	4.0x	58%
Chip Area	1.4x	12%
Density	2.8x	40%
Equipment Cost		
Complexity (No. steps)	1.2x	6%
Unit Price Increase	1.5x	15%
Total	1.8x	22%

*3 years is 1 generation

Source: IBM Microelectronics 19771

Figure 4-11. DRAM Industry Trends

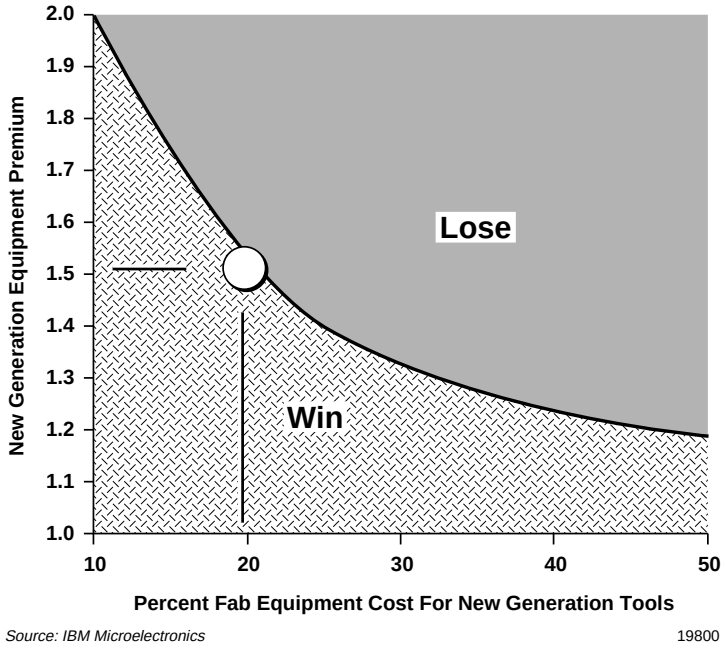


Figure 4-12. Profitability Strategy

All existing fabs continually undergo frequent changes and adjustments, and share the same constraint including[1]:

- The need to continue production operations during expansion,
- Restrictions in cleanroom space and layout,
- Constraints in available capital and operating costs,
- Fixed time to implement changes,
- Given process capabilities,
- Given cleanroom design (Class 100, Class 10, etc.),
- Given labor force,
- Existing customer commitments and inventories, and
- Existing process flows.

Equipment Productivity

Equipment productivity is a key issue in manufacturing as the performance of each wafer processing tool ultimately affects fab productivity, cycle time, and the company's ability to meet customer demands for devices. A semiconductor processing tool is available for production when it is not down due to system failure, or the performance of preventive maintenance (PM) or qualification procedures. The amount of time the system is utilized relative to the time it is available for production, is the effective utilization. One of the results of Texas Instruments' landmark MMST (Microelectronics Manufacturing Science & Technology) program was the finding that the effective utilization of semiconductor equipment averages only 35 percent[2]. As detailed in Figure 4-13, the rest of the time is spent:

- Setting-up the equipment to process the wafer (s) (including test wafer runs),
- Waiting for product to traverse through the production line,
- Misprocessing wafers due to drift in processing parameters or using the wrong process recipe,
- Adjusting process parameters,
- Processing bad material, or
- Performing scheduled or unscheduled maintenance procedures.

Such procedures lead to poor utilization of capital. In addition, as companies make transitions in wafer size, especially from 150mm to 200mm, the throughputs of tools accomplished in production have dropped. Batch to single wafer transitions in the fab also increase the amount of WIP and limit fab productivity.

Therefore, cost-reduction strategies that minimize misprocessing, set-up time, test wafer use, and unscheduled maintenance, will improve equipment utilization, and consequently, the productivity of the fab.

The COO model typically relates cost per wafer for a given device to labor rates, cost of consumables, spare parts, scrap, maintenance, off-line metrology, facilities, etc. From constructed Pareto charts that show the magnitude of each cost element, the manufacturer can target the most costly segments (Figure 4-14). In general, COO modeling has shown the industry that machine throughput, tool reliability, and defect limiting yield often have a more significant impact on COO than equipment purchase price.

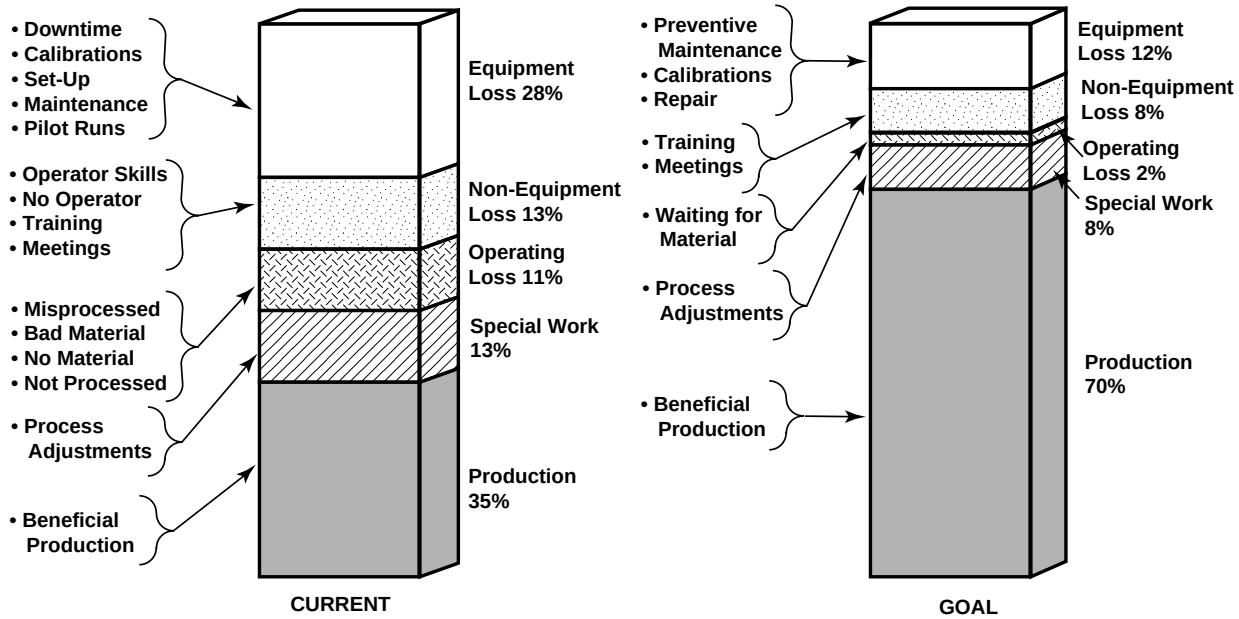


Figure 4-13. Improving Capital Productivity

$$\text{Cost per wafer} = \frac{\$F + \$V + \$Y}{L \times TPT \times Y(TPT) \times U}$$

where,

- $F = fixed cost
- $V = variable cost
- $Y = cost of yield loss
- L = equipment life
- TPT = throughout rate
- Y(TPT) = throughout yield
- U = production utilization capability

$$\text{Cost of yield loss} = [W(TPT) \times \$P] + [W(D) \times \$T]$$

where,

- W(TPT) = wafers lost to throughput yield
- $P = value of wafer at process step
- W(D) = wafers lost to defect-limited yield
- $T = value of wafer at test

$$\text{Wafers lost to defect-limited yield} = R \times L \left(1 - \frac{1}{1 + (A \times P \times D)}\right)$$

where,

- R = wafer per week
- L = equipment life
- A = die area
- P = defect fault probability
- D = physical defect density

$$\text{Production utilization capability} = 1 - \frac{(SM + USM + TEST + TA + STBY)}{168}$$

where,

- SM = scheduled maintenance
- USM = unscheduled maintenance
- TEST = production test
- TA = assist time
- STBY = standby

Source: Semiconductor International

19750

Figure 4-14. Sematech Cost-of-Ownership Model

However, despite its attributes, COO modeling cannot indicate how effectively a system is used in production.[3] For these reasons, a new metric, overall equipment effectiveness (OEE) is now gaining industry attention.

Overall Equipment Effectiveness (OEE)

OEE is the time a given system spends producing product wafers. As shown in Figure 4-15, the goal, determined using Sematech's fab model, is to improve equipment effectiveness to over 60 percent for the 0.25μm generation of equipment. An OEE of 60 percent means that the majority of losses are due to the fact that no product is available for processing (no WIP), with much smaller contributions from throughput loss, scheduled and unscheduled downtime, and setup procedures. The hope is that by focusing on OEE, manufacturers will be able to improve maintenance procedures, setup procedures and make modifications to increase machine throughput, reduce rework, etc.[5] OEE is also related to another important industry metric, labor productivity.

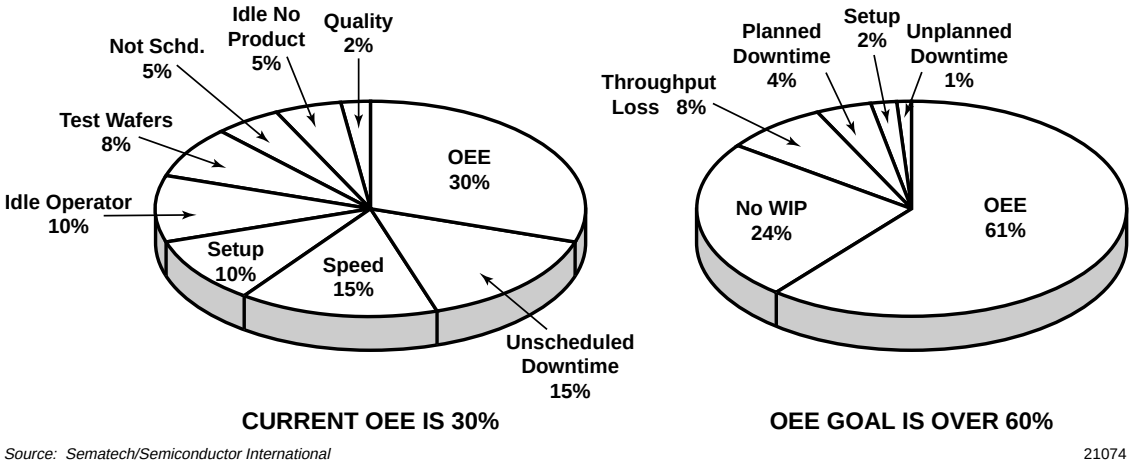


Figure 4-15. Overall Equipment Effectiveness

Cost of Ownership

Many companies use activity-based costing (ABC) to determine the relationship between the cost of devices produced by a fab and each of the components that contribute to this cost. Typically, ABC is implemented by forming the ABC team, developing the ABC model, costing the product line, planning cost reduction efforts, implementing cost reduction, and evaluating results. Cross-functional teams typically contain employees from all factory departments including finance, purchasing, technology development, process engineering, equipment engineering, production control, and facility groups. The ABC model demonstrates cost per wafer sensitivity to composite yield, production volume, utilization rate of existing equipment, and the cost of purchasing new equipment.

One type of activity-based costing technique is cost of ownership (COO) modeling. The Sematech COO model (Figure 4-14) and its many modified versions, are gaining popularity among North American companies. It is commonly used by equipment manufacturers and IC manufacturers to compare the cost of new, competing pieces of processing equipment. Some companies, particularly U.S. semiconductor manufacturers, also use modified versions of the model to estimate the cost components of tool sets in a well-established production line, an existing product line that is undergoing expansion, or a new product line. An example of a COO calculation is shown in Figure 4-16.

The cost of ownership model typically relates cost per wafer for a given device to labor rates, cost of consumables, spare parts, scrap, maintenance, off-line metrology, facilities, etc. From constructed Pareto charts that show the magnitude of each cost element, the manufacturer can target the most costly segments (Figure 4-17). In general, COO modeling has shown the industry that machine throughput, tool reliability and defect limiting yield often have a more significant impact on COO than equipment purchase price. For existing product lines, a focus on the top five cost elements, as well as specific areas where dollars are expended each year to keep the tools operating (i.e. spare parts, setup requirements, chemical

consumption, power, etc.) can lead to a simplified, more useful model.[4] A team for each operation is set up to:

- List all the major components required to perform the task,
- Collect data to estimate cost of the items over a particular time frame (weeks, months, years),
- Perform Pareto chart analysis by dividing total costs by total number of wafers produced,
- Target key areas for cost reduction, establish action plan,
- For parts/services provided by vendors, work with vendors to lower cost, extend the life, decrease the quantity required, and consider purchasing the part from the OEM rather than a distributor, and
- Obtain quotes from other vendors, give original vendor opportunity to lower prices.

For fabs undergoing a facility expansion, the model is a little more complex as it must factor in floor-space, equipment cost and depreciation, and facilities requirements.[5]

Management Summary		
Production		**$/wafer**
Throughput yield	99.95%	$0.13
Defect density (defects/cm^2)	0.01	
Probe yield	98.22%	$9.05
Composite yield (throughput yield x probe yield)	98.17%	$9.18
Production utilization capability*	63.20%	
Equipment		
Original capital cost per system	$3,400,000	$3.08
Raw throughput (throughput at capacity)	57	
Maximum wafer starts per week per system	5,992	
Equipment utilization capability**	87.13%	
Headcount Per Shift		
Direct	0.9	$0.47
Maintenance	0.3	$0.13
Indirect	0.5	$0.42
Total	1.7	$1.02
Top Three Cost Drivers		
Scrap	39.49%	$9.18
Consumables	27.98%	$6.50
Equipment (depreciation, moves, space, training)	14.34%	$3.33
All others	18.19%	$4.23
Cost Per Good Wafer Out		$23.25

*Production utilization capability: The maximum production utilization for the given qualification requirements.

PUC = Equipment Utilization Capability (EUC) - (scheduled process qual time)/168 hours as a percentage.

**Equipment Utilization Capability: The maximum utilization possible for the given equipment downtime characteristics.

EUC = 1 – (scheduled maintenance + unscheduled maintenance)/168 hours as a percentage

Source: Sematech/Solid State Technology 19765

Figure 4-16. Sample COO Summary

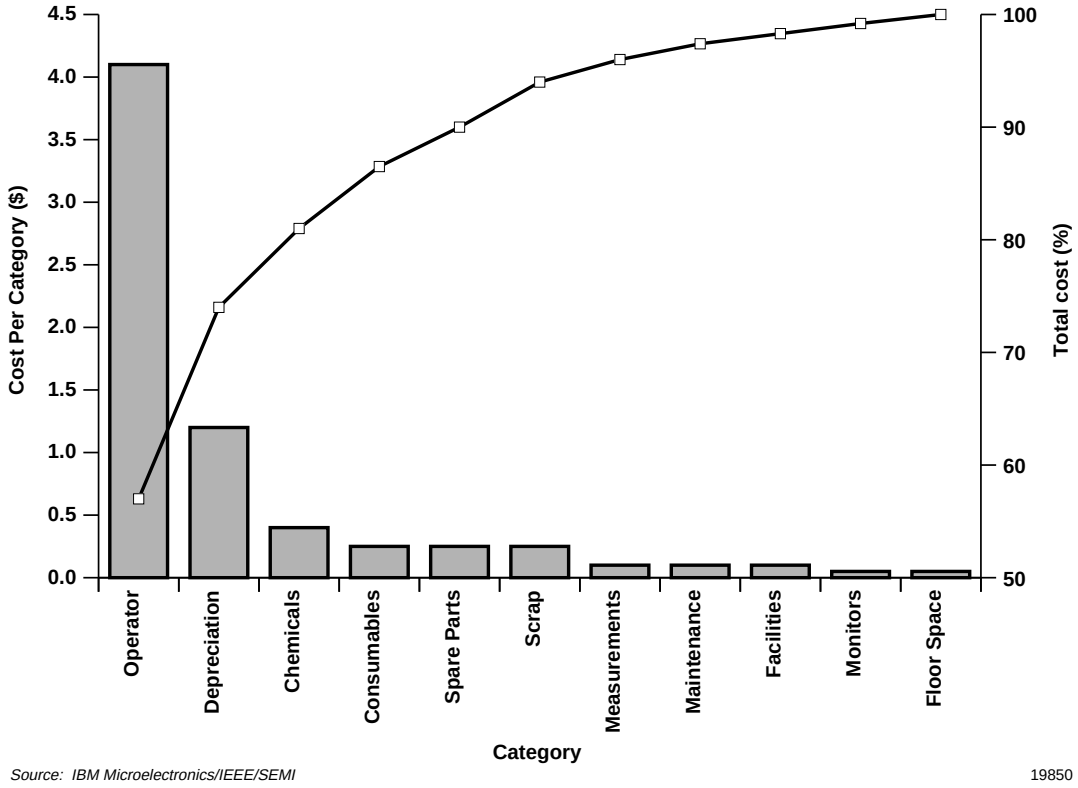


Figure 4-17. A Pareto Chart Indicates Areas to Focus on to Reduce Total Cost

Labor Productivity

Labor productivity in actual fabs is shown in Figure 4-18. As indicated, the most competitive fabs in the study completed 63 layers per operator per day. The least competitive was at 8 layers and the average was 29.6 layers processed per operator per day. Expanding beyond direct labor, the labor productivity in layers completed per total staff per day ranged between 3.3 and 37.7 with the average coming in at 17.6 layers per individual per day.[6] Other information in this table indicates the dramatic differences in performance among semiconductor fabs worldwide.

Metric	Best Score	Average Score	Worst Score
Cycle Time per Layer (Days)	1.2	2.6	3.3
Line Yield per Ten Layers (%)	98.9	92.8	88.2
Murphy Defect Density (Defects/cm^2)			
0.7 - 0.9μm CMOS Memory	0.28	0.74	1.52
0.7 - 0.9μm CMOS Logic	0.28	0.79	1.94
1.0 - 1.25μm CMOS Logic	0.23	0.47	0.96
1.3 - 1.5μm CMOS Logic	0.21	0.61	1.15
5x Stepper Throughput (5x Layers Completed per Machine-Day)	724 (30 w/hr)	382 (16 w/hr)	140 (6 w/hr)
Direct Labor Productivity (Wafer Layers Completed/Operator-Day)	63.0	29.6	8.0
Total Labor Productivity (Wafer Layers Completed/Total Staff-Day)	37.7	17.6	3.3
On-Time Delivery (% of Line Items With 95% of Die Output on Time)	100%	89%	76%

Note: Average and worst scores are calculated after discarding the worst data sample for each metric.

Source: UC Berkeley/ICE, "Mid-Term 1996" 21069

Figure 4-18. Results of Competitive Semiconductor Manufacturing Survey

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