8

Useful Methods for Improving Equipment Performance in Manufacturing

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As IC manufacturing costs continue to rise and profitability becomes more difficult to maintain, IC manufacturers are increasing their focus on the cost effectiveness, flexibility, and longevity of existing fabs. As a result, existing fabs are implementing a variety of equipment improvement programs (EIPs) and management strategies to increase the company's utilization of assets (employees, as well as equipment and materials). Lines previously drawn between management, engineering, and operators are also being removed to allow proactive improvements in fab operations.

This chapter focuses exclusively on improving the cost effectiveness of existing fabs. There are over 800 fabs in operation today that are continually challenged to reduce manufacturing costs. These fabs strive for on-going performance improvement, while dealing with the limitations of existing facilities, such as older equipment sets and limited funding for new technology. Especially during years of industry slowdown, companies must continuously improve equipment performance and fab productivity in lieu of purchasing new equipment and new fabs.

Next, equipment improvement programs that improve the performance and productivity of equipment are presented. Examples include the upgrade of wet processing stations; development of a manufacturable, collimated sputtering system for Ti/TiN deposition; improvement of tungsten etch and CVD systems; characterization of a batch RIE reactor; and improvement of an APCVD system. This section is followed by a discussion of cost modeling and examples demonstrating when new equipment purchases become feasible.

Equipment-level Hardware and Software

IC manufacturers generally instituted equipment improvement programs (EIPs) when equipment is new, or, is being used in production and may not be consistently performing to specification and requires frequent maintenance. Typically, new equipment that provides the necessary process results in the prototype or R&D stages must be modified to allow its use in a manufacturing environment. Manufacturability must be improved to reduce downtime due to scheduled and unscheduled maintenance, identification and elimination of the causes of high particle levels, and generally, reducing processing costs.

In addition, an improvement program might be initiated because the system is exhibiting high downtime and is identified as the cause of yield loss. Efforts to improve system throughput might be performed when a tool is causing grid-lock, limiting fab productivity. For instance, if a CVD tool is typically

waiting for product from a photoresist stripper, an improvement program on the stripper that reduces process time would allow a more continuous flow of wafers through the line. Finally, EIPs are performed to improve the performance of existing equipment sets that will be used to process the next generation of devices. As requirements change, process capability usually needs to be extended, and issues such as uniformity, equipment availability, and others, may become more pronounced. EIPs are either performed independently by the IC manufacturer, or in conjunction with the equipment or material suppliers.

Here, the results of six specific EIPs are reviewed including:

- Motorola's use of response surface methodology to improve a multilevel-metal etch process using a batch hexode reactor[1],
- AMD's use of an in-line particle monitor to reduce the defect density of an integrated tungsten CVD-etchback process by 10-fold[2],
- Intel's use of Failure Modes and Effects (FMEA) analysis to eliminate a wafer backside contamination issue in a W-CVD system, and to eliminate uniformity problems that resulted from upgrading the W-CVD system from 150mm to 200mm processing[3],
- Digital's modification of an oxidation furnace to enable processing of thin reoxidized nitrided oxide films for 0.5µm manufacturing[4],
- Varian's and Sematech's co-development of of a manufacturable process for collimated TiN CVD[5],
- Intel's improvement of an APCVD's exhaust system to improve film thickness uniformity[6], and

- IBM's upgrade of six automated wet stations at a cost of $1.9 million, saving nearly $7 million over the price of purchasing new systems.[7]

Refining a Batch, Multilevel Metal Etch Process

Design of experiments is a commonly used method of process development today. It can also be used to improve existing processes. At Motorola's MOS 12 fab, engineers recently improved the performance of a hexode batch etcher using screening experiments and response surface methodology.[1] These techniques allowed the optimization of individual step chemistries in a multilevel metal RIE process. Targeting three critical parameters, etch rate, uniformity and selectivity, the bulk etch process included:

- Descum of residual (undeveloped) photoresist from high aspect ratio openings,
- Etch of the hardmask (plasma enhanced oxide) used for profile control,
- Metal etch of Al-Cu (1.5 percent),
- TiW etch, and
- Passivation to prevent post-etch corrosion.

Motorola's process was a four-layer, Al-Cu metal/polyimide dielectric interconnect on 100mm silicon wafers, that used the Applied Materials' Precision 8300 hexode RIE system to simultaneously etch the metal stack.[1] Tools used in the study included cross-sectional analysis to view sidewall profiles, Tencor Alpha-Step 100 or Nanometrics Nanospec, and SEMs. Original screening experiments identified the key variables that determine the desired results (including etch uniformity, etch rate, and selectivity). In the descum process, a fractional factorial design identified that DC bias and pressure accounted for 90 percent of the variation in

etch rate, while 88 percent of the variation in uniformity was modeled by DC bias, pressure, and O_2 flow. A four factor response surface experiment allowed simultaneous optimization of the hardmask etch rate, uniformity, and etch selectivity at 250Å/min etch rate and greater than 3:1 hardmask to photoresist selectivity (Figure 8-1). The experiments allowed a catering of process needs. For instance, in this process, load sizes typically vary and the engineers wanted to optimize the metal etch for constant etch rate and good uniformity across various load sizes. The original CF_4 metal etch chemistry was replaced with CHF_3 and Cl_2 (to prevent undercutting), followed by a CF_4/O_2 step to promote anisotropy. Response surfaces and experiments led to an optimized RIE process with known relationships between process parameters (i.e., DC bias, pressure, and chemistry) and results (etch rate, selectivity, and etch uniformity).[1]

Improving Tungsten CVD and Etch Processes

AMD developed an in-line defect density monitor to dramatically improve existing tungsten CVD and etch processes.[2] In this study, failure analysis revealed that tungsten deposition and etchback steps were responsible for both low average yields and catastrophic yield depressions. AMD developed an in-line defect density monitor to measure the defect contribution for tungsten deposition and etchback. By continuously monitoring the process, factors of ten improvements in equipment, processes, and maintenance were realized, while product yields improved and low yield excursions were eliminated.[2]
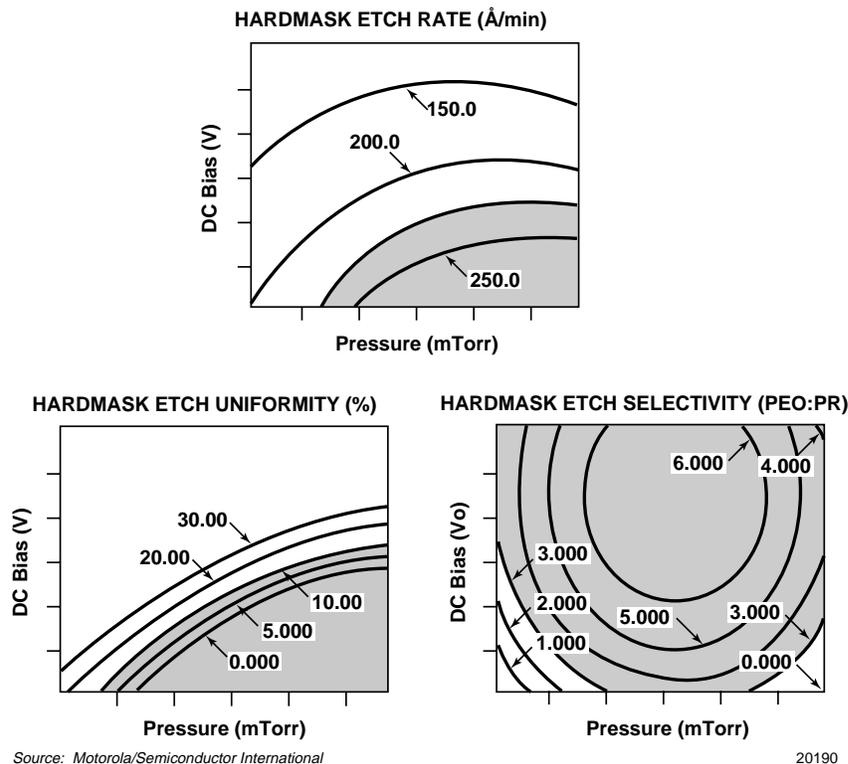
HARDMASK ETCH RATE (Å/min)

HARDMASK ETCH UNIFORMITY (%)   **HARDMASK ETCH SELECTIVITY (PEO:PR)**

Source: Motorola/Semiconductor International

20190

Figure 8-1. Shaded Areas of Response Surfaces Indicate Process Windows

The Contamination Free Manufacturing Group at AMD developed a laser scanning inspection test that allows real-time process monitoring of a tungsten plug process. The inspection system used was an Inspex-3500 patterned wafer inspection tool. The monitor wafer was first patterned and etched to provide alignment marks for the inspection system and a focal plane during review. The wafers had a Ti/TiN adhesion layer that was rapid thermal annealed (RTA). The monitor could reliably detect $0.7 \mu m$ defects. The monitor wafer was run as the first wafer in each product lot. It was scanned before processing, underwent CVD and etch, then was scanned again. The goal was to reduce defect density of the integrated tungsten deposition and etchback process by a factor of three.[2]

The result, based on the solutions shown in Figure 8-2, was a ten-fold reduction in defect density as measured by the integrated defect monitor. In addition, the monitor wafer was used to prevent the misprocessing of wafers under high defect density conditions. Figure 8-3 gives, on an arbitrary scale, the die yield

for a part that used the tungsten plug process, labeling the points at which performance improvements were implemented.

Eliminating Backside Contamination and Uniformity Issues in a Tungsten CVD System

One strategy commonly used for equipment improvement is FMEA (Failure Modes and Effects Analysis), a systematic method used to identify potential failure modes (causes) in semiconductor manufacturing, resulting in a ranked priority of fab and die yield improvement activities. The FMEA approach typically involves the documentation of:

- Unit process step,
- Process owner (responsible engineer),
- Process failure modes (i.e., backside contamination),
- Potential effects of the failure (i.e., low yields, contamination of subsequent chambers),
- Potential causes of the failure (tungsten CVD process),

| Problem Detected by Monitor in CVD and Etchback Systems	Solution
Heat transfer from wafer heaters caused deposition inside the CVD shower head, leading to deposition of large defects ($1-5\mu m$) on wafer	CVD system supplier provided and installed a water-cooled version of the shower heads, preventing problem from reoccurring for 1 year
Gas phase nucleation in CVD chamber due to 1:1 ratio of $SiH_4 : WH_6$	Revised timing of reactive gas introduction
Increased CVD system defect density due to clogging of dry pump burn box of process gases, also affecting pumping capacity	Altered preventive maintenance of pump to maintain system cleanliness
Periodic detection of Ti/TiN and W flakes on wafers after etch back	Periodic cleaning of etch chamber with dilute mixture of H_2O_2 in H_2O

19981

Figure 8-2. Improving Defect Density in Tungsten CVD and Etch Processes

- Current controls,
- Rating of risk factors (rated for severity, occurrence, and detection),
- Assignment of risk priority numbers, and
- Recommended actions given to eliminate the problem.

Intel recently used an FMEA program, together with Finite Element Modeling to identify and rectify the cause of low yield on a tungsten CVD system.[3] In this example, the backside tungsten (BSW) deposition problem was first detected by a downstream wet station that reported higher than normal levels on the station monitor. Effects of the failure were low line yields and contamination of several steppers, lithography tracks, diffusion furnaces, and wet stations.

Tungsten CVD steps include: the nucleation, the bulk deposition, and the backside etch (BSE) steps. BSE can be performed by elevating the wafer in the chamber, so that it is flush with the showerhead at the top of the chamber, and an RF plasma is used to remove residual tungsten left on the wafer backside from the deposition. The FMEA study revealed that wafer placement and argon flow were the most important causes of problems (Figure 8-4). Wafer placement was corrected by visually checking it on a regular basis. Changing the argon MFC and regularly checking the calibration factors on the MFCs on a weekly basis solved the problem. Finite element simulation using a commercially available program, FIDAP, revealed several process regimes (with different gas flow rates), where redeposition was more likely to occur. Long term, simulation was used to develop improved process recipes.[3]
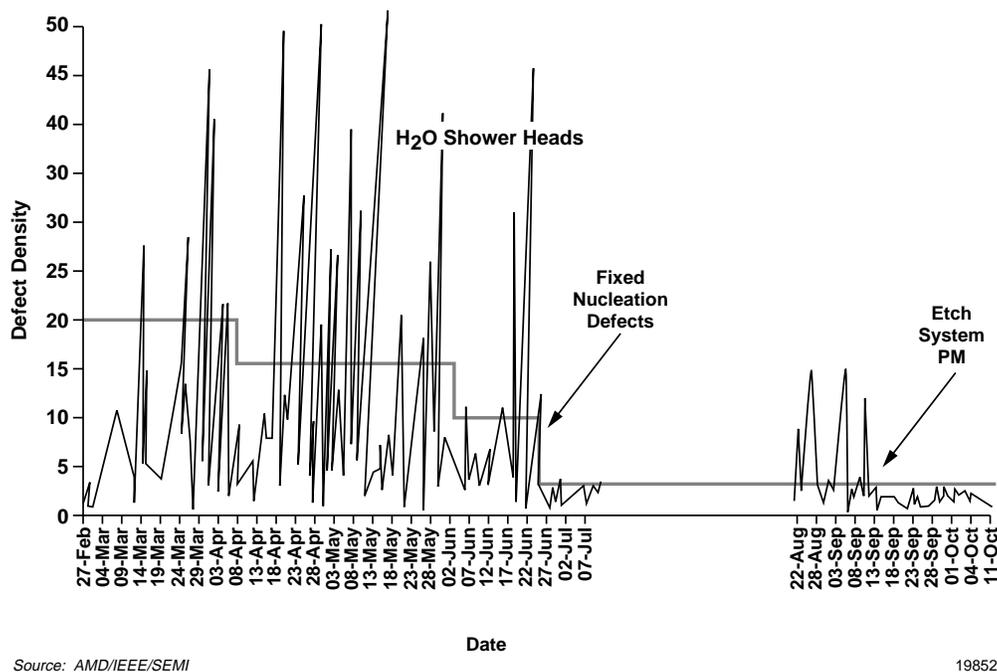
Source: AMD/IEEE/SEMI   19852

Figure 8-3. Factor of Ten Reduction in Defect Density for a Tungsten CVD Tool

Equipment Name: ABC Reactor
Subsystem/Function: LPCVD/W

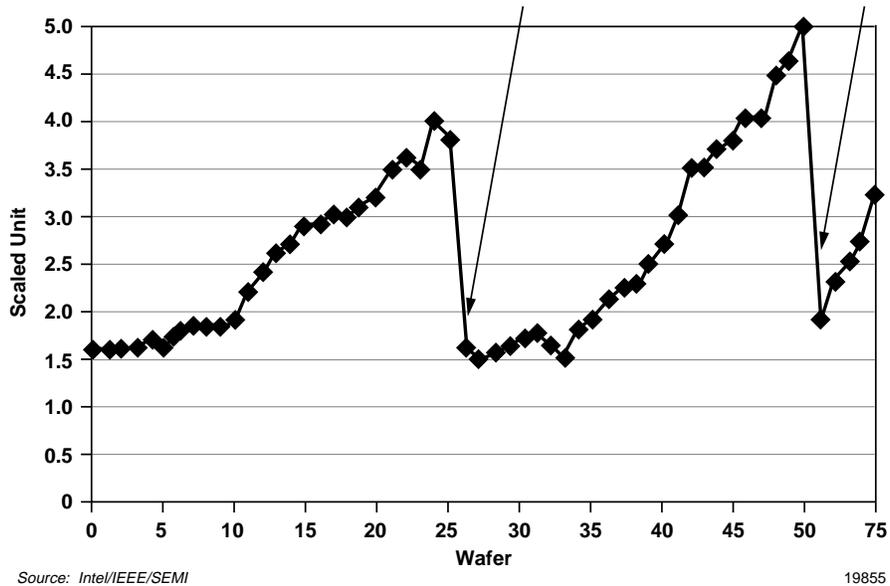| Causes	Occurrences	Effects	Severity	Detection	Protection	RPN	Recommended Actions
Argon Flow	7	Uniformity	6	MFC fault	8	336	Check MFC calibration weekly
Wafer Variability	5	Different backsides susceptible to deposition	2	Not detected	8	80	Run limited product types
Pressure (baratron)	2	Change in deposition rate	8	Not detected	6	96	Calibrate weekly
Pressure Circuits	0	Change in display	8	Not detected	6	0	N/A
Inadequate Chamber Clean	0	Residual W in chamber gives residues over time	5	Higher defects after several wafers	2	0	Check software revision
Wafer Placement	13	WF_6 seeps under the wafer	4	Uniformity	4	208	Check robot belt tension
Spacing	3	Backside etch uneven	2	Visual and uniformity	2	12	Lube shafts

Source: Intel/IEEE/SEMI   19854

Figure 8-4. FMEA for Backside Tungsten Deposition Problem

Intel followed this EIP with a second project designed to eliminate poor uniformity of a tungsten CVD process resulting from directly scaling-up a 150mm process to a 200mm process (Figure 8-5)[3]. To make a manufacturing-worthy process, the engineers conducted process simulations and an FMEA. The model showed the presence of vortices at the edge of the wafer where reactant gases from the top and the argon purge from the bottom merge before getting pumped away. The FMEA (Figure 8-6) pointed to residue accumulation of fluorine in the reactor chamber due to the higher amount of WF_6 used to process the larger wafers. This was the cause of the uniformity drift, subsequently confirmed by residual gas analysis. The action taken was to introduce inert purge between wafers, and increasing pumping speed by increasing pump size and inner diameter of pumping line. These actions reduced the uniformity drift from every 25 wafers to approximately 150 wafers. To further improve the process, the susceptor ceramic ring spacing was later increased and the flow rate of the bottom purge was lowered to reduce vortices at the edge of the wafer and improve uniformity.

In these studies, Intel recommends using the FMEA to solve process and equipment problems in the manufacturing line because it is easier than simulation studies and uses less resources. In both cases, the FMEAs quickly led to the root causes of the problems. One further recommendation was the use of modeling techniques at new equipment and process development stages.[3]

Source: Intel/IEEE/SEMI   19855

Figure 8-5. Uniformity for the Original Tungsten CVD 200mm Process

Equipment Name: **ABC Reactor**
Subsystem/Function: LPCVD/W

Causes	Occurrences	Effects	Severity	Detection	Protection	RPN	Recommended Actions
Robot drift	7	Uniformity	5	None	8	280	Calibrate robot
MFC drifts	5	Uniformity	5	MFC fault	1	25	Perform calibration regularly
Gas delivery pressure	2	Unknown, MFC (?)	5	MFC flow	2	20	Observe
Pump speeds	0	All parameters	8	Interlocks	4	0	N/A
Residue Accumulation	0	Uniformity, others	5	None	9	45	Introduce inert purge Increase pumping speed

Source: Intel/IEEE/SEMI   19856

Figure 8-6. Failure Modes and Effects Analysis for Reactor Scale-Up

Developing a New Dielectric Process Using an Existing Furnace

Digital Equipment Corp. in Hudson, Mass., improved the manufacturability of a thin reoxidized nitrided oxide (ROXNOX) process, a new application for a horizontal oxidation furnace, developed for the processing of a 0.5μm, 3.3V, 64-bit microprocessor[4]. The Model BDF 41 furnace from Bruce Technologies was modified to allow low-pressure processing (Figure 8-7). To form sufficient nitrogen at the Si-SiO$_2$ interface, high-temperature processing (>950°C) was needed, and low pressure allowed better control of the oxidation rate. For this process, a very thin reoxidized nitrided oxide film (<100Å) was used to improve the hot carrier resistance of the gate. Running the prototype process in the existing furnace resulted in severe downtime due to equipment malfunctions, high particle levels and poor film uniformity. A series of equipment and process changes were performed to develop a production-worthy process. These changes resulted in a factor of two film uniformity improvement, a twenty percent improvement in equipment availability, a factor of two reduction in average particle counts, and significant reduction in the magnitude and occurrence of particle spikes.[4]

Figure 8-8 summarizes the hardware changes made to significantly reduce in-process particle levels and improve film uniformity to ±4Å. As a result of these changes, furnace availability was improved by 20 percent, and time spent performing unscheduled maintenance was reduced by 22 percent. Reduced standard deviations in both cases indicates better process stability. Particle tests, using test wafers at the front and rear of the furnace, measured on a Tencor Surfscan 4500, revealed significant improvements in particle levels and film uniformity (to ±3Å).

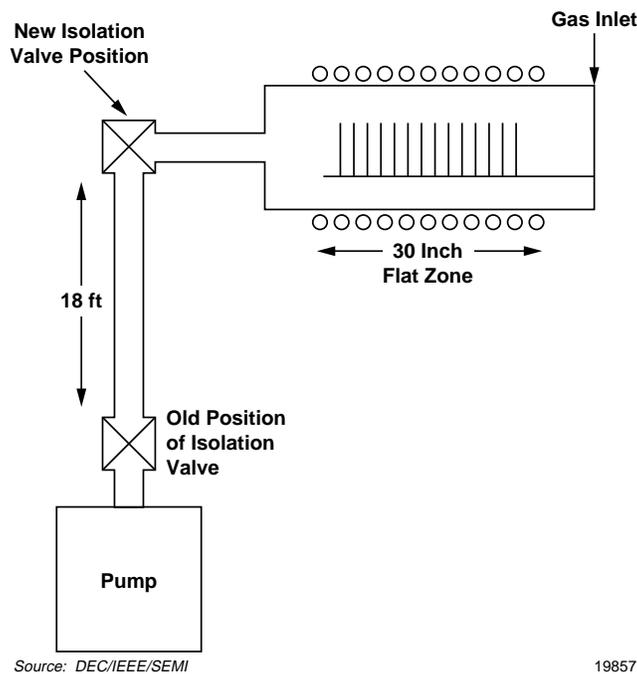Source: DEC/IEEE/SEMI   19857

Figure 8-7. Modified Diffusion Furnace Used to Process Thin Reoxidized Nitrided Oxide Films

Problem Encountered	Solution Used Improve Manufacturability
O-ring failures after 4 weeks of continuous operation on rear of tube and front door	**Initially replaced o-ring every 3 weeks, eventually extending the length of the tube to drop the temperature (rear), and redesigned the front door to place o-ring away from the radiation heat source**
High particle levels during initial pumpdown, due to rapid drops in pressure	**Installed a Flow Surge Suppression system to allow slow reduction in pressure during pump down**
High particle levels due to pump-line back-fill into process chamber as door was opened and chamber changed from low pressure to atmospheric	**Moved gate valve to back of the tube, and installed over/under pressure transducer, allowing interval advancing only when the transducer sensed equal pressure inside and outside the tube. Front door will not open until pressure inside equals pressure in fab**
High particle counts and film thickness non-uniformity due to programmed changes in pressure during processing	**Modified recipe to eliminate rapid pressure drops**

19982

Figure 8-8. Hardware Modifications Made to Improve the Manufacturability of a New Reoxidized Nitrided Oxide Process

Developing a Collimated Sputtering Process Using Existing Equipment

The next example also illustrates a procedure used to modify an existing piece of semiconductor equipment for a new application. Through a partnership between Varian and Sematech, a manufacturable process for depositing barrier metal (Ti/TiN) into sub-half-micron contacts and vias, using a collimated sputtering system was developed.[6] Using a modified version of Varian's M2000 PVD system, design of experiments was used to optimize the step coverage, thickness uniformity, material properties, resistivity, defect density, and cost of ownership of the process. "Marathon" tests, which led to the replacement of the collimator material and other modifications, significantly improved system manufactuability for use in $0.35\mu m$ processing. Over the course of a year, at least 14,000 wafers were processed. Daily calls, weekly conference calls, and monthly meetings between team members as well and quarterly reviews with the Sematech board, facilitated communication and cooperation.

The use of low contact resistance titanium films as a barrier metal is challenging due to the need to provide conformal sidewall coverage, with no thinning and no "shoulder cusping" in high aspect ratio (5:1 or more) structures. New CVD systems are competing with collimated sputtering tools for this application. Collimation, which is capable of controlling the angle of incidence in a sputtering environment (Figure 8-9), is one solution that may be able to extend barrier metal use well beyond $0.5\mu m$ processing. A key issue in collimated sputtering is the low useful life of the collimator, which has prevented its use in a manufacturing environment.
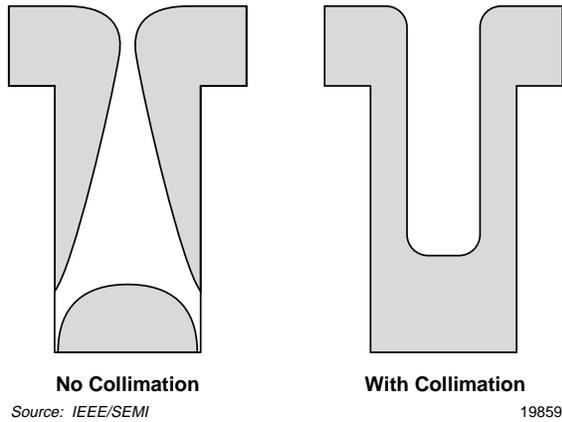
No Collimation **With Collimation**

Source: IEEE/SEMI   19859

Figure 8-9. Typical Step Coverage Profiles

| Contact Diameter (μm)	0.8	0.6	0.4
Aspect Ratio	1.4	1.6	2.3
Uncollimated Bottom Coverage	19%	N/A	4%
Collimated Bottom Coverage	50%	45%	40%
Uncollimated Sidewall	15-36%	N/A	3%
Collimated Sidewall	21-26%	19-22%	15-20%

Source: Sematech/Varian/IEEE/SEMI   19860

Figure 8-10. Step Coverage Comparison of Collimated Versus Uncollimated Ti/TiN Sputter Depositions

The system used in the Equipment Improvement Project between Sematech and Varian incorporated a degas station, magnetically-enhanced etch module, and collimated and uncollimated Ti/TiN modules[5]. Step coverage and bottom fill for collimated deposition showed substantial improvement over uncollimated films, particularly below 0.8μm contact width (Figure 8-10). Marathon tests revealed the need to replace the collimator material, which could not withstand the thermal environment and reduced the already slow deposition rate due to film build-up on the collimator. Through various changes, throughput was brought up to 20 wafers per hour (average), new collimator life was increased to over 10,000 wafers, system reliability was improved, and cost of ownership was improved by 33 percent. The program also led to classes in statistics, passive data collection, and basic design of experiments being taught at Varian by Sematech employees.[5]

Equipment Improvement Program for an APCVD System

After system operation demonstrated unpredictable film uniformity and high machine downtime, Intel performed an EIP on an APCVD system. The goal was to reduce the impact of air flow/exhaust fluctuations on film thickness uniformity.[6] The exhaust pressures from semiconductor process tools, and atmospheric tools in particular, have been known to be susceptible to changes and fluctuations. This problem becomes compounded in a rapidly changing cleanroom environment, caused by installation and/or removal of tools with different exhaust pressure requirements.

Intel first characterized the system using extensive "smoke" tests (Figure 8-11) and hot wire anemometer studies. Installation of panels to isolate the heater elements and the process chamber from unpredictable air flow resulted in temperature variability in the APCVD system to less than 10°C, despite fluctuations in the bay-to-chase air flow and scrubber exhaust. System availability and wafer-to-wafer BPSG thickness uniformity (Figure 8-12) were significantly improved.[6]
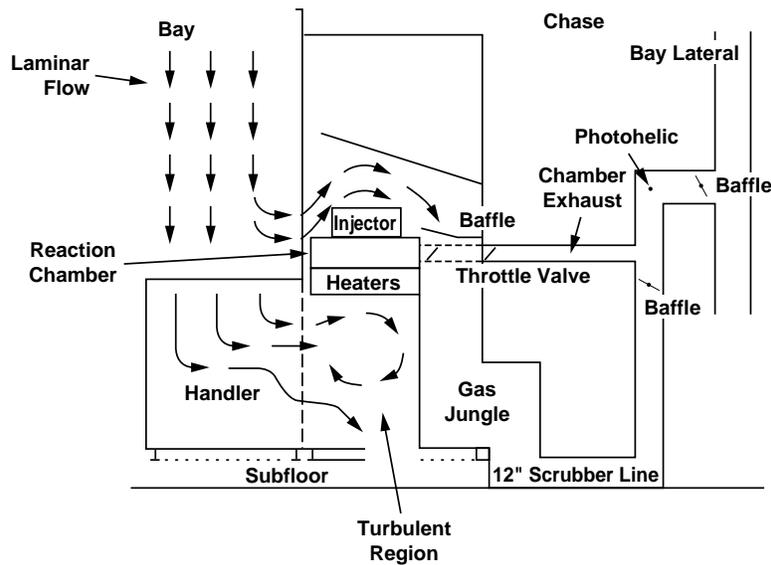
Source: Intel/IEEE/SEMI   19861

Figure 8-11. Side View of APCVD Air Flow Patterns
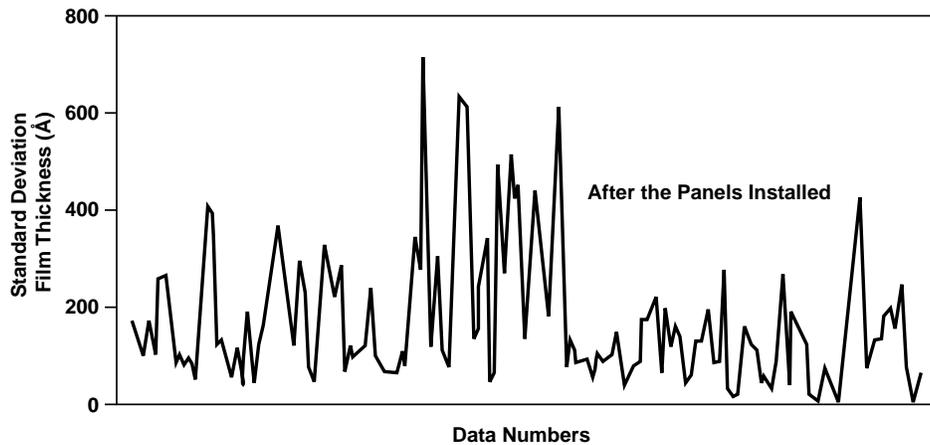
Source: Intel/IEEE/SEMI   19862A

***Figure 8-12. After Panels Were Installed to Isolate the Heater Elements,
Wafer-to-Wafer BPSG Film Uniformity Improved***

Rejuvenating 5-year-old Wet Stations

The final example demonstrates a complete upgrade program of six wet stations by IBM and Phoenix Process Automation, which cost $1.9 million, saving nearly $7 million of the cost of new wet station.[7] After 5-6 years of operation, the wet stations were characterized by excessive downtime, frequent chemical spills, high scrap rates, and reduced through-put. Engineers at IBM's Essex Junction, Vermont, fab and Phoenix Process Automation personnel worked closely to plan and implement a comprehensive upgrade program that included major improvements to hardware and software controls, to improve wet station reliability and productiv-ity. One added benefit to the year-long

upgrade program was the fact that it provided production-worthy wet benches in a faster turnaround time than new systems.

The upgrade required replacement of the control hardware, installation of new control software, completely upgraded plumbing, and refurbishing of the robots on the wet stations. Project steps are shown in Figure 8-13. This wet station upgrade led to:

• Extended wet station life,
• Doubled station capacity,
• Decreased losses caused by robot and control failures,
• Improved sanitation, and
• Increased yield

In addition, it also improved system throughput to over 120 wafers per hour, increased system availability to over 85 percent, extended mean-time-to-failure to 215 hours, and significantly reduced the number of chemical spills that occurred (Figure 8-14), thereby enhancing worker safety.[7]

The Attractiveness of Used Equipment

Over the last several years, used equipment has gained a big boost in the industry as cost-sensitivity and new equipment prices continue to rise. About 8 years ago, Texas Instruments formed a department specializing in purchasing refurbished tools. Since that time, many companies have followed suit. To date, about half of the total number of semiconductor manufacturers have taken advantage of the availability of used wafer

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• **Upgrade proposal planned between Project Manager at Phoenix, IBM process engineers, maintenance technicians, wet station operators, and equipment managers.**

• **Phoenix personnel set-up office on-site to coordinate detailed controls, plumbing and hardware rework investigation.**

• **Project manager drafted design specifications and outlined overall project schedules for six stations.**

• **Planning phase completed after six weeks. Equipment Procurement Specification signed by IBM and Phoenix.**

• **Arrangement of alternate process routes for product and safe removal of first sulfuric/nitric acid processing station. Removal and decontamination of robot and track, laminar hoods, and plumbing. Physical layout of station modules, electrical and electronic controls, facility drains, and control software.**

• **Installed new wafer transfer unit with 50-wafer capability (from 25).**

• **Refurbished flow hoods and installed frames. Reinstalled chemical and rinse modules. Drip pans installed.**

• **Installed new power distribution center. Upgrade of wet station was completed within 8 weeks.**

• **Process was repeated for five other stations.**

Source: ICE   19983

Figure 8-13. Steps Taken to Upgrade Six Wet Stations Saving $7 Million Relative to New Systems' Cost

processing, testing, and assembly equipment. Historically, the market for used assembly and test equipment has enjoyed the greatest success as a number of companies have marketed reconditioned or remanufactured testers, dicing saws, wire bonders, die bonders, etc., for years. In 1994, Hewlett-Packard officials reported that used equipment represented 10 percent of automatic test equipment (ATE) sales[8].

Aside from cost concerns, used equipment sales are also increasing due to the widespread availability of the systems today, which results from years of companies having to retire hundreds of systems. In addition, many companies manufacturing non-leading-edge chips would like to take advantage of the lower price of used equipment (typically 20-60 percent of new equipment prices). One of Motorola's older fabs, making bipolar memories and linear analog devices, saved 45 percent off new equipment costs by purchasing used equipment 25 times out of 77[9]. More recently, companies in regions of the world that have just begun

developing their semiconductor industry, such as China, are finding used equipment particularly appealing. In addition, overall equipment reliability has also improved dramatically since the early days of semiconductor manufacturing, making the used option even more attractive.

Used equipment goes by many names including "refurbished," "reconditioned," "remanufactured," and "pre-owned." Perhaps pre-owned is the most accurate term as the equipment typically retains a great percentage of its original value. Although strict definitions do not exist, users generally use "refurbish" or "recondition" to describe a system only requiring system cleaning and the replacement of a few parts prior to resale. Alternatively, if the equipment is rebuilt from the ground up, replacing some or most of the system components, the equipment is "remanufactured." Remanufactured equipment often must meet or exceed original equipment specifications and may be delivered with a one- or two- year warranty.
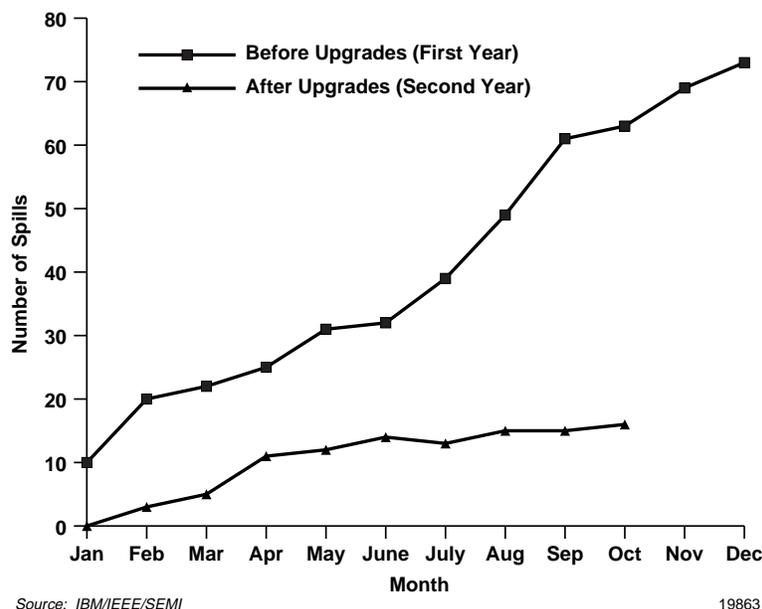

Source: IBM/IEEE/SEMI
19863

Figure 8-14. Reduction in Number of Chemical Spills Due to Wet Station Upgrades

Remanufactured equipment offers advantages of lower purchase price and faster return on investment than new equipment. Used equipment may also be immediately available through an IC manufacturer, equipment refurbishing company, or asset management company. The downside to purchasing pre-owned equipment includes the possible risk of owning and operating the equipment typically without OEM support, limited availability of spare parts, no warranty or service agreements, and poor system-to-system matching for tools that have been owned and operated in different fashions in the past.

For these reasons, some OEMs work with one specific company to ensure quality and performance of remanufactured systems. For instance, Lam Research's popular AutoEtch line of plasma etchers, of which over a thousand systems are installed worldwide, are being remanufactured and sold by Aspect Systems. Tegal is selling remanufactured versions of its 900 and 1500 series plasma etchers, with an installed based of over 1200 systems. Concept Systems caught onto this concept several years ago when it began remanufacturing Gemini I and II epi reactors, of which around 300 systems are installed. Another company, Raines Technology, built its business on remanufacturing plasma etchers, although it currently markets a variety of products. Karl Suss offers remanufactured versions of its machines, often ensuring that the systems have been maintained by Suss field personnel over the course of the machine's life. In addition to these companies, numerous small shops in key manufacturing areas will now remanufacture semiconductor equipment.

Evaluating Criteria for Used Equipment

Figure 8-15 lists the principle issues to consider when evaluating pre-owned equipment. In addition to these concerns, its helpful to keep in mind that certain systems, such as wet baths, chemical distribution systems, and gas cabinets, do not lend well to refurbishing, while photoresist processing systems, ion implanters, horizontal diffusion furnaces, epi reactors, CVD systems, and aligners do[9].

The Importance of In-situ Monitoring

There is an overwhelming need to monitor process parameters and wafer-level characteristics during processing, thereby detecting yield-limiting events as they occur. The need for in-situ sensors increases as the industry moves to larger wafers (200 or 300mm), and the value of the wafer being processed is so high that off-line process controls no longer suffice. In addition, as discussed in Chapter 1, it is not only the high price of monitor or particle-per-wafer-pass (PMP) wafers that makes them undesirable, but also their inability to precisely depict process conditions for the actual product wafers.

In-situ Particle Monitors

Perhaps the best candidate for in-situ monitoring of vacuum-based tool operation is the in-situ particle monitor. The beauty of in-situ particle monitors is that they can detect a wide variety of process problems, as many of them result in high particle levels (sampling shown in Figure 8-16). Most importantly, studies show that these monitors can result in an annual savings of $200,000 to $1.5 million for a single-wafer processing tool! Cost savings result from a

number of areas including the detection of misprocessing, the optimization of PM and chamber cleaning cycles, the elimination or significant reduction in test wafer usage, and real-time detection of particle bursts that lead to yield loss. In fact, in-situ particle monitors have the potential to eliminate test (PWP) wafer usage. In essence, in-situ sensors facilitate yield improvements and cycle time improvements that are virtually impossible without their use. They also provide a very promising path to true run-to-run or real-time process control. In addition, the key factor that has prevented their use in a production environment, the lack of availability on commercially available wafer processing tools, is being resolved as companies including Eaton, Lam Research, Genus, and Applied Materials, are beginning to offer in-situ particle monitors on their tools. At least part of this progress is due to the fact that

equipment vendors have been using in-situ particle monitors for process and product development for several years.

Estimated Cost Savings Above $200k per Tool

In 1992, Sematech engineers reported a $200,000 annual cost of ownership savings using an in-situ particle sensor in an Eaton NV-20A high-current ion implanter.[9] They realized a 4 percent decrease in the number of particles generated during the process and a 15 percent increase in tool availability due to improved operation of chamber cleaning cycles and reduction of ion beam current to minimize particle generation.[9] In fact, Eaton pioneered the offering of in-situ particle monitors as a standard option on its implanters.

- **Performance to specifications**
- **Installed base of the systems**
- **Necessary facility modifications**
- **Upgrade-ability and other configuration changes**
- **Application(s) for which the system was previously used**
- **Warranty**
- **Training**
- **Installation**
- **Equipment reliability (MTBF and MTTR)**
- **Preventive maintenance procedures, and time needed to requalify the equipment following downtime**
- **System condition**
- **System set-up, recipe storage capacity**
- **Initial system qualification -- what needs to be done and how long will it take?**
- **Typical throughput (wafers/month)**
- **Availability of spare parts, availability of additional units of the same system**
- **System-to-system matching**

Source: ICE   19979

Figure 8-15. Considerations for Purchasers of Used Equipment

| Process	Optimization
CVD	Determine effectiveness of dry cleaning process Ability to adjust gas flow rates to eliminate gas phase nucleation (W-CVD) Indicate need for electrode replacement
Etch	Determine process effects caused by using inherently dirty chemistries such as WF_6

Ion Implantation	Determine photoresist problems (i.e.: insufficient edge bead removal,
	   improper prebake, etc.)
	Ability to maximize beam current to increase throughput while
	   preventing resist burning
	Gain more effective use of cleaning procedures and gettering implants

Photoresist Stripping	Detection of incomplete stripping
Sputtering	Detect flaking on TiN and TiW films from clips or targets Detect cathode arcing Indicate need to change clamps Detect out-of-control wafer backside conditions
Diffusion	Detect leaks from chamber door Detect flaking from walls as temperature changes Detect the scraping of cantilevers
All Vacuum Processes	Directly indicates need for chamber cleans Indicate whether a chamber is ready for processing Detect leaking or degrading O-rings, valves, etc.

Source: Semiconductor International   19910

Figure 8-16. *Process Events Optimized Using In-Situ Particle Monitors*

Since then, a conservative $213,500 annual savings was estimated by a group of engineers from Sematech, Hewlett-Packard, Lam Research, and High Yield Technology, using an in-situ particle monitor on a Lam 4400 polysilicon and silicon nitride etcher (Figure 8-17).[11] Importantly, the group was able to correlate in-situ particle counts to functional yield, short loop monitors, and patterned wafer visual inspections. Cost savings resulted from the identification of misprocessing (in this case, accidental replacement of an empty C_2F_6 cylinder with a cylinder of CHF_3), the avoidance of yield loss due to an identified "seasoning" period following electrode replacement, and a reduction in usage of test wafers. Figure 8-18 shows the correlation between in-situ

particle counts per lot versus normalized lot yield, and Figure 8-19 shows the cost savings calculation.[11]

Most recently, LSI Logic and Lam Research showed that $1.5 million per year can be saved using an in-situ sensor in a Rainbow 4500 oxide etcher. This savings is due to increases in yield, extension of electrode life, and elimination of test wafer usage. In addition, a 15 percent increase in system uptime resulted from the optimization of PM and chamber cleaning cycles. The study's correlation between probe yield and in-situ counts is shown in Figure 8-20.[12] Importantly, this study showed that in-situ counts are more stable than PWP counts, causing LSI to eliminate the test wafer usage completely from this process.
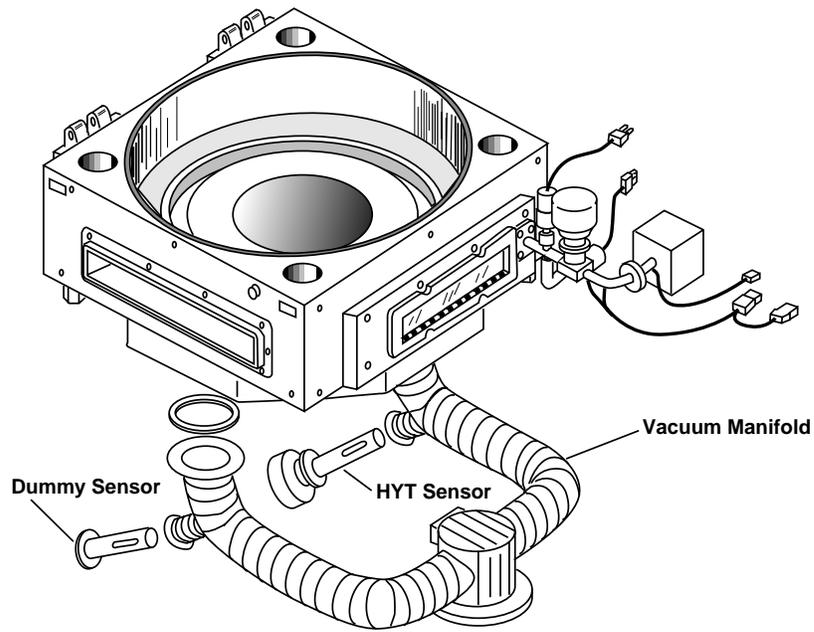
Source: Lam/HYT/IEEE/SEMI   19911

Figure 8-17. HYT Sensor Located in the Etch Chamber Vacuum Manifold of a Lam 4400 System
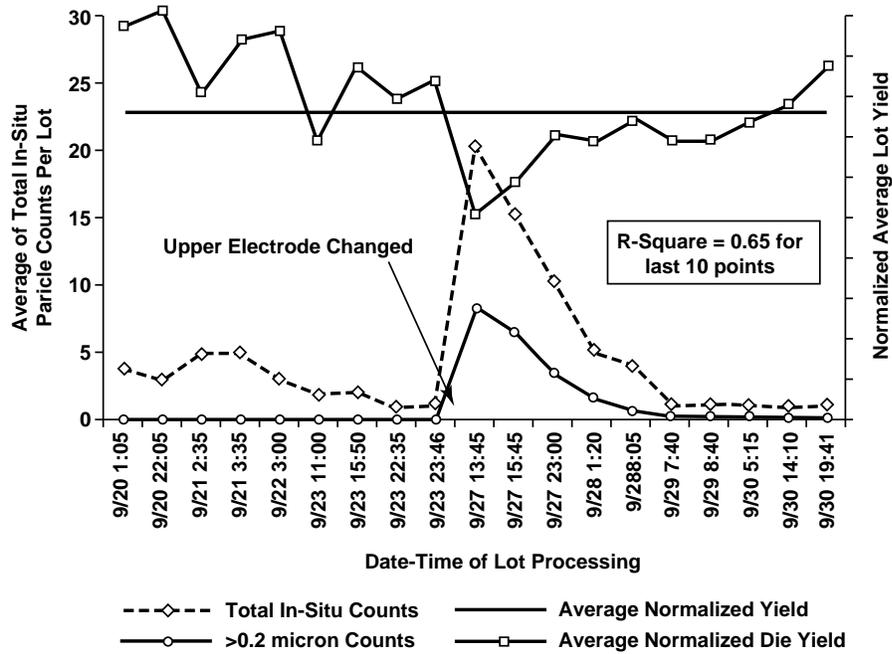
Source: IEEE/SEMI   19912A
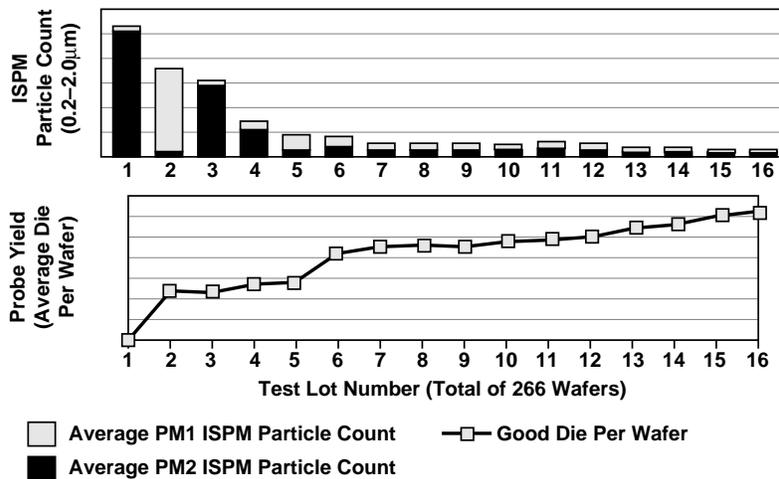
Figure 8-18. Correlation Between In-Situ Particle Counts and Yield

Event	Estimate of Wafers Saved	Estimate of Event Occurrence Per Year	Total Wafers Saved Per Year	Wafer Value at the Process Step	Savings Per Year (K$)	Change in Wafer Cost Based on COO ($)	Annual Change in COO (K$)
Electrode Change	20	12	240	$500	$120.0	$1.11	$166.7
PWP Wafers Per Week	18	52	936	$50	$46.8	$0.31	$46.8
Wrong Gas	24	1	24	$150	$3.6		
Total					$170.4		$213.5

Source: IEEE/SEMI   19913

Figure 8-19. *Potential Return on Investment Realized by Using In-Situ Particle Monitors*

Source: Semiconductor International   19914

Figure 8-20. *Good Correlation Between In-Situ Particle Counts and Probe Yield*

The critics of in-situ particle monitoring claim that the sensors are not sensitive enough, that they are too costly to implement in every piece of process equipment, and, most importantly, that they may impact the reliability and availability of the process equipment. Much of this skepticism stems for early sensor use where reliability was questionable. Today, production-worthy sensors are available from companies including High Yield Technology, Particle Measuring Systems (PMS), and TSI. The argument of sensitivity is not very relevant as often, when smaller particles are generated, large ones are also generated. In addition, unless the sensor is not detecting any particles (which has not been shown to occur), the particle data is useful.

The challenges associated with building in-situ particle sensors into process tools includes positioning the sensor so that counts accurately reflect counts at the wafer level and the sensor optics do not become coated with films. Most importantly, the enormous amount of data collected by in-situ particle monitors makes it very difficult to manage. However, with data storage capability increasing nearly every day, it is expected that such an analysis should prove possible very soon. Otherwise, techniques must be developed to record only particle bursts that represent out-of-spec processing conditions.

Other Promising In-situ Sensors

Beyond these applications, there are significant needs to monitor particle levels in process fluids (especially chemical purity and concentration in wafer cleaning/etching baths); critical dimensions (CDs) following photoresist development; uniformity, selectivity and CD control during etch; film thickness and composition during CVD and sputtering processes; and temperature during RTP, CVD, epitaxy, and etch processes.

During TI's MMST program, multi-point fiberoptic temperature sensors, acoustic thermometers, scatterometry systems and ellipsometers were developed for many of these purposes. For plasma processing, TI found that certain well-established processes, including polysilicon etch, tungsten etch, and nitride strip, are significantly improved with the addition of in-situ sensors (Figure 8-21). Resist ashing, on the other hand, is a well-established process that does not benefit considerably from the use of in-situ sensors.[13] Over the next several years, ICE expects at least some of these sensors to become available on commercial etch and stripping tools. Figure 8-22 lists some of the outstanding sensor needs for most wafer processes, as identified by TI. Here we include only the sensors needed to measure the process state (e.g., plasma density, delivered power) and the wafer state (e.g. film thickness, uniformity), as many of the equipment state parameters are already monitored by commercially available process tools.[14]

Process	Sensor Type	Sensor Use
Polysilicon Etch	Single wavelength ellipsometer	Endpoint control Etch rate and uniformity control
Silicon Nitride Etch	Monochromator	Endpoint control Etch rate and uniformity control
Tungsten Etch	Eddy current sensor Monochromator Critical dimension sensor	Endpoint calculation Endpoint control Pre-etch linewidth control
Silicon Nitride Strip	Special ellipsometer	Endpoint control Diagnostics
Resist Ash	Monochromator	Endpoint control Diagnostics

Source: Solid State Technology   19966

Figure 8-21. In-Situ Sensors for Plasma Etch Processes

	Process State [1]	Wafer State [2]

CVD		**Particles on wafer**
		  Film uniformity
		Dielectric film properties:
		  Index of refraction
		  Stoichiometry

PVD/
PECVD
	Wafer temperature
	Local or spatially resolved
	  plasma density
		Particles on wafer
		General film properties:
		  Thickness (deposition rate)
		  Uniformity
		  Index of refraction(dielectrics)
		  Sheet resistance (metals)

Oxidation		**Film uniformity**
Implantation	**Dopant energy** **Dopant dose**	**Particles on wafer**
Annealing/ **Diffusion**		**Particles on wafer** **Planarity (reflow)**
RTP/RTCVD	**Dynamic wafer temperature**	**Dopant activation** **Junction depth**
Lithography: **Coat**		**Resist thickness** **Resist uniformity**
Expose		**Latent image** **Image overlay**
Wet Develop	**Endpoint**	**Resist profile (width/height/slope)** **Latent image**
Silylation	**Endpoint based on latent** **image**	**Latent image**
Dry Develop	**As in plasma etch**	**Resist profile (width/height/slope)**
Chemically **Amplified Resist**	**Endpoint based on latent** **image**	**Latent image**

Plasma Etch	**Local or spacially resolved:**
	  Reactant concentration
	  Plasma density
	  Ion energy
	  Ion flux
		CD of resist (before etch)
		CD of etched feature
		Etch rate
		Etch rate uniformity

Wet Clean	**Solution conc. at wafer** **Fluid flow at wafer surface**	**Particles on wafer** **Surface roughness**

[1] **In-situ measurements required.**
[2] **In-situ measurements preferred, in line (e.g., metrology module on a cluster tool) is**
  a good initial alternative, off line, if necessary.

Source: Solid State Technology/ICE   19995

Figure 8-22. Sensor Needs for IC Manufacturing

In addition to these sensors, in-situ deposition rate monitoring, typically performed in research applications, is desirable in production-level thin-film deposition processes.[15] The key requirements for these sensors are cost effectiveness ($15,000/sensor) and reliability of the sensor when integrated into the hardware and process flow. Unless the sensor's reliability is at least as long as the time between preventive maintenance routines, one might have to shut the equipment down just to change (or clean) the sensor, which is not acceptable in a production environment.

Yield Modeling for New Equipment Decisions

To effectively reduce manufacturing costs, many manufacturers will attempt to use their equipment for as long as possible. However, as equipment is pushed beyond its original capabilities, often lower defect levels with existing equipment can only be attained at a higher operating cost, usually in the form of higher maintenance costs. Therefore, engineers must continually weigh the costs of acquiring and using new equipment, versus continuing to operate existing equipment at higher costs.

Yield modeling is widely used for various applications in the semiconductor industry to determine in-line yield loss, forecast factory outputs, and predict yield on future devices. Yield models help manufacturers focus on improvements needed to maximize yields and predict the effects of design or technology changes. The defect information used in yield modeling comes from equipment particle levels, actual defects detected on product wafers, and/or on back-calculations based on actual yields and failure analysis data.

Advanced Micro Devices (AMD) recently showed how yield models can be used to determine if it is more cost-effective to continue running existing equipment, or replace it with new and improved equipment.[16] The company currently uses a yield model to correlate in-line particle counts to actual yields on a die-for-die basis. Defects are classified, and "kill ratios" for defects based on type or origin, location on the device, and their relative size, are compiled at selected in-line inspection operations. Defects are related to yield using:

In-line defect density
x Area scanned
x # die tested/#die   =   Expected die loss
scanned x scaling   per wafer
factor (kill rate)

An example of defect kill ratios based both on defect size and classification is given in Figure 8-23. These types of charts are commonly used in manufacturing to provide a focus on the top issues relating to yield loss. In this example, yield loss is manifested in polysilicon shorts, scratches, general shorts, pattern defects, and source/drain shorts. By focusing on these top issues, the fab with limited resources can improve yields faster and more effectively.

AMD chose to measure yield impact against particles seen on real product. Once the average defect levels for a piece of equipment are determined, the cost in potential yield is:

Yield = #particles x Kill rate

Once the loss due to the current tool set is determined, the engineer must estimate the loss associated with newer generation equipment, which may replace the existing tool. A comparison is made by:

(Δ) Yield = (Δ) Particles * Kill rate

However, since kill rate is a function of defect size, the complete formula in die costs becomes:

$$\Delta\text{Savings}_{\text{new-old}} = \left[\sum_{i=o}^{n} \Delta\text{Particles}_i \times \text{Kill Rate}_i \right] \times \text{Die Cost}$$

i = Particle sizes
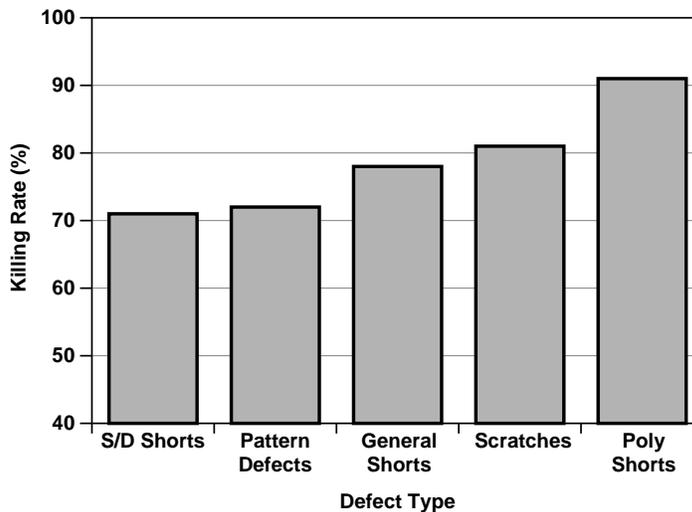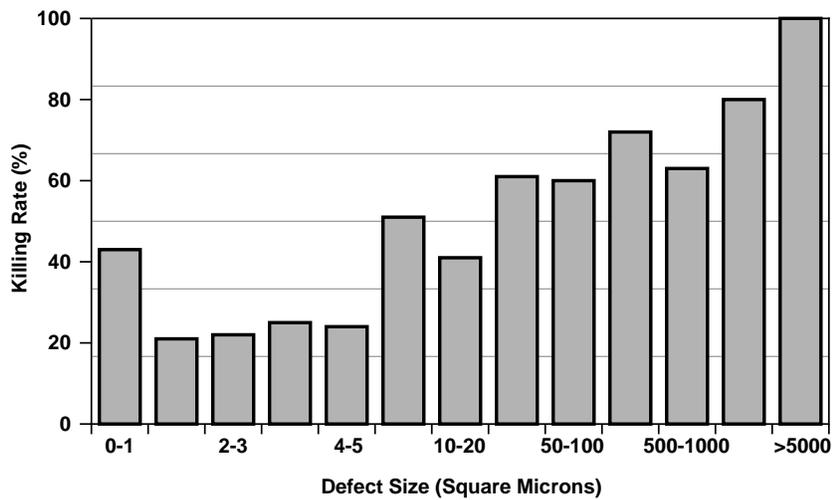
Source: AMD/IEEE/SEMI   19864

Figure 8-23. Yield Impact on Defect Size and Classification

The formula covers variables such as defect density, defect size, kill rates per defect size, and die cost. Frequently, however, defect kill rates can be very dependent on the location within a die, depending on whether the defect is on active or field regions of the chip. The equation becomes:

$$\Delta \text{Savings}_{\text{new-old}} = \left[\sum_{a} \sum_{i=o}^{n} \Delta \text{Particles}_{a,i} \times \text{Kill Rate}_{a,i} \right] \times \text{Die Cost}$$

i = Particle sizes

a = defect's die location

To calculate overall savings, one uses the above equation, the production run rate (wafers/week), and the price per chip produced. Given:

Die size	0.47 cm^2
Die/wafer:	150
Active area	0.12 cm^2
Price/die	$10.00
Run rate	250 wafers/week

The calculated cost saving is $11,668 per week. This substantial saving must be added to estimated savings resulting from improvements in line yield, maintenance costs, labor costs, chemical consumption, and power usage. When the saving is calculated, the question becomes, is the cost to purchase the new equipment and increase in per wafer processing costs, due to depreciation, offset by the payback in improved yields? Of course, the article warns that while this model will give a useful first-approximation of cost savings, other issues to consider in the purchase of new equipment include:

• Determining if there is another dominant yield limiting step in the process, which more critically affects yield.

• The certainty or predictability factor of the model developed and its application to all processes running in manufacturing.

• The degradation, over time, of chip price, which will lengthen pay-back periods, or the changing of product mix before equipment is installed.

• The ability to apply new equipment to improve the process at multiple operations, causing benefits of new acquisitions to go up.

• The numerous business issues including ROI, payback, and cost added from depreciation.

References

1. J.A. Chan, "Response Surface Methodology Improves Batch RIE Processing," *Semiconductor International*, Mar. 1995, p.5.

2. B. Anderson, A. Berezin, and I. Emami, "Defect Density Reduction in Tungsten Deposition and Etchback," IEEE/SEMI *Advanced Semiconductor Manufacturing Conference Proceedings*, 1994, p. 279.

3. S. Tripathi, et. al., "Comparison of the Applications of Process Simulations and FMEA: Two Case Studies," IEEE/SEMI *Advanced Semiconductor Manufacturing Conference Proceedings*, 1994, p. 140.

4. S. Bilotta and D. Proctor, "Development of a Manufacturable Low Pressure ROXNOX Oxidation Process," *IEEE/SEMI Advanced Semiconductor Manufacturing Conference Proceedings*, 1994, p. 39.

5. G. Actor, et al., "Partnering Works: A Case in Point," IEEE/SEMI International Semiconductor Manufacturing Science Symposium Proceedings, 1993, p. 74.

6. M. Moinpour, et al., "Factors Affecting the Temperature Stability of APCVD Systems in a Rapidly Changing Semiconductor Manufacturing Environment," *IEEE/SEMI International Semiconductor Manufacturing Symposium Proceedings*, 1993, p. 33.

7. N. Vedaa and M. Pakulski, "New Technology for Old Equipment," *IEEE/SEMI Advanced Semiconductor Manufacturing Conference Proceedings*, 1994, p. 220.

8. S. Loffredo, "Need an Etcher Fast? Try Used Gear Mart," *Electronic Business Buyer*, March, 1994, p. 36.

9. "How to Help Bottom Line Without Hurting Process Line," *Microcontamination*, Dec. 1993, p.10.

10. R. Burghard, D. Dance, and R. Markle, "Reducing Ion-implant Equipment Cost of Ownership Through In Situ Contamination Prevention and Reduction," *Microcontamination*, Sept. 1992, p. 27.

11. B. Busselman, et al., "In Situ Particle Monitoring in a Single Wafer Poly Silicon and Silicon Nitride Etch System," *IEEE/SEMI International Semiconductor Manufacturing Science Symposium Proceedings*, 1993, p. 20.

12. H.-D. Pham, M. Elzingre, and P. Borden, "LSI Logic Proves Yield Gain Using In-situ Monitor," *Semiconductor International*, April 1995, p. 101.

13. G. Barna, et al., "Dry Etch Processes and Sensors," *Solid State Technology*, January, 1994, p. 47.

14. G. Barna, M. Moslehi, and Y.J. Lee, "Sensor Needs for IC Manufacturing," *Solid State Technology*, April 1994, p.57.

15. R. Iscoff, "In-situ Deposition Rate Monitoring for Thin Films," *Semiconductor International*, Aug. 1994, p. 69.

16. M. McIntyre and J. Meitz, "Applying Yield Impact Models as a First Pass in Upgrade Decisions," *IEEE/SEMI Advanced Semiconductor Manufacturing Conference Proceedings*, 1994, p. 147.